



DMN2005LPK

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

NEW PRODUCT

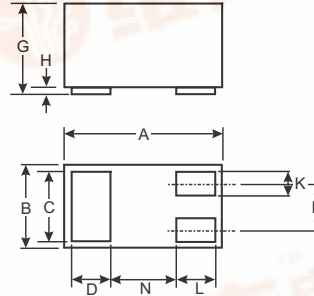
Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Lead Free By Design/RoHS Compliant (Note 2)**
- **"Green" Device (Note 4)**
- **ESD Protected Gate**

Mechanical Data

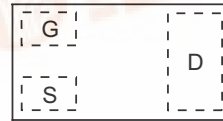
- Case: DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals Connections: See Diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking: See Last Page
- Ordering & Date Code Information: See Last Page

UNDER DEVELOPMENT

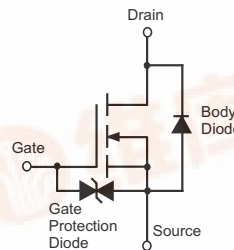


DFN1006-3			
Dim	Min	Max	Typ
A	0.95	1.075	1.00
B	0.55	0.675	0.60
C	0.45	0.55	0.50
D	0.20	0.30	0.25
G	0.47	0.53	0.50
H	0	0.05	0.03
K	0.10	0.20	0.15
L	0.20	0.30	0.25
M	—	—	0.35
N	—	—	0.40

All Dimensions in mm



TOP VIEW



EQUIVALENT CIRCUIT



ESD protected

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V _{DSS}	20	V
Gate-Source Voltage	V _{GSS}	±8	V
Drain Current per element (Note 1)	I _D	200	mA
Continuous Pulsed (Note 3)		250	
Total Power Dissipation (Note 1)	P _d	200	mW
Thermal Resistance, Junction to Ambient	R _{θJA}	625	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

- Note:
1. Device mounted on FR-4 PCB.
 2. No purposefully added lead.
 3. Pulse width ≤10μS, Duty Cycle ≤1%.
 4. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.



Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (per element) (Note 5)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0V, I_D = 100\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	$V_{DS} = 17V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 8V, V_{DS} = 0V$
ON CHARACTERISTICS (per element) (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	0.53	—	1.2	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	0.9	1.5	Ω	$V_{GS} = 4V, I_D = 10mA$
		—	0.85	1.7		$V_{GS} = 2.7V, I_D = 200mA$
		—	1.2	1.7		$V_{GS} = 2.5V, I_D = 10mA$
		—	2.4	3.5		$V_{GS} = 1.8V, I_D = 200mA$
		—	2.5	3.5		$V_{GS} = 1.5V, I_D = 1mA$
Forward Transfer Admittance	$ Y_{fs} $	40	—	—	mS	$V_{DS} = 3V, I_D = 10mA$

Notes: 5. Short duration test pulse used to minimize self-heating effect.

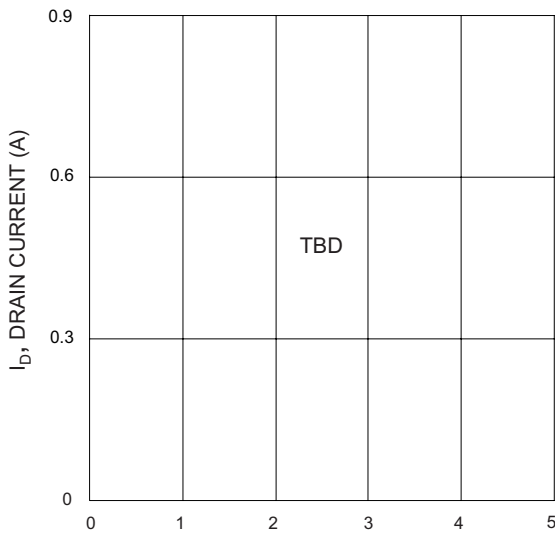


Fig. 1 Typical Output Characteristics

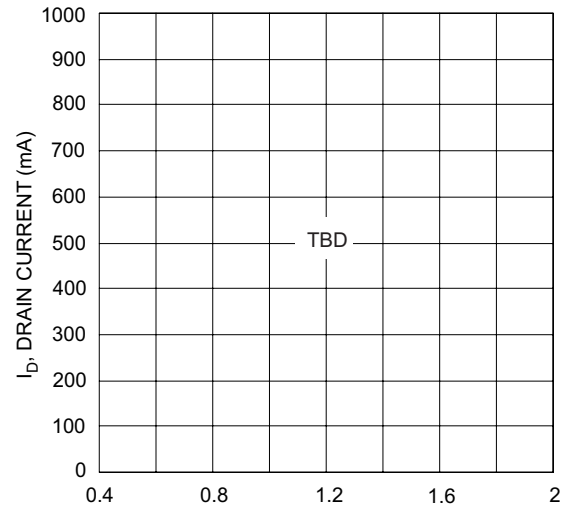


Fig. 2 Reverse Drain Current vs. Source-Drain Voltage

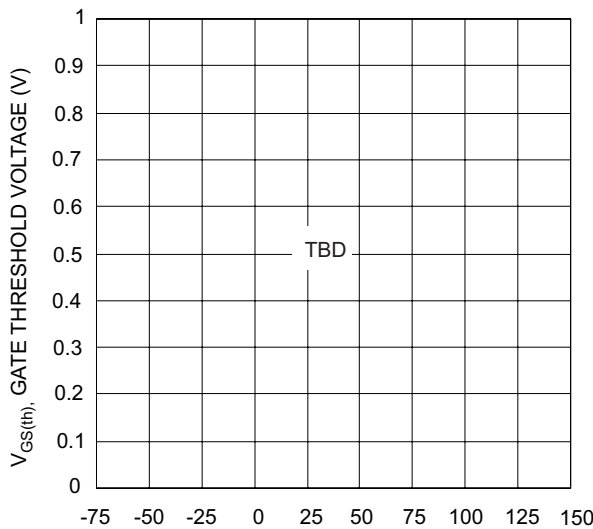


Fig. 3 Gate Threshold Voltage vs. Channel Temperature

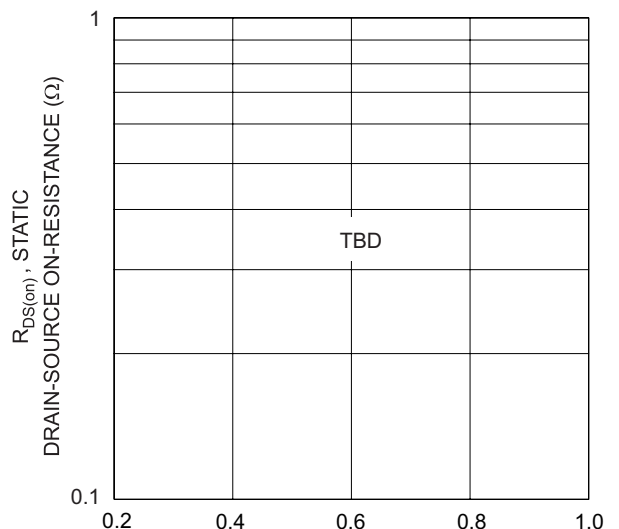


Fig. 4 Static Drain-Source On-Resistance Vs. Drain Current

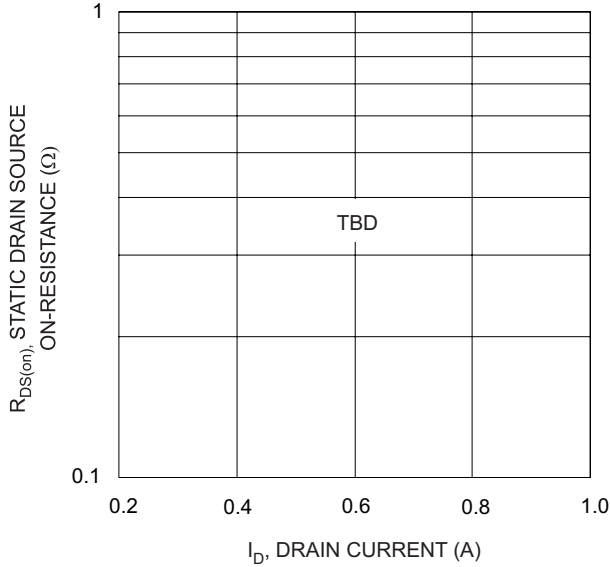


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

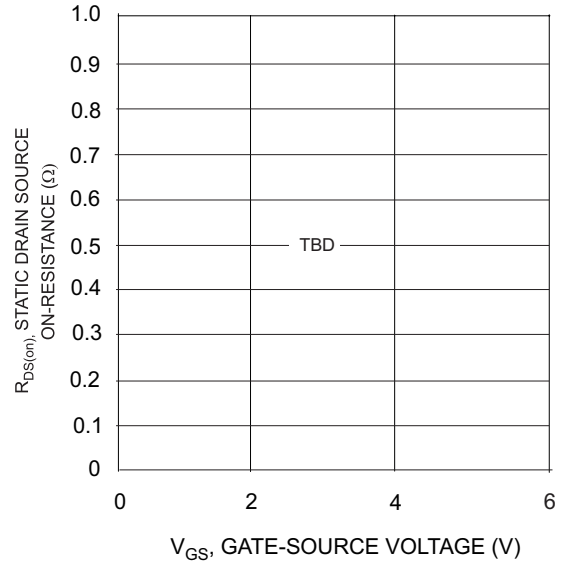


Fig. 6 Static Drain-Source, On-Resistance vs. Gate-Source Voltage

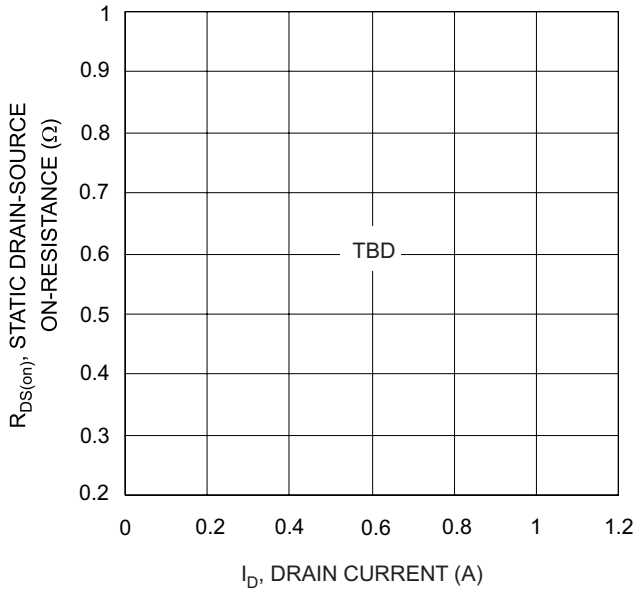


Fig. 7 On-Resistance vs. Drain Current and Gate Voltage

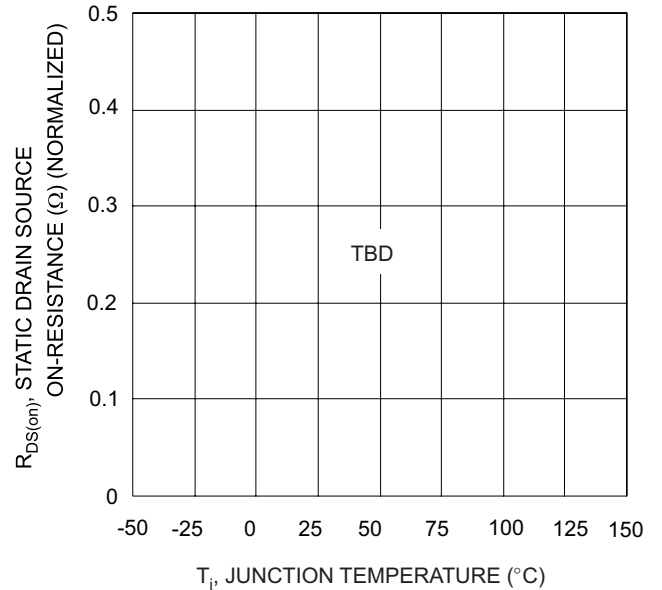


Fig. 8 Static Drain-Source, On-Resistance vs. Temperature

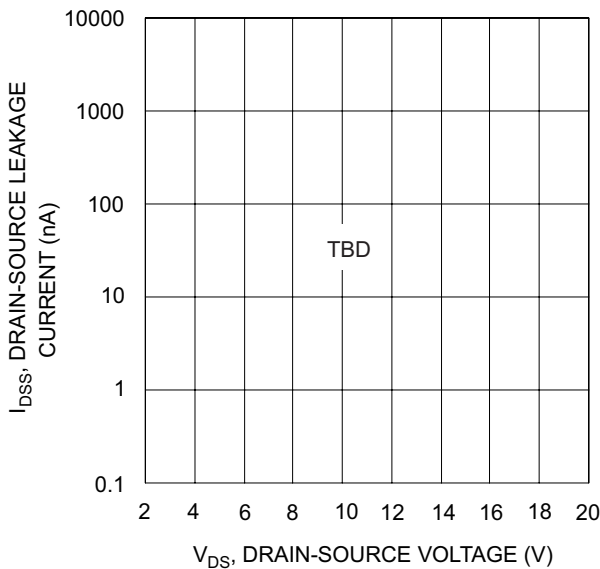


Fig. 9 Drain Source Leakage Current vs. Voltage

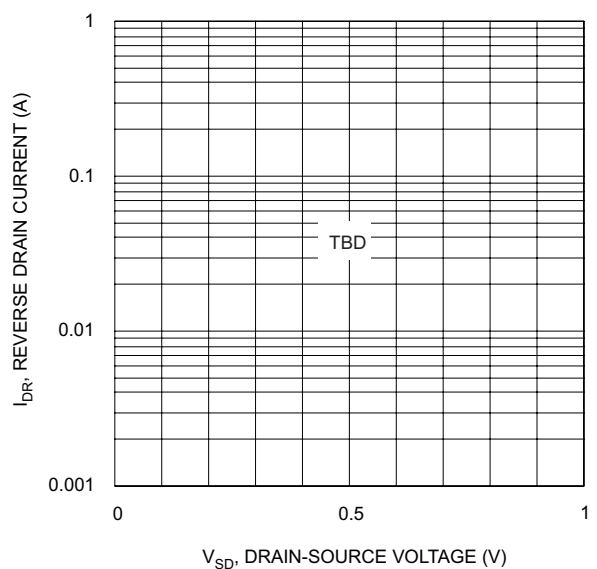


Fig. 10 Reverse Drain Current vs. Source-Drain Voltage

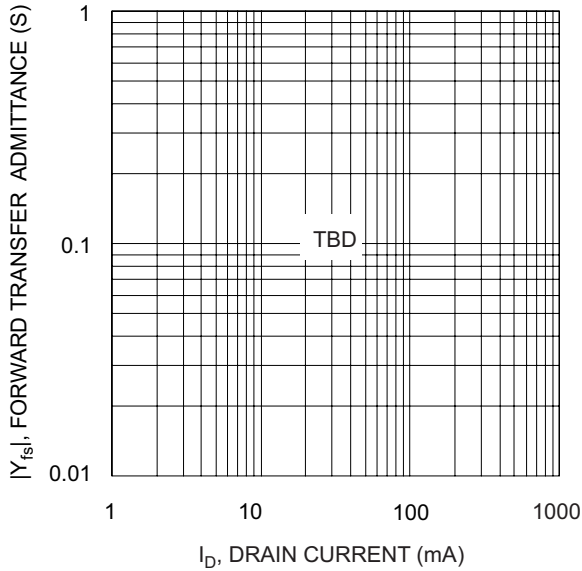


Fig. 11 Forward Transfer Admittance vs. Drain Current

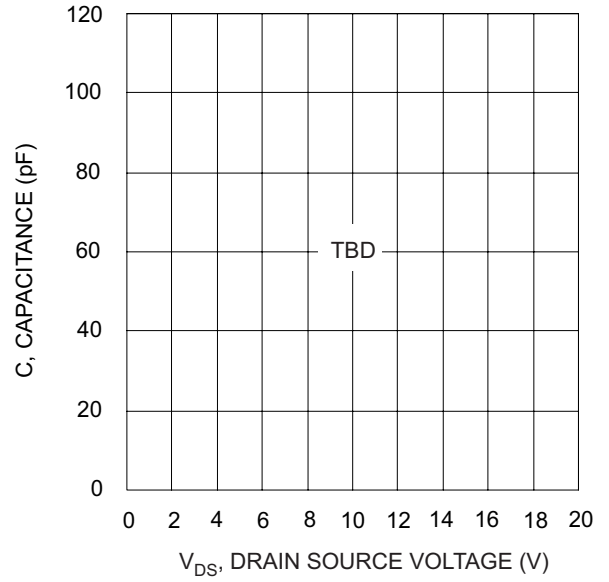


Fig. 12 Capacitance Variation

Ordering Information (Note 6)

Device	Packaging	Shipping
DMN2005LPK-7	DFN1006-3	3000/Tape & Reel

Notes: 6. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

Marking Information



DM = Product Type Marking Code,
Dot Denotes Collector Side

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