National Semiconductor

DP8510 BITBLT Processing Unit

General Description

The DP8510 BITBLT Processing Unit (BPU) is a high-performance microCMOS device designed for use in raster graphics applications. It implements, in high-speed pipelined logic, the data operations which are fundamental to BITBLT (BIT boundary Block Transfer) graphics: shifting, masking and bitwise logic operations. Under control of external hardware such as a state machine or a general-purpose microprocessor, it provides all necessary data path operations, easing the implementation of a wide variety of BITBLT systems. A number of input pins control the proper data flow in the BPU. A simple handshake scheme is used to interface the CPU, the BPU and the memory system.

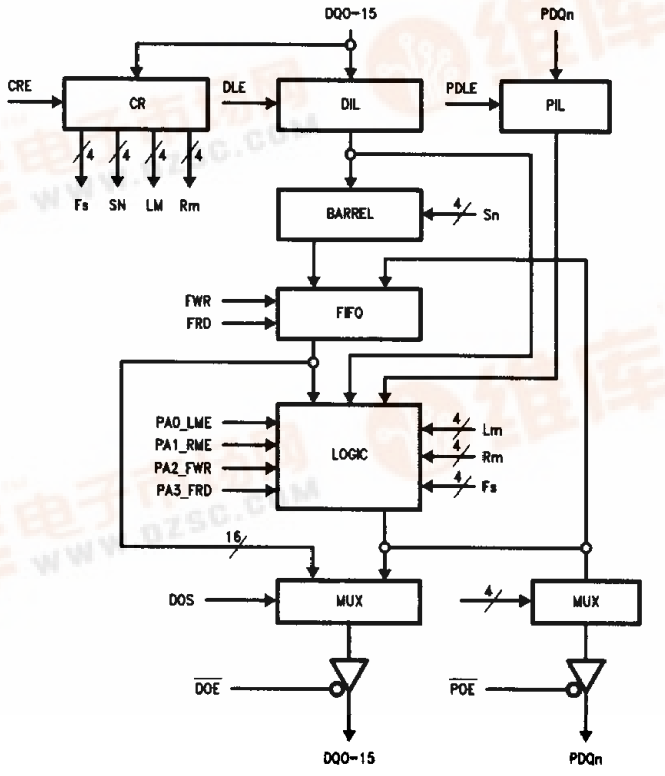
The BPU has two modes, BITBLT and line drawing. The mode is set by the $\overline{B}$/L pin. The line-drawing mode can be treated as a special case BITBLT with height and width equal to one.

In order to perform a BITBLT operation, the BPU's control register must first be loaded with four parameters: the shift number, left and right masks and the function select code, a total of 16 bits. BITBLT can then proceed, as directed by an external processor or state machine. It is the responsibility of the controller to generate appropriate addresses for the BITBLT, to interface with the frame buffer's memory control circuitry, and to control the BPU itself.

Features

- Supports all 16 classical BITBLT functions
- Pipelined data input for high system throughput
- Flexible architecture allows BPU to be used with a state machine or processor
- Multiple BPUs can be used for multiple bitplane/color applications
- Line drawing support
- Compatible with static or dynamic RAMs, including Video DRAMs
- Compatible with page mode, nibble mode and static column RAMs
- 32-bit to 16-bit barrel shifter
- 16-bit data port
- 16-word FIFO
- 16-bit logic operations
- 20 MHz operation
- Single +5 volt supply
- All inputs and outputs TTL-compatible
- Packaged in a 44-pin PCC (commercial) or 44-pin PGA (MIL)
- Single-bit pixel I/O port
- A member of National's Advanced Graphics Chip Set
- microCMOS technology

Block Diagram



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