National Semiconductor

April 2007

DS15BA101
1.5 Gbps Differential Buffer with Adjustable Output Voltage

General Description

The DS15BA101 is a high-speed differential buffer for cable driving, level translation, signal buffering, and signal repeating applications. Its fully differential signal path ensures exceptional signal integrity and noise immunity and it drives both differential and single-ended transmission lines at data rates in excess of 1.5 Gbps.

Output voltage amplitude is adjustable via a single external resistor for level translation and cable driving applications into 50-ohm single-ended and 100-ohm differential mode impedances.

The DS15BA101 is powered from a single 3.3V supply and consumes 150 mW (typ) at 1.5 Gbps. It operates over the full −40°C to +85°C industrial temperature range and is available in a space saving 3x3 mm LLP-8 package.

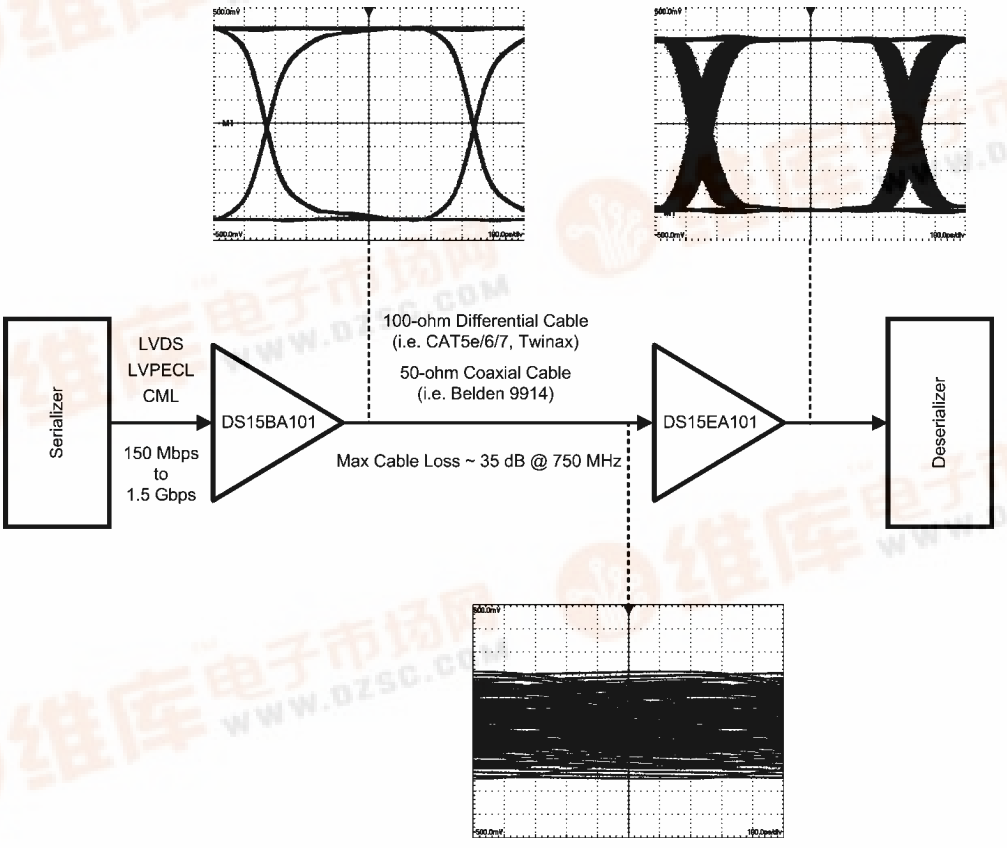
Features

- Data rates from DC to 1.5+ Gbps
- Differential or single-ended input
- Adjustable output amplitude
- Single 3.3V supply
- Industrial -40°C to +85°C temperature
- Low power: 150 mW (typ) at 1.5 Gbps
- Space-saving 3 x 3 mm LLP-8 package

Applications

- Cable extension applications
- Level translation
- Signal buffering and repeating
- Security cameras

Typical Application



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Absolute Maximum Ratings (Note 1)

Supply Voltage:	−0.5V to 3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Output Current	28 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance	
θ_{JA} LLP-8	+90.7°C/W
θ_{JC} LLP-8	+41.2°C/W
ESD Rating (HBM)	5 kV
ESD Rating (MM)	250V

Recommended Operating Conditions

Supply Voltage (VCC – GND):	3.3V ±5%
Operating Free Air Temperature (T_A)	
DS15BA101SD	−40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2, 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{ICM}	Input Common Mode Voltage	(Note 4)	IN+, IN-	0.8		V_{CC} – V_{ID}/2	V
V_{ID}	Differential Input Voltage Swing			100		2000	mV_{P-P}
V_{OS}	Output Common Mode Voltage		OUT+, OUT-		V_{CC} – V_{OUT}/2		V
V_{OUT}	Output Voltage	Single-ended, 50Ω load R_{VO} = 953Ω 1%,			400		mV_{P-P}
		Single-ended, 50Ω load R_{VO} = 487Ω 1%,			800		mV_{P-P}
I_{CC}	Supply Current	(Note 5)			45	49	mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{MAX}	Maximum Data Rate	(Note 4)	IN+, IN-	1.5	2.0		Gbps
t_{LHT}	Output Low to High Transition Time	20% – 80% (Note 6)	OUT+, OUT-		120	220	ps
t_{HLT}	Output High to Low Transition Time				120	220	ps
t_{PLHD}	Propagation Low to High Delay	(Note 4)		0.95	1.10	1.35	ns
t_{PHLD}	Propagation High to Low Delay	(Note 4)		0.95	1.10	1.35	ns
t_{TJ}	Total Jitter	1.5 Gbps			26		ps_{P-P}

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to GND.

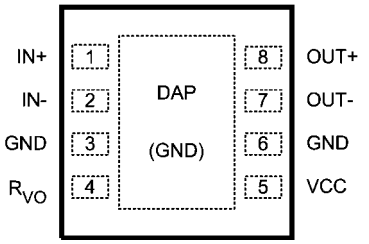
Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Note 4: Specification is guaranteed by characterization.

Note 5: Maximum I_{CC} is measured at V_{CC} = +3.465V and T_A = +70°C.

Note 6: Specification is guaranteed by characterization and verified by test.

Connection Diagram



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8-Pad LLP
Order Number DS15BA101SD or DS15BA101SDX
See NS Package Number SDA08A

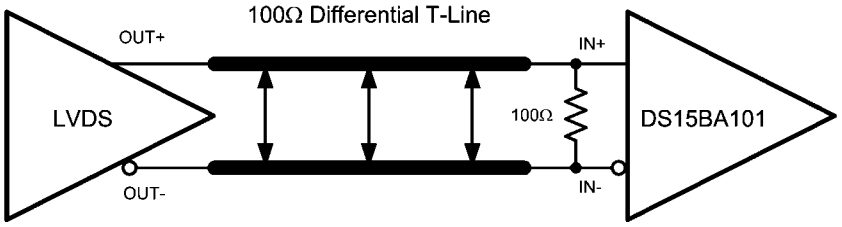
Pin Descriptions

Pin #	Name	Description
1	IN+	Non-inverting input pin.
2	IN-	Inverting input pin.
3	GND	Circuit common (ground reference).
4	R_{VO}	Output voltage amplitude control. Connect a resistor to V_{CC} to set output voltage.
5	V_{CC}	Positive power supply (+3.3V).
6	GND	Circuit common (ground reference).
7	OUT-	Non-inverting output pin.
8	OUT+	Inverting output pin.

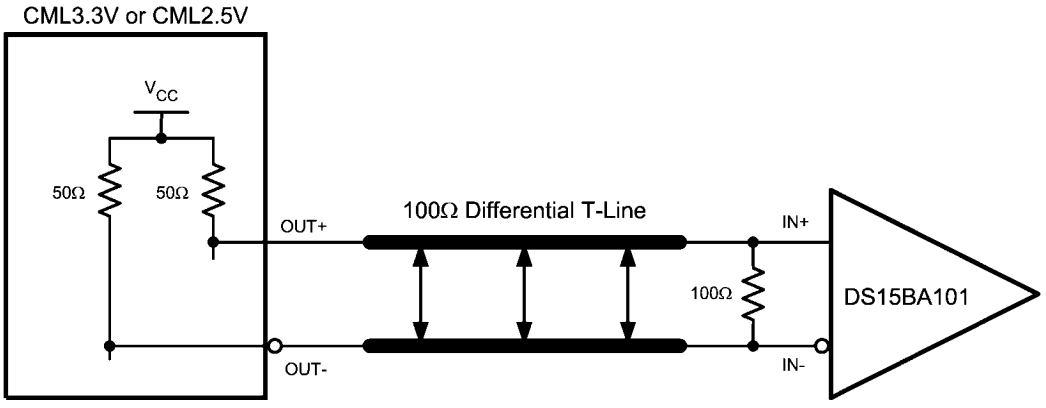
Device Operation

INPUT INTERFACING

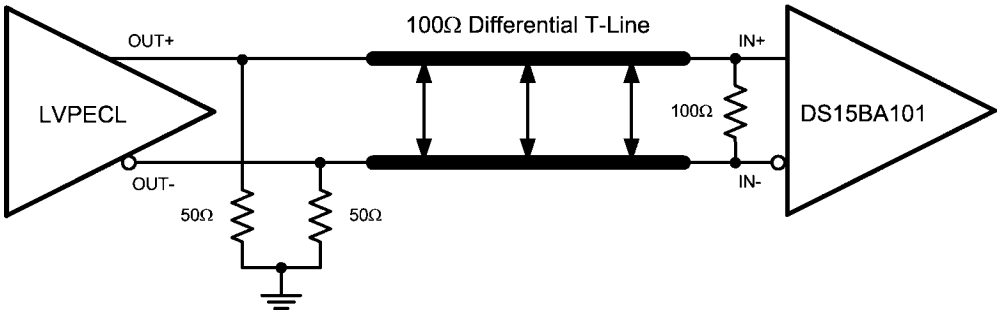
The DS15BA101 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range. The IN+ and IN- pins are self-biased at approximately 2.1V with V_{CC} = 3.3V. The following three figures illustrate typical DC-coupled interface to common differential drivers.



Typical LVDS Driver DC-Coupled Interface to DS15BA101 Input



Typical CML Driver DC-Coupled Interface to DS15BA101 Input

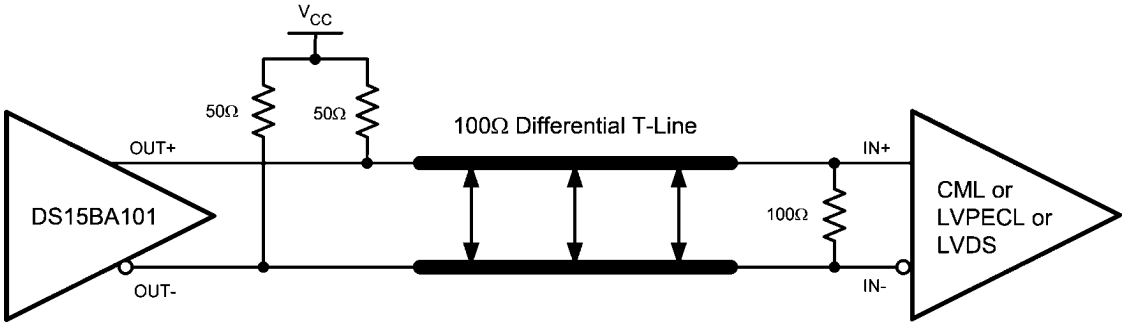


Typical LVPECL Driver DC-Coupled Interface to DS15BA101 Input

OUTPUT INTERFACING

The DS15BA101 uses current mode outputs. Single-ended output levels are 400 mV_{P-P} into AC-coupled 100Ω differential cable (with R_{VO} = 953Ω) or into AC-coupled 50Ω coaxial cable (with R_{VO} = 487Ω). Output level is controlled by the value of the R_{VO} resistor connected between the R_{VO} and V_{CC}.

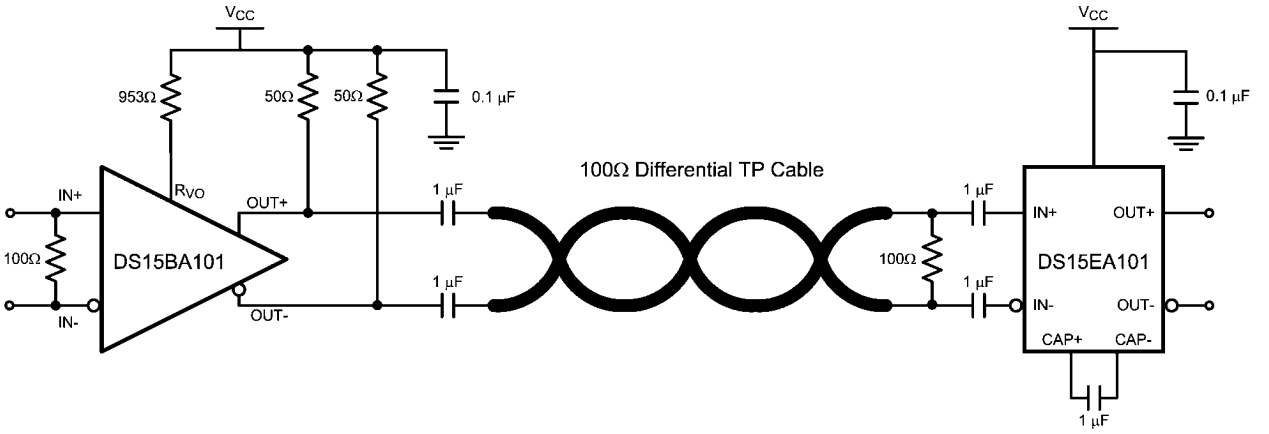
The R_{VO} resistor should be placed as close as possible to the R_{VO} pin. In addition, the copper in the plane layers below the R_{VO} network should be removed to minimize parasitic capacitance. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most receivers have a common mode input range that can accomodate CML signals, it is recommended to check respective receiver's datasheet prior to implementing the suggested interface implementation.



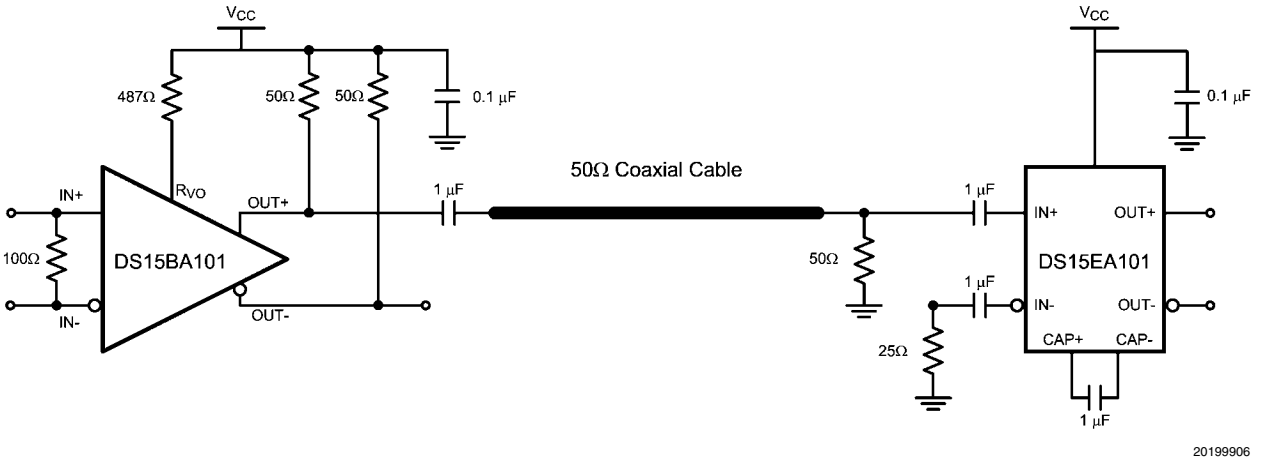
Typical DS15BA101 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

CABLE EXTENDER APPLICATION

The DS15BA101 together with the DS15EA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and field programmable gate arrays (FPGAs) over 100Ω differential (i.e. CAT5e/6/7 and twinax) and 50Ω coaxial cables. Setting correct DS15BA101 output amplitude and proper cable termination are keys for optimal operation. The following two figures show recommended chipset configuration for 100Ω differential and 50Ω coaxial cables.



Cable Extender Chipset Connection Diagram for 100Ω Differential Cables

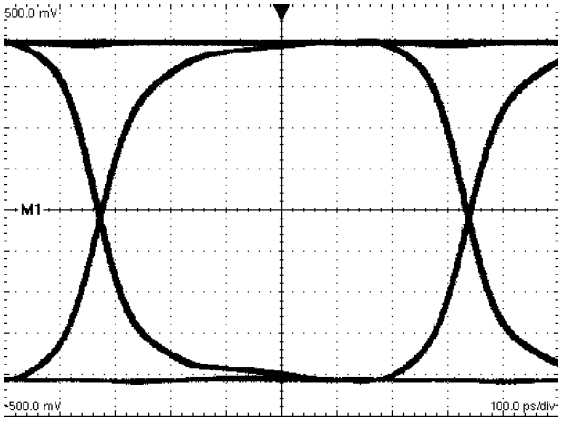


Cable Extender Chipset Connection Diagram for 50Ω Coaxial Cables

REFERENCE DESIGN

There is a complete reference design (P/N: DriveCable02EVK) available for evaluation of the cable extender chipset (DS15BA101 and DS15EA101). Fore more information visit http://www.national.com/appinfo/lvds/drivecable02evk.html.

Typical Performance



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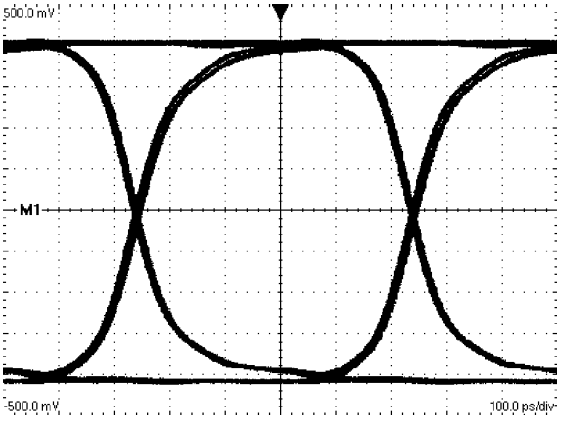
1.5 Gbps Differential DS15BA101 Output
R_{VO} = 953Ω, H:100 ps / DIV, V:100 mV / DIV



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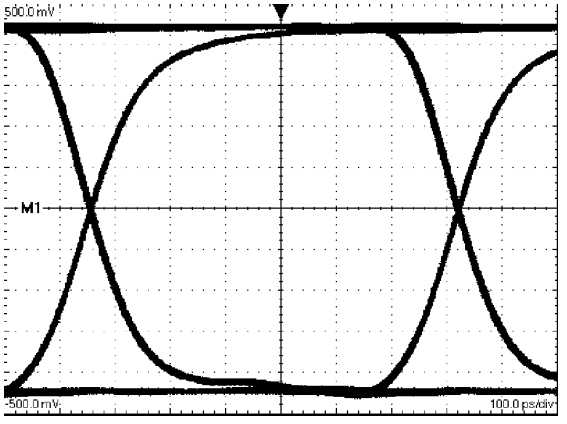
2.0 Gbps Differential DS15BA101 Output
R_{VO} = 953Ω, H:100 ps / DIV, V:100 mV / DIV



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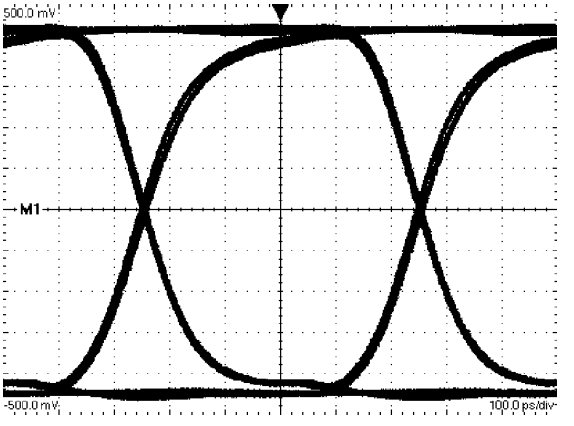
1.5 Gbps Single-ended DS15BA101 Output
R_{VO} = 487Ω, H:100 ps / DIV, V:100 mV / DIV



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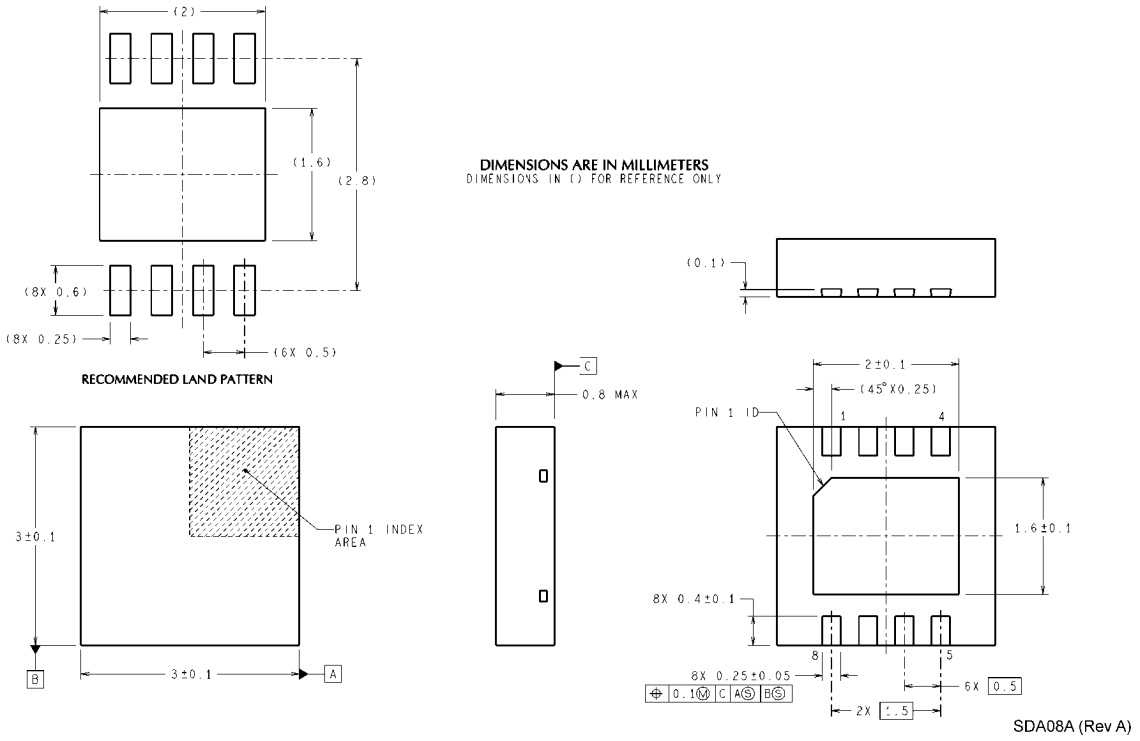
2.0 Gbps Single-ended DS15BA101 Output
R_{VO} = 487Ω, H:100 ps / DIV, V:100 mV / DIV

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pad LLP
Order Number DS15BA101SD or DS15BA101SDX
NS Package Number SDA08A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

Notes

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