DALLAS SEMICONDUCTOR

DS1990A
Serial Number iButton™

www.dalsemi.com

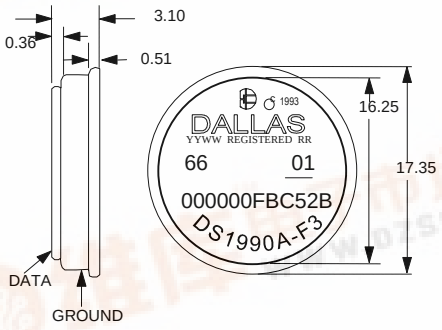
DS1990A SPECIAL FEATURES

- Upgrade of DS1990 allows multiple Serial Number iButtons to reside on a common bus
- Unique 48–bit serial number
- Low-cost electronic key for access control
- 8-bit CRC for checking data integrity
- Can be read in less than 5 ms
- Operating temperature range of -40°C to +85°C

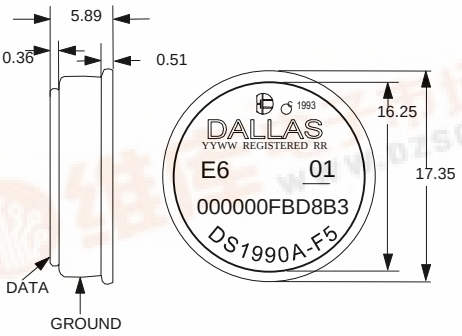
COMMON iButton FEATURES

- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Multidrop controller for MicroLAN
- Digital identification by momentary contact
- Chip-based data carrier compactly stores information
- Data can be accessed while affixed to an object
- Economically communicates to bus master with a single digital signal at 16.3k bits per second
- Standard 16 mm diameter and 1-Wire™ protocol ensure compatibility with iButton family
- Button shape is self-aligning with cup-shaped probes
- Durable stainless steel case engraved with registration number withstands harsh environments
- Easily affixed with self-stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim
- Presence detector acknowledges when reader first applies voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class 1, Division 1, Group A, B, C and D locations

F3 MICROCAN™



F5 MICROCAN™



All dimensions shown in millimeters

ORDERING INFORMATION

DS1990A-F3	F3 MicroCan
DS1990A-F5	F5 MicroCan

EXAMPLES OF ACCESSORIES

DS9096P	Self-Stick Adhesive Pad
DS9101	Multi-Purpose Clip
DS9093RA	Mounting Lock Ring
DS9093F	Snap-In Fob
DS9092	iButton Probe

iButton DESCRIPTION

The DS1990A Serial Number iButton is a rugged data carrier that acts as an electronic registration number for automatic identification. The DS1990A consists of a factory-lasered, 64-bit ROM that includes an unique 48-bit serial number, an 8-bit CRC and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol which requires only a single data lead and a ground return. The DS1990A is fully compatible with the DS1990 Serial Number iButton but provides the additional 1-Wire protocol capability that allows the Search ROM command to be interpreted by the DS1990A and therefore allows multiple DS1990A devices to reside on a single data line.

The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture and shock. Its compact coin-shaped profile is self-aligning with mating receptacles, allowing the DS1990A to be used easily by human operators. Accessories permit the DS1990A to be mounted on plastic key tabs, photo ID badges, printed circuit boards or any smooth surface of an object. Applications include access control, work-in-progress tracking, tool management and inventory control.

OPERATION

The DS1990A's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the Dallas 1-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the DS1990A is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal type and timing). For a more detailed protocol description, refer to Chapter 4 of the Book of DS19xx iButton Standards.

Hardware Configuration

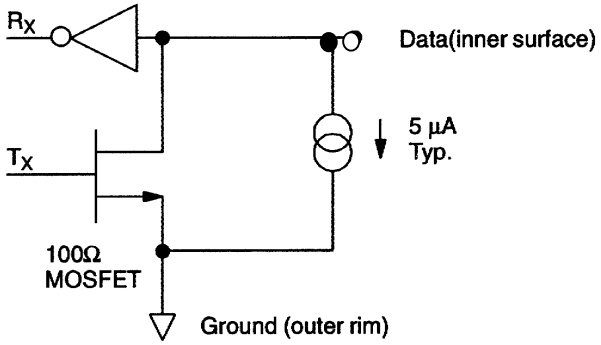
The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have an open drain connection or 3-state outputs. The DS1990A is an open drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3. The value of the pullup resistor should be approximately 5 kΩ for short line lengths. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3k bits per second.

The idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120 µs, one or more of the devices on the bus may be reset.

DS1990A MEMORY MAP Figure 1

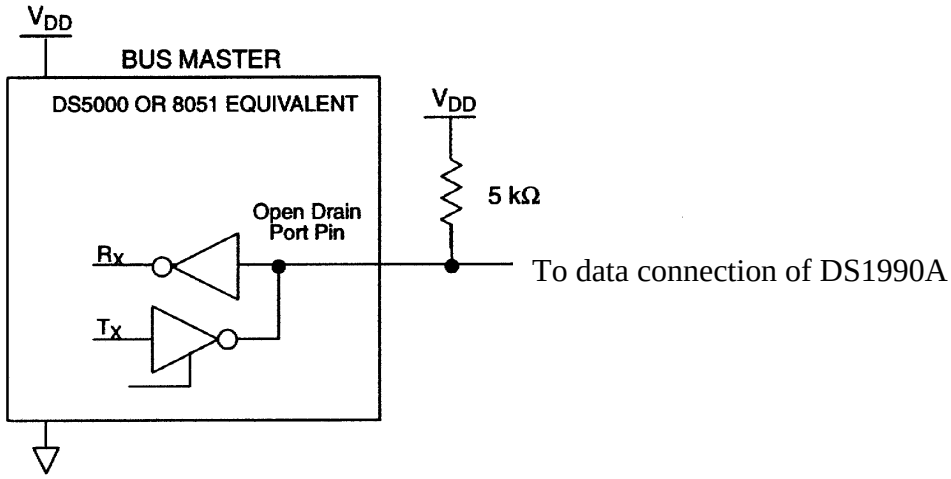
8-Bit CRC Code		48-Bit Serial Number		8-Bit Family Code (01h)	
MSB	LSB	MSB	LSB	MSB	LSB

DS1990A EQUIVALENT CIRCUIT Figure 2

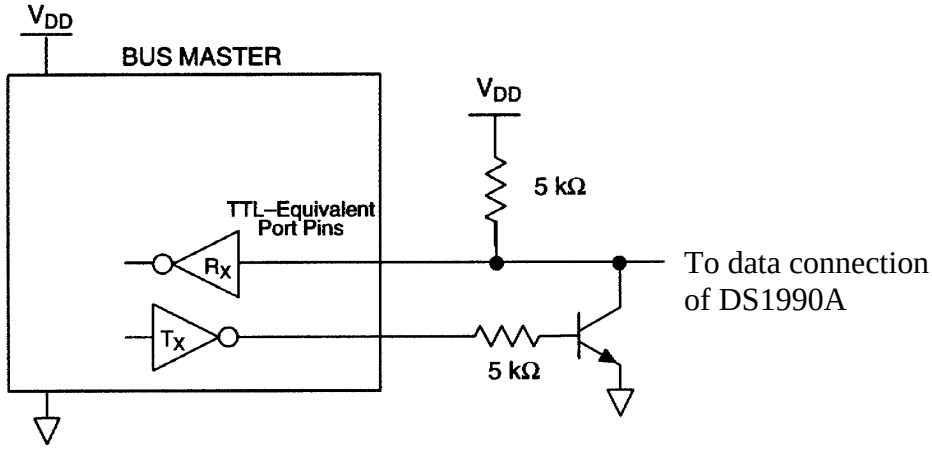


BUS MASTER CIRCUIT Figure 3

A) Open Drain



B) Standard TTL



TRANSACTION SEQUENCE

The sequence for accessing the DS1990A via the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Read Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a presence pulse(s) transmitted by the slave(s).

The presence pulse lets the bus master know that the DS1990A is on the bus and is ready to operate. For more details, see the "1-Wire Signaling" section.

ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are eight bits long. A list of these commands follows (refer to flowchart in Figure 4):

Read ROM [33h] or [0Fh]

This command allows the bus master to read the DS1990A's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1990A on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The DS1990A Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the DS1990, which will only respond to a 0Fh command word with its 64-bit ROM data.

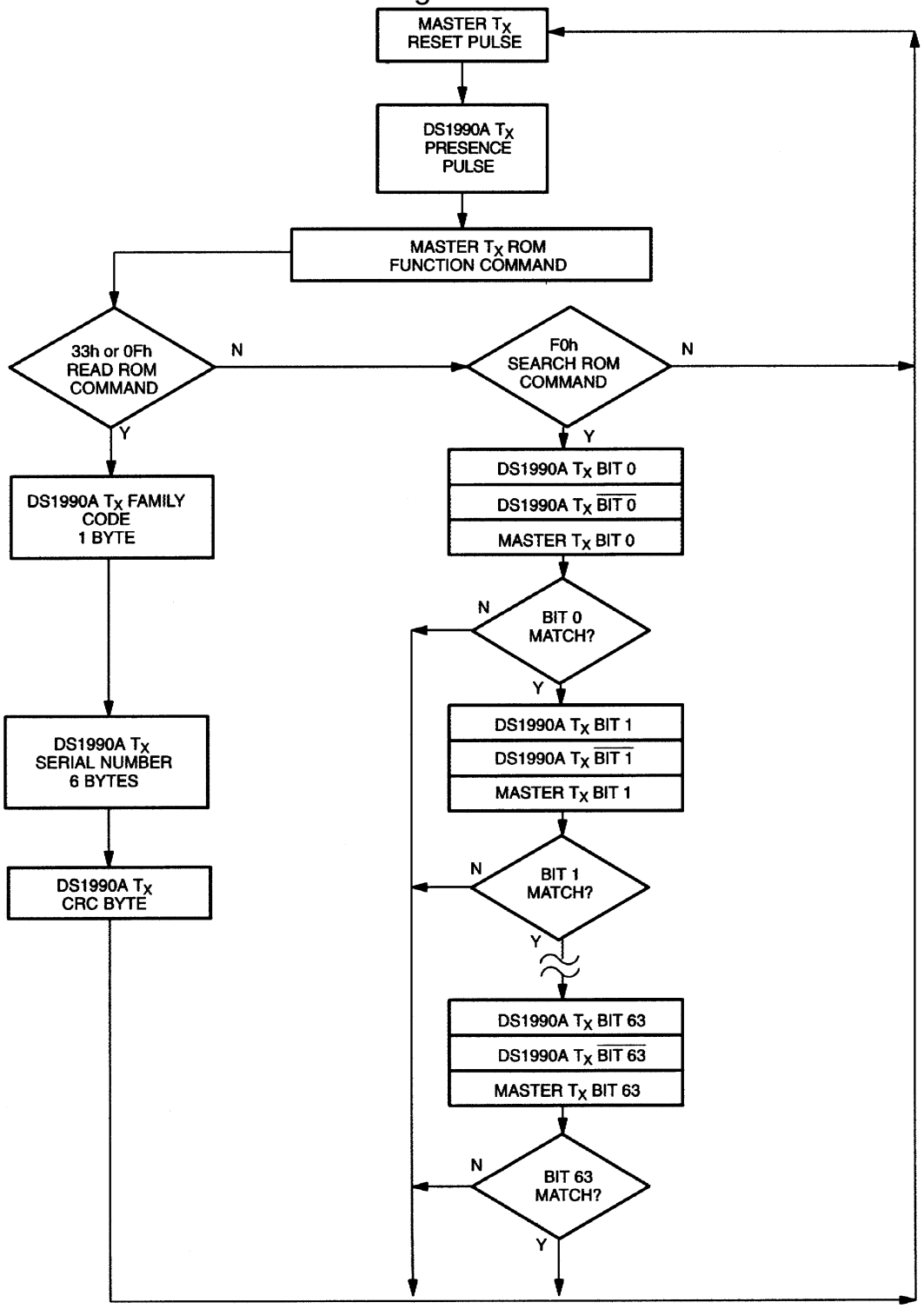
Match ROM [55h] / Skip ROM [CCh]

The complete 1-Wire protocol for all Dallas Semiconductor iButtons contains a Match ROM and a Skip ROM command. (See the Book of DS19xx iButton Standards.) Since the DS1990A contains only the 64-bit ROM with no additional data fields, the Match ROM and Skip ROM are not applicable and will cause no further activity on the 1-Wire bus if executed. The DS1990A does not interfere with other 1-Wire parts on a multidrop bus that do respond to a Match ROM or Skip ROM (example DS1990A and DS1994 on the same bus).

Search ROM [F0h]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The remaining number of devices and their ROM codes may be identified by additional passes. See Chapter 5 of the Book of DS19xx iButton Standards for a comprehensive discussion of a ROM search, including an actual example.

ROM FUNCTIONS FLOW CHART Figure 4



1-WIRE SIGNALING

The DS1990A requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: Reset sequence with Reset Pulse and Presence Pulse, write 0, write 1 and read data. All these signals except presence pulse are initiated by the bus master.

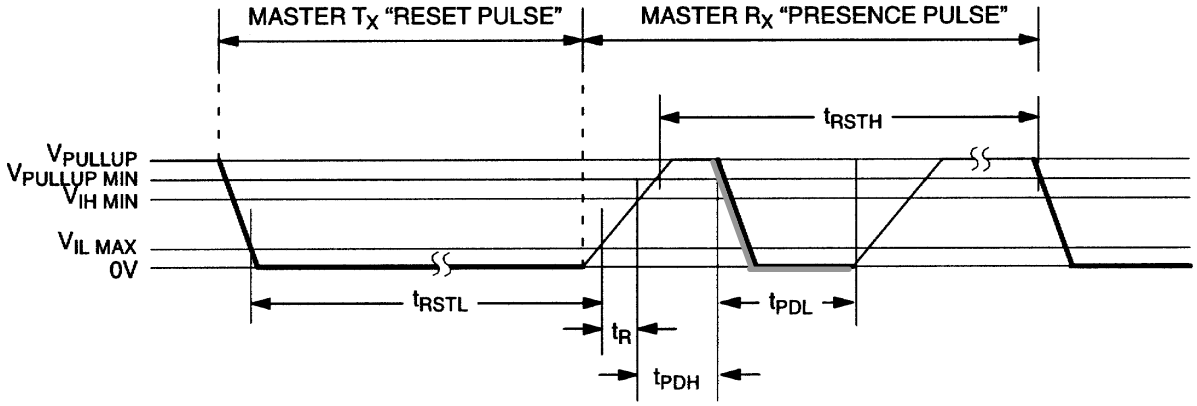
The initialization sequence required to begin any communication with the DS1990A is shown in Figure 5. A Reset Pulse followed by a Presence Pulse indicates the DS1990A is ready to send or receive data given the correct ROM command.

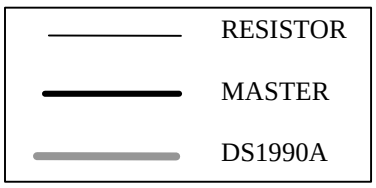
The bus master transmits (T_X) a reset pulse (a low signal for a minimum of 480 µs). The bus master then releases the line and goes into receive mode (R_X). The 1-Wire bus is pulled to a high state via the 5 kΩ pullup resistor. After detecting the rising edge on the data contact, the DS1990A waits (t_{PDH} , 15-60 µs) and then transmits the presence pulse (t_{PDL} , 60-240 µs).

READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the DS1990A to the master by triggering a delay circuit in the DS1990A. During write time slots, the delay circuit determines when the DS1990A will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the DS1990A will hold the data line low overriding the 1 generated by the master. If the data bit is a "1", the iButton will leave the read data time slot unchanged.

INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5



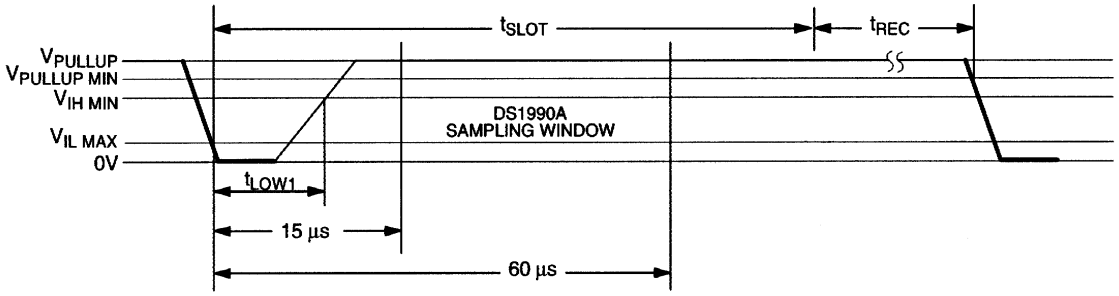


480 µs ≤ t_{RSTL} < ∞ *
480 µs ≤ t_{RSTH} < ∞ (includes recovery time)
15 µs ≤ t_{PDH} < 60 µs
60 µs ≤ t_{PDL} < 240 µs

* In order not to mask interrupt signaling by other devices on the 1-Wire bus, t_{RSTL} + t_R should always be less than 960 µs.

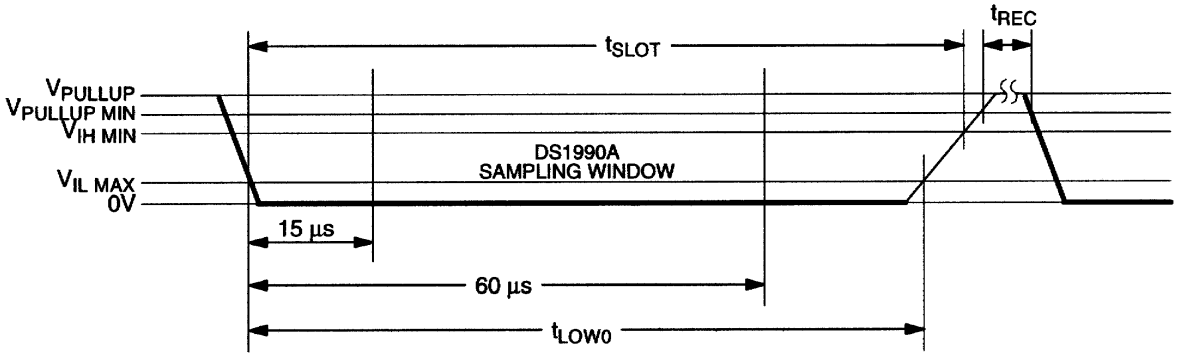
READ/WRITE TIMING DIAGRAM Figure 6

Write-One Time Slot



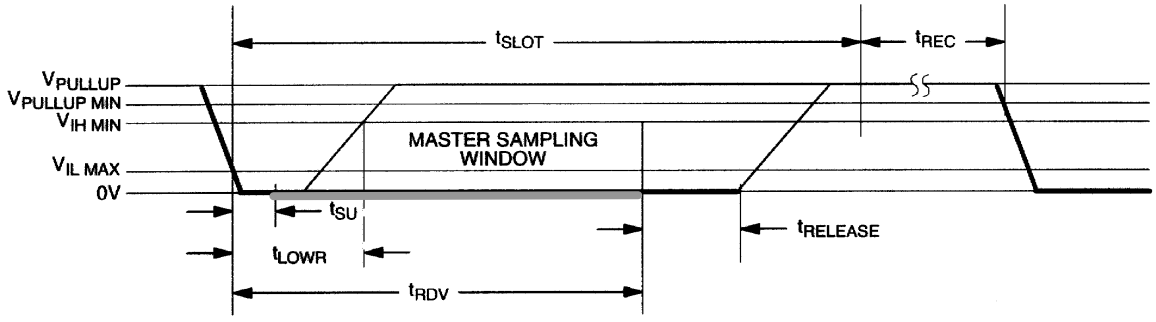
$60\ \mu s \le t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{LOW1} < 15\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

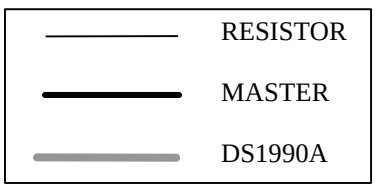
Write-Zero Time Slot



$60\ \mu s \le t_{LOW0} < t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{REC} < \infty$

Read-Data Time Slot





$60\ \mu s \le t_{SLOT} < 120\ \mu s$
$1\ \mu s \le t_{LOWR} < 15\ \mu s$
$0 \le t_{RELEASE} < 45\ \mu s$
$1\ \mu s \le t_{REC} < \infty$
$t_{RDV} = 15\ \mu s$
$t_{SU} = 1\ \mu s$

CRC ASSEMBLY LANGUAGE PROCEDURE Table 1

```
DO_CRC:     PUSH    ACC         ; save the accumulator
            PUSH    B           ; save the B register
            PUSH    ACC         ; save bits to be shifted
            MOV     B,#8         set shift=8bits
                                ;
CRC_LOOP:   XRL     A,CRC       ; calculate CRC
            RRC     A           ; move it to the carry
            MOV     A,CRC       ; get the last CRC value
            JNC     ZERO        ; skip if data=0
            XRL     A,#18H      ; update the CRC value
                                ;
ZERO:       RRC     A           ; position the new CRC
            MOV     CRC,A       ; store the new CRC
            POP     ACC         ; get the remaining bits
            RR      A           ; position the next bit
            PUSH    ACC         ; save the remaining bits
            DJNZ    B,CRC_LOOP  ; repeat for eight bits
            POP     ACC         ; clean up the stack
            POP     B           ; restore the B register
            POP     ACC         ; restore the accumulator
            RET
```

CRC GENERATION

To validate the data transmitted from the DS1990A, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1990A. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but *not* over the stored CRC value itself. If the two CRC values match, the transmission is error-free.

An example of how to generate the CRC using assembly language software is shown in Table 1. This assembly language code is written for the DS5000 Soft microcontroller which is compatible with the 8031/51 Microcontroller family. The procedure DO_CRC calculates the cumulative CRC of all the bytes passed to it in the accumulator. It should be noted that the variable CRC needs to be initialized to 0 before the procedure is executed. Each byte of the data is then placed in the accumulator and DO-CRC is called to update the CRC variable. After all the data has been passed to DO_CRC, the variable CRC will contain the result. The equivalent polynomial function of this software routine is:

$$CRC = x^8 + x^5 + x^4 + 1$$

For more details, see the Book of DS19xx iButton Standards.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		V_{CC} +0.3	V	1,6
Logic 0	V_{OL}	-0.3		+0.8	V	1
Output Logic Low @ 4 mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}		V_{PUP}	6.0	V	1,2
Input Load Current	I_L		5		µA	3
Operating Charge	Q_{OP}			30	nC	7,8

CAPACITANCE (TA = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
I/O (1-Wire)	$C_{IN/OUT}$		100	800	pF	9

AC ELECTRICAL CHARACTERISTICS (V_{PUP}=2.8V to 6.0V; -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Data Valid	t_{RDV}	exactly 15			µs	
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	5
Recovery Time	t_{REC}	1			µs	
Reset Time High	t_{RSTH}	480			µs	4
Reset Time Low	t_{RSTL}	480			µs	10
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.

2. V_{PUP} = external pullup voltage.

3. Input load is to ground.

4. An additional reset or communication sequence cannot begin until the reset high time has expired.

5. Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1 µs of this falling edge and will remain valid for 14 µs minimum. (15 µs total from falling edge on 1-Wire bus.)

6. V_{IH} is a function of the external pullup resistor and the V_{CC} supply.

7. 30 nanocoulombs per 72 time slots @ 5.0V.

8. At V_{CC} =5.0V with a 5 kΩ pullup to V_{CC} and a maximum time slot of 120 µs.

9. Capacitance on the I/O pin could be 800 pF when power is first applied. If a 5 kΩ resistor is used to pull up the I/O line to V_{CC}, 5 µs after power has been applied the parasite capacitance will not affect normal communications.

10. The reset low time (t_{RSTL}) should be restricted to a maximum of 960 µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses if this device is used in parallel with a DS1994.