



November 6, 2007

## DS25BR110

### 3.125 Gbps LVDS Buffer with Receive Equalization

#### General Description

The DS25BR110 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. A fully differential signal path ensures exceptional signal integrity and noise immunity.

The DS25BR110 features four levels of receive equalization (EQ), making it ideal for use as a receiver device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

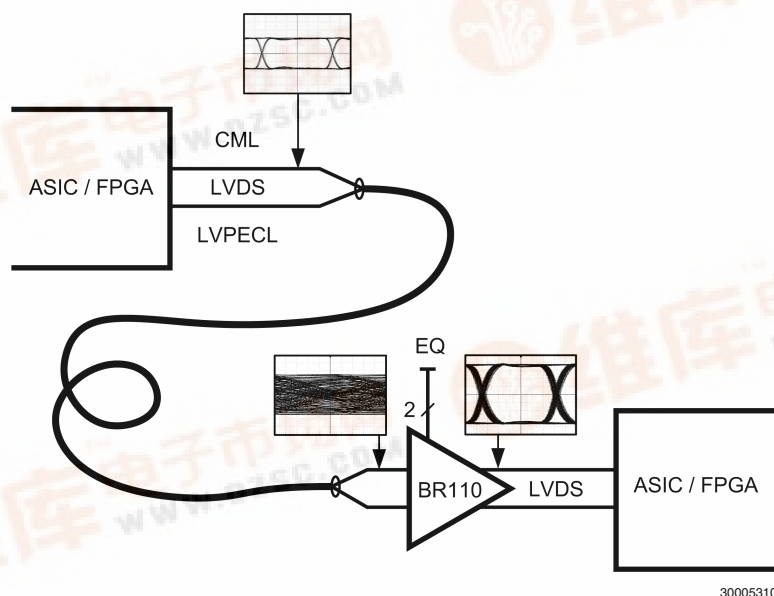
#### Features

- DC - 3.125 Gbps low jitter, high noise immunity, low power operation
- Four levels of receive equalization reduce ISI jitter
- On-chip 100Ω input and output termination minimizes insertion and return losses, reduces component count and minimizes board space
- 7 kV ESD on LVDS I/O pins protects adjoining components
- Small 3 mm x 3 mm 8-LLP space saving package

#### Applications

- Clock and data buffering
- Metallic cable equalization
- FR-4 equalization

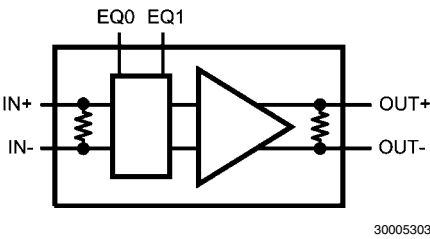
#### Typical Application



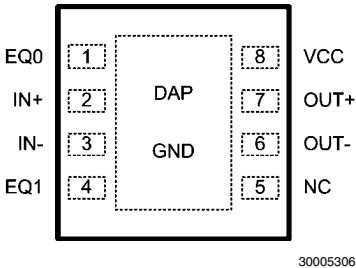
30005310



Block Diagram



Pin Diagram



Pin Descriptions

Pin Name	Pin Name	Pin Type	Pin Description
EQ0	1	Input	Equalizer select pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
EQ1	4	Input	Equalizer select pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

Control Pins (EQ0 and EQ1) Truth Tables

EQ1	EQ0	Equalization Level
0	0	Off
0	1	Low (Approx. 4 dB at 1.56 GHz)
1	0	Medium (Approx. 8 dB at 1.56 GHz)
1	1	High (Approx. 16 dB at 1.56 GHz)

Ordering Codes and Configurations

NSID	Function	Available Equalization Levels	Available Pre-emphasis Levels
DS25BR100TSD	Buffer/Repeater	Low / Medium	Off / Medium
DS25BR110TSD	Receiver	Off / Low / Medium / High	NA
DS25BR120TSD	Driver	NA	Off / Low / Medium / High
DS25BR150TSD	Buffer/Repeater	NA	NA

## Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.3V to +4V
LVC MOS Input Voltage (EQ0, EQ1)	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Input Voltage (IN+, IN-)	-0.3V to +4V
LVDS Differential Input Voltage ((IN+) - (IN-))	0V to 1.0V
LVDS Output Voltage (OUT+, OUT-)	-0.3V to ( $V_{CC} + 0.3V$ )
LVDS Differential Output Voltage ((OUT+) - (OUT-))	0V to 1.0V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SDA Package	2.08W
Derate SDA Package	16.7 mW/°C above +25°C

## Package Thermal Resistance

$\theta_{JA}$	+60.0°C/W
$\theta_{JC}$	+12.3°C/W

## ESD Susceptibility

HBM (Note 1)	≥7 kV
MM (Note 2)	≥250V
CDM (Note 3)	≥1250V

**Note 1:** Human Body Model, applicable std. JESD22-A114C

**Note 2:** Machine Model, applicable std. JESD22-A115-A

**Note 3:** Field Induced Charge Device Model, applicable std. JESD22-C101-C

## Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Receiver Differential Input Voltage ( $V_{ID}$ )			1.0	V
Operating Free Air Temperature ( $T_A$ )	-40	+25	+85	°C

## DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVCMOS INPUT DC SPECIFICATIONS (EQ0, EQ1)</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$I_{IH}$	High Level Input Current	$V_{IN} = 3.6V$ $V_{CC} = 3.6V$		0	±10	µA
$I_{IL}$	Low Level Input Current	$V_{IN} = GND$ $V_{CC} = 3.6V$		0	±10	µA
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18 \text{ mA}$ , $V_{CC} = 0V$		-0.9	-1.5	V
<b>LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)</b>						
$V_{OD}$	Differential Output Voltage	$R_L = 100\Omega$	250	350	450	mV
$\Delta V_{OD}$	Change in Magnitude of $V_{OD}$ for Complimentary Output States		-35		35	mV
$V_{OS}$	Offset Voltage	$R_L = 100\Omega$	1.05	1.2	1.375	V
$\Delta V_{OS}$	Change in Magnitude of $V_{OS}$ for Complimentary Output States		-35		35	mV
$I_{OS}$	Output Short Circuit Current (Note 8)	OUT to GND		-35	-55	mA
		OUT to $V_{CC}$		7	55	mA
$C_{OUT}$	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
$R_{OUT}$	Output Termination Resistor	Between OUT+ and OUT-		100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LVDS INPUT DC SPECIFICATIONS (IN+, IN-)</b>						
$V_{ID}$	Input Differential Voltage	$V_{CM} = +0.05V$ or $V_{CC} - 0.05V$	0		1	V
$V_{TH}$	Differential Input High Threshold			0	+100	mV
$V_{TL}$	Differential Input Low Threshold		-100	0		mV
$V_{CMR}$	Common Mode Voltage Range	$V_{ID} = 100$ mV	0.05		$V_{CC} - 0.05$	V
$I_{IN}$	Input Current	$V_{IN} = 3.6V$ or $0V$ $V_{CC} = 3.6V$ or $0V$		$\pm 1$	$\pm 10$	$\mu A$
$C_{IN}$	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
$R_{IN}$	Input Termination Resistor	Between IN+ and IN-		100		$\Omega$
<b>SUPPLY CURRENT</b>						
$I_{CC}$	Supply Current	EQ0 = 0, EQ1 = 0		35	43	mA

**Note 4:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

**Note 5:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 6:** Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except  $V_{OD}$  and  $\Delta V_{OD}$ .

**Note 7:** Typical values represent most likely parametric norms for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 8:** Output short circuit current ( $I_{OS}$ ) is specified as magnitude only, minus sign indicates direction only.

**AC Electrical Characteristics** (Note 11)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 9, 10)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t <sub>PHLD</sub>	Differential Propagation Delay High to Low	R <sub>L</sub> = 100Ω		350	465	ps	
t <sub>PLHD</sub>	Differential Propagation Delay Low to High			350	465	ps	
t <sub>SKD1</sub>	Pulse Skew  t <sub>PLHD</sub> – t <sub>PHLD</sub>   (Note 12)			45	100	ps	
t <sub>SKD2</sub>	Part to Part Skew (Note 13)			45	150	ps	
t <sub>LHT</sub>	Rise Time	R <sub>L</sub> = 100Ω		80	150	ps	
t <sub>HLT</sub>	Fall Time			80	150	ps	
JITTER PERFORMANCE WITH EQ = OFF							
t <sub>RJ1A</sub>	Random Jitter (RMS Value) No Test Channels (Note 14)	V <sub>ID</sub> = 350 mV V <sub>CM</sub> = 1.2V Clock (RZ) EQ0 = 0, EQ1 = 0	2.5 Gbps		0.5	1	ps
t <sub>RJ2A</sub>				3.125 Gbps		0.5	1
t <sub>DJ1A</sub>	Deterministic Jitter (Peak to Peak) No Test Channels (Note 15)	V <sub>ID</sub> = 350 mV V <sub>CM</sub> = 1.2V K28.5 (NRZ) EQ0 = 0, EQ1 = 0	2.5 Gbps		11	40	ps
t <sub>DJ2A</sub>				3.125 Gbps		11	47
t <sub>TJ1A</sub>	Total Jitter (Peak to Peak) No Test Channels (Note 16)	V <sub>ID</sub> = 350 mV V <sub>CM</sub> = 1.2V PRBS-23 (NRZ) EQ0 = 0, EQ1 = 0	2.5 Gbps		0.05	0.16	UI <sub>P-P</sub>
t <sub>TJ2A</sub>				3.125 Gbps		0.08	0.20

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
JITTER PERFORMANCE WITH EQ = LOW (Figures 5 and 6 )							
t <sub>RJ1B</sub>	Random Jitter (RMS Value) Test Channel D (Note 14)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.5	1	ps
t <sub>RJ2B</sub>		V <sub>CM</sub> = 1.2V Clock (RZ) EQ0 = 1, EQ1 = 0	3.125 Gbps		0.5	1	ps
t <sub>DJ1B</sub>	Deterministic Jitter (Peak to Peak) Test Channel D (Note 15)	V <sub>ID</sub> = 350 mV	2.5 Gbps		1	16	ps
t <sub>DJ2B</sub>		V <sub>CM</sub> = 1.2V K28.5 (NRZ) EQ0 = 1, EQ1 = 0	3.125 Gbps		11	31	ps
t <sub>TJ1B</sub>	Total Jitter (Peak to Peak) Test Channel D (Note 16)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.03	0.09	UI <sub>P-P</sub>
t <sub>TJ2B</sub>		V <sub>CM</sub> = 1.2V PRBS-23 (NRZ) EQ0 = 1, EQ1 = 0	3.125 Gbps		0.06	0.14	UI <sub>P-P</sub>
JITTER PERFORMANCE WITH EQ = MEDIUM (Figures 5 and 6 )							
t <sub>RJ1C</sub>	Random Jitter (RMS Value) Test Channel E (Note 14)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.5	1	ps
t <sub>RJ2C</sub>		V <sub>CM</sub> = 1.2V Clock (RZ) EQ0 = 0, EQ1 = 1	3.125 Gbps		0.5	1	ps
t <sub>DJ1C</sub>	Deterministic Jitter (Peak to Peak) Test Channel E (Note 15)	V <sub>ID</sub> = 350 mV	2.5 Gbps		10	29	ps
t <sub>DJ2C</sub>		V <sub>CM</sub> = 1.2V K28.5 (NRZ) EQ0 = 0, EQ1 = 1	3.125 Gbps		27	43	ps
t <sub>TJ1C</sub>	Total Jitter (Peak to Peak) Test Channel E (Note 16)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.07	0.12	UI <sub>P-P</sub>
t <sub>TJ2C</sub>		V <sub>CM</sub> = 1.2V PRBS-23 (NRZ) EQ0 = 0, EQ1 = 1	3.125 Gbps		0.12	0.17	UI <sub>P-P</sub>
JITTER PERFORMANCE WITH EQ = HIGH (Figures 5 and 6)							
t <sub>RJ1D</sub>	Random Jitter (RMS Value) Test Channel F (Note 14)	V <sub>ID</sub> = 350 mV	2.5 Gbps		1.6	2.1	ps
t <sub>RJ2D</sub>		V <sub>CM</sub> = 1.2V Clock (RZ) EQ0 = 1, EQ1 = 1	3.125 Gbps		1.7	2.3	ps
t <sub>DJ1D</sub>	Deterministic Jitter (Peak to Peak) Test Channel F (Note 15)	V <sub>ID</sub> = 350 mV	2.5 Gbps		30	45	ps
t <sub>DJ2D</sub>		V <sub>CM</sub> = 1.2V K28.5 (NRZ) EQ0 = 1, EQ1 = 1	3.125 Gbps		43	59	ps
t <sub>TJ1D</sub>	Total Jitter (Peak to Peak) Test Channel F (Note 16)	V <sub>ID</sub> = 350 mV	2.5 Gbps		0.14	0.27	UI <sub>P-P</sub>
t <sub>TJ2D</sub>		V <sub>CM</sub> = 1.2V PRBS-23 (NRZ) EQ0 = 1, EQ1 = 1	3.125 Gbps		0.19	0.28	UI <sub>P-P</sub>

**Note 9:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 10:** Typical values represent most likely parametric norms for  $V_{CC} = +3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 11:** Specification is guaranteed by characterization and is not tested in production.

**Note 12:**  $t_{SKD1}$ ,  $t_{PLHD} - t_{PHLD}$ , is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

**Note 13:**  $t_{SKD2}$ , Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same  $V_{CC}$  and within  $5^\circ\text{C}$  of each other within the operating temperature range.

**Note 14:** Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

**Note 15:** Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

**Note 16:** Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

## DC Test Circuits

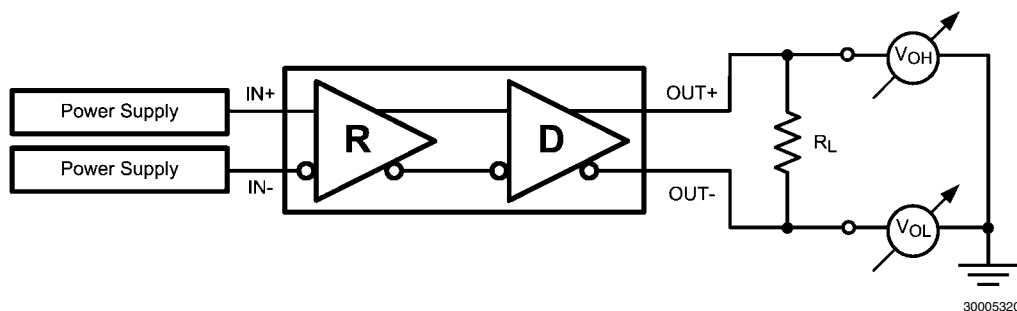


FIGURE 1. Differential Driver DC Test Circuit

## AC Test Circuits and Timing Diagrams

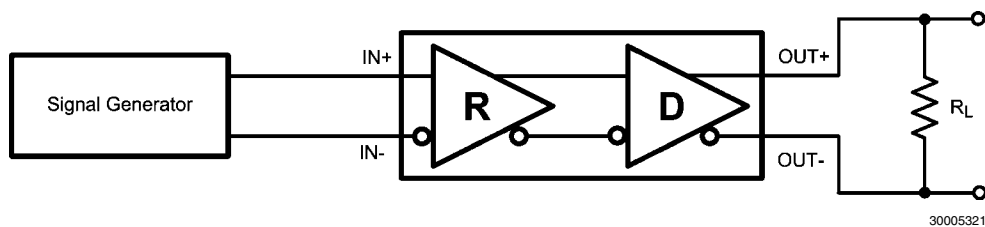


FIGURE 2. Differential Driver AC Test Circuit

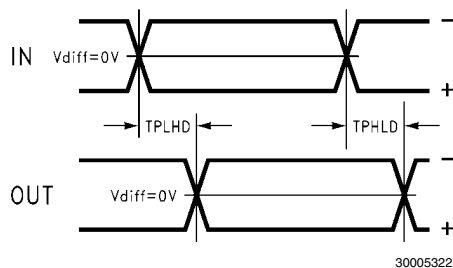


FIGURE 3. Propagation Delay Timing Diagram

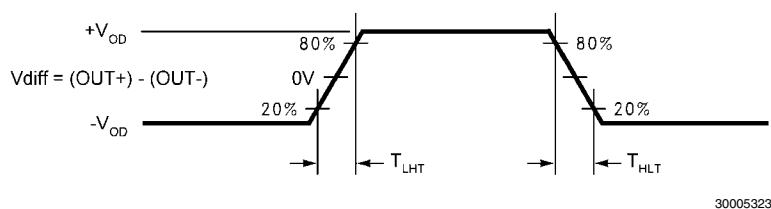
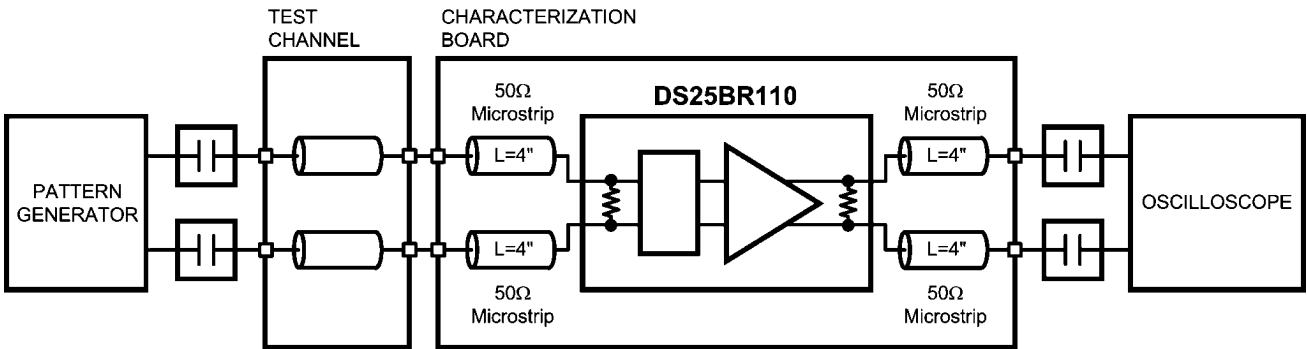


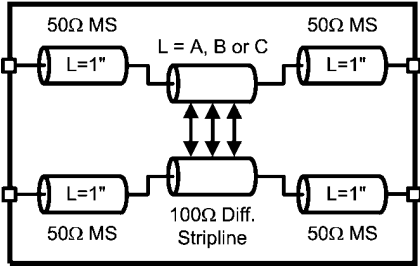
FIGURE 4. LVDS Output Transition Times

## Equalization Test Circuits



30005326

FIGURE 5. Equalization Performance Test Circuit



30005328

FIGURE 6. Test Channel Description

## Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

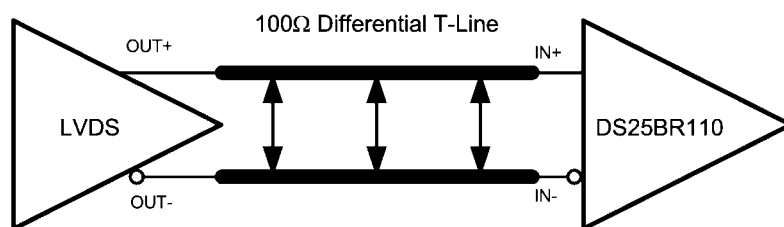
Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0



## Device Operation

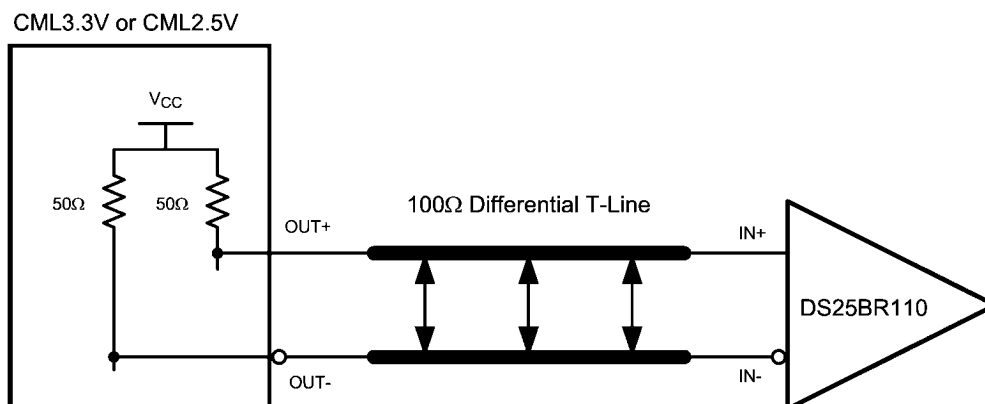
### INPUT INTERFACING

The DS25BR110 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR110 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR110 inputs are internally terminated with a 100Ω resistor.



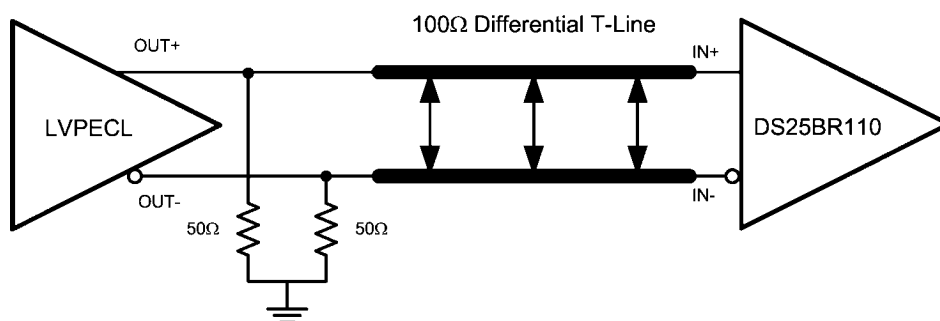
Typical LVDS Driver DC-Coupled Interface to DS25BR110 Input

30005311



Typical CML Driver DC-Coupled Interface to DS25BR110 Input

30005312

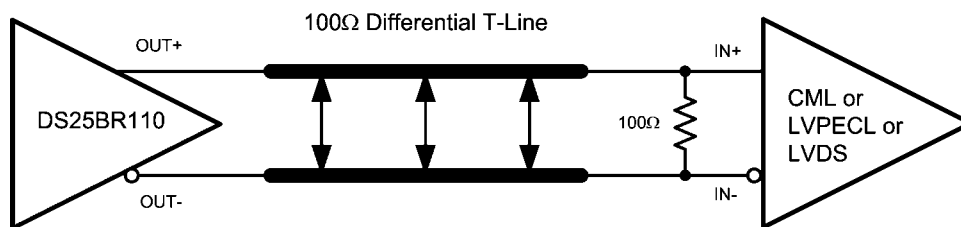


Typical LVPECL Driver DC-Coupled Interface to DS25BR110 Input

30005313

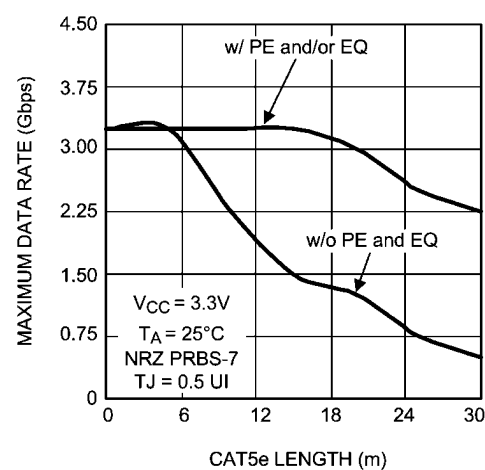
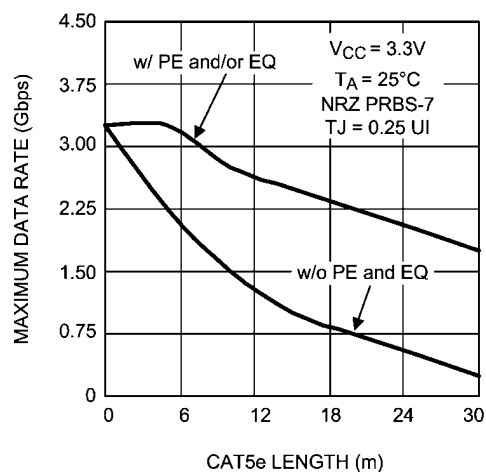
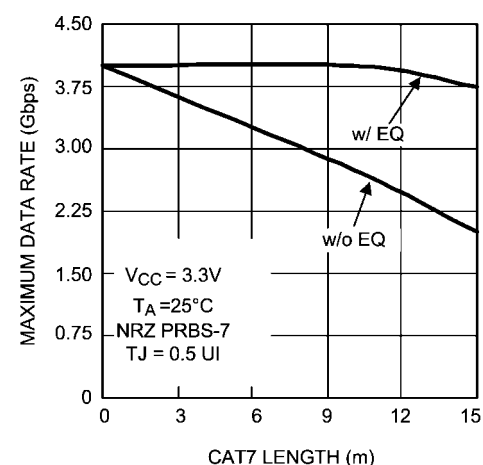
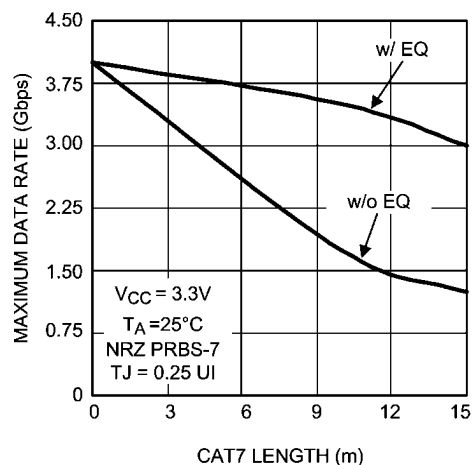
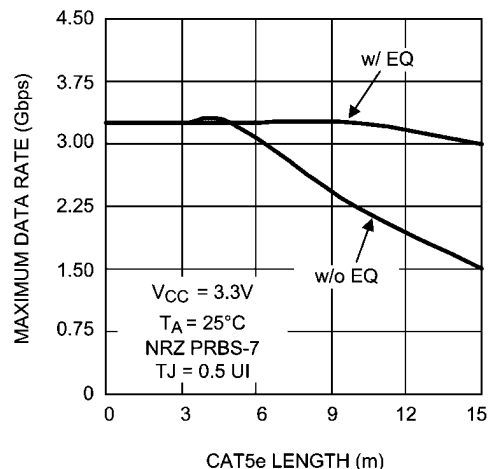
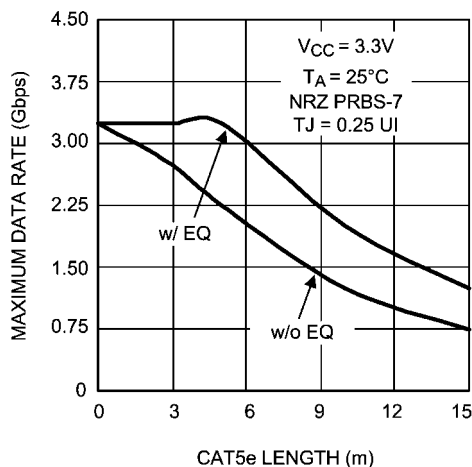
## OUTPUT INTERFACING

The DS25BR110 outputs signals compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



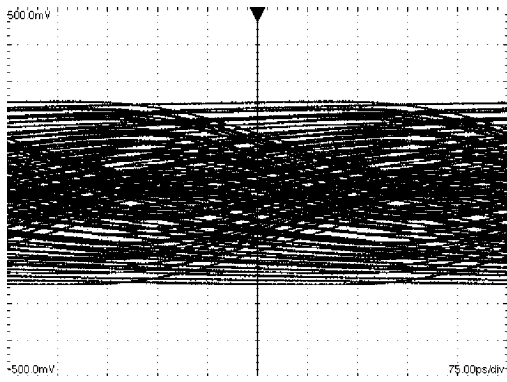
Typical DS25BR110 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver 30005314

## Typical Performance

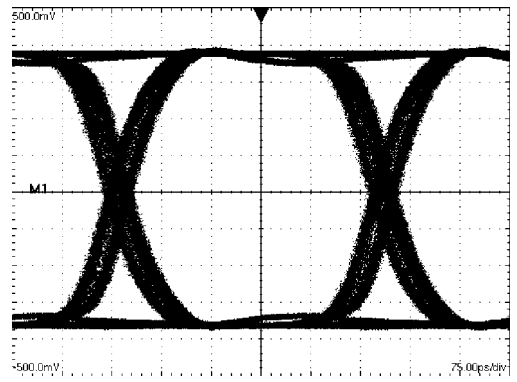


Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length  
DS25BR120 Used as a Driver  
DS25BR110 Used as a Receiver

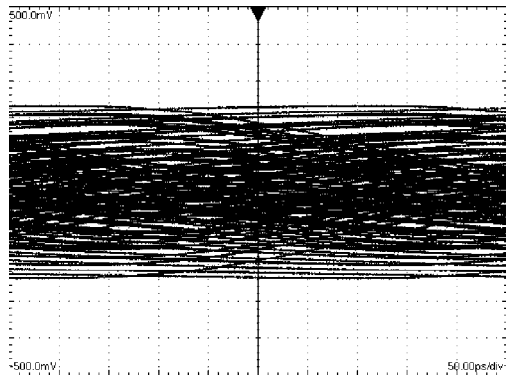
Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length  
DS25BR120 Used as a Driver  
DS25BR110 Used as a Receiver



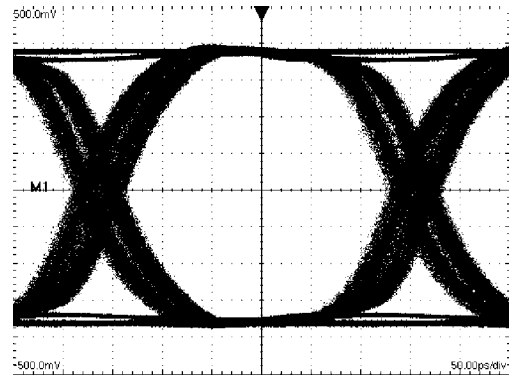
**A 2.5 Gbps NRZ PRBS-7 After 70"**  
Differential FR-4 Stripline  
V:100 mV / DIV, H:75 ps / DIV



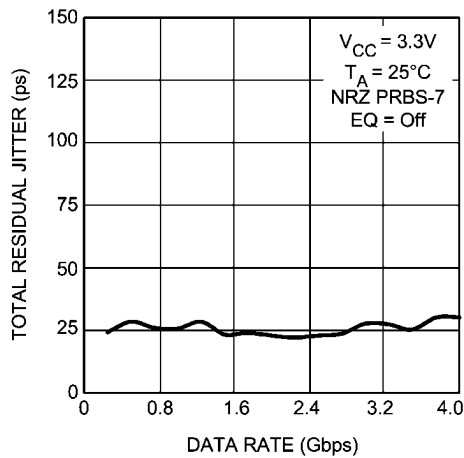
**An Equalized 2.5 Gbps NRZ PRBS-7 After 70"**  
Differential FR-4 Stripline  
V:100 mV / DIV, H:75 ps / DIV



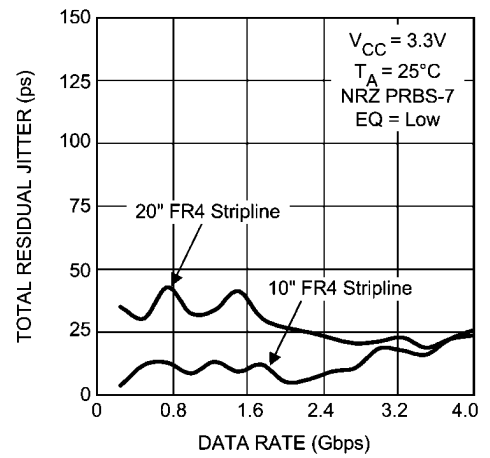
**A 3.125 Gbps NRZ PRBS-7 After 70"**  
Differential FR-4 Stripline  
V:100 mV / DIV, H:50 ps / DIV



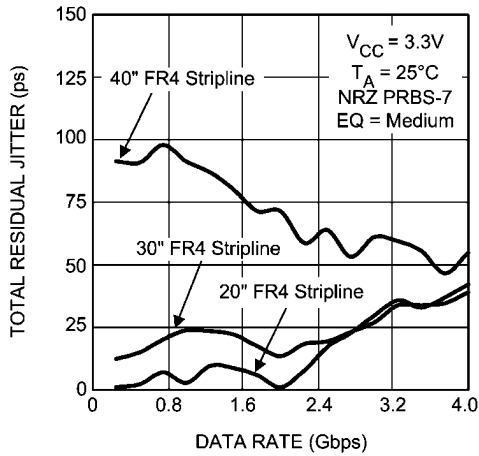
**An Equalized 3.125 Gbps NRZ PRBS-7 After 70"**  
Differential FR-4 Stripline  
V:100 mV / DIV, H:50 ps / DIV



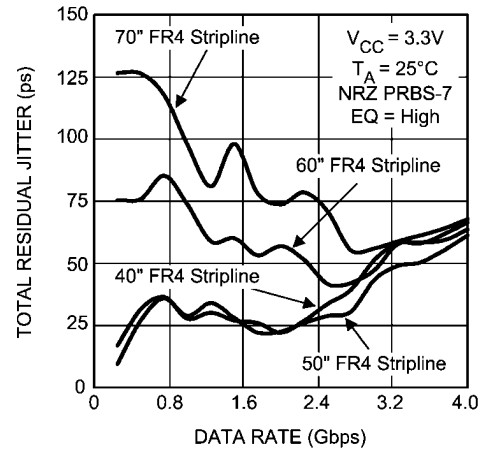
**Total Jitter as a Function of Data Rate**



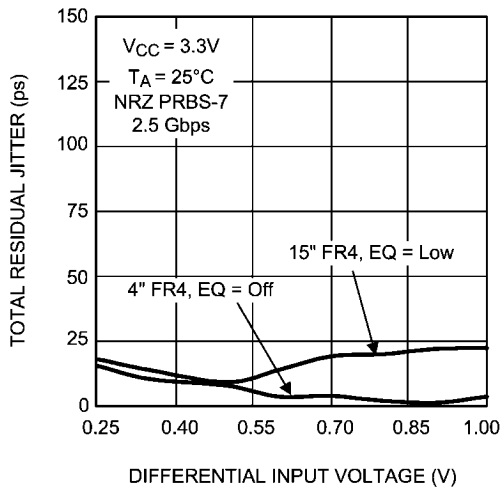
**Total Jitter as a Function of Data Rate**



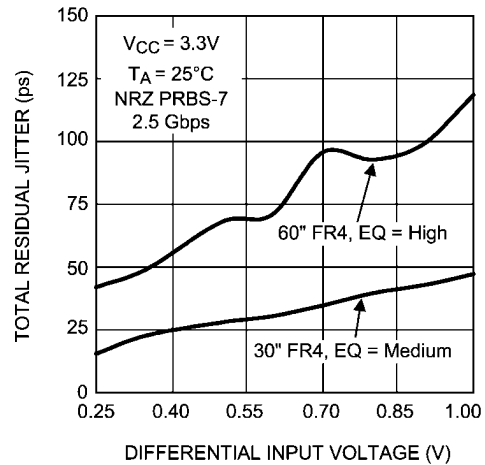
Total Jitter as a Function of Data Rate



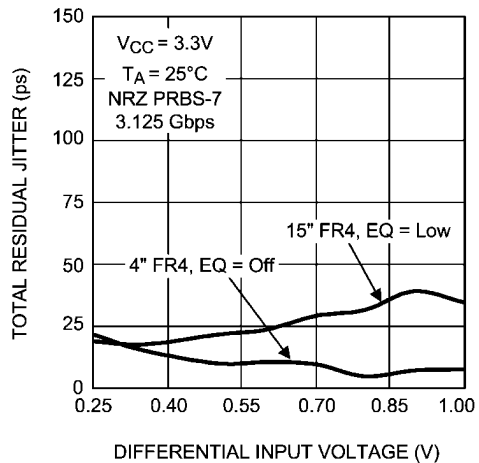
Total Jitter as a Function of Data Rate



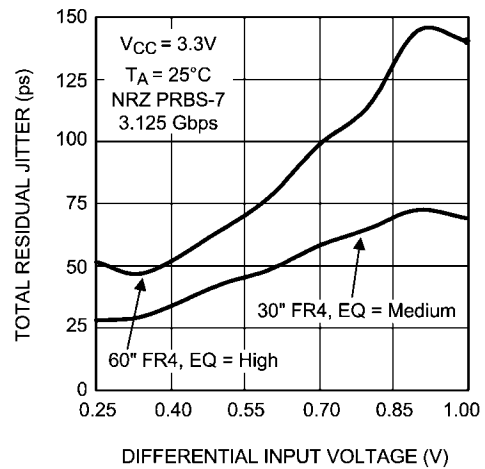
Total Jitter as a Function of Input Amplitude



Total Jitter as a Function of Input Amplitude



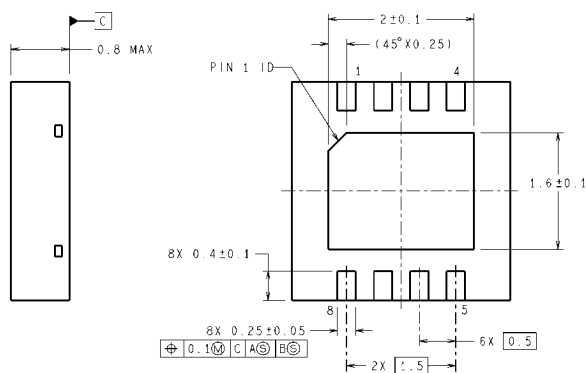
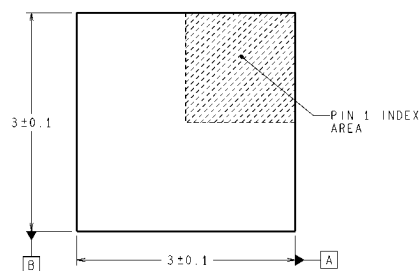
Total Jitter as a Function of Input Amplitude



Total Jitter as a Function of Input Amplitude



### RECOMMENDED LAND PATTERN



SDA08A (Rev A)

**Order Number DS25BR110TSD**  
**NS Package Number SDA08A**  
**(See AN-1187 for PCB Design and Assembly Recommendations)**

## Notes

## Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	<a href="http://www.national.com/amplifiers">www.national.com/amplifiers</a>	WEBENCH	<a href="http://www.national.com/webench">www.national.com/webench</a>
Audio	<a href="http://www.national.com/audio">www.national.com/audio</a>	Analog University	<a href="http://www.national.com/AU">www.national.com/AU</a>
Clock Conditioners	<a href="http://www.national.com/timing">www.national.com/timing</a>	App Notes	<a href="http://www.national.com/appnotes">www.national.com/appnotes</a>
Data Converters	<a href="http://www.national.com/adc">www.national.com/adc</a>	Distributors	<a href="http://www.national.com/contacts">www.national.com/contacts</a>
Displays	<a href="http://www.national.com/displays">www.national.com/displays</a>	Green Compliance	<a href="http://www.national.com/quality/green">www.national.com/quality/green</a>
Ethernet	<a href="http://www.national.com/ethernet">www.national.com/ethernet</a>	Packaging	<a href="http://www.national.com/packaging">www.national.com/packaging</a>
Interface	<a href="http://www.national.com/interface">www.national.com/interface</a>	Quality and Reliability	<a href="http://www.national.com/quality">www.national.com/quality</a>
LVDS	<a href="http://www.national.com/lvds">www.national.com/lvds</a>	Reference Designs	<a href="http://www.national.com/refdesigns">www.national.com/refdesigns</a>
Power Management	<a href="http://www.national.com/power">www.national.com/power</a>	Feedback	<a href="http://www.national.com/feedback">www.national.com/feedback</a>
Switching Regulators	<a href="http://www.national.com/switchers">www.national.com/switchers</a>		
LDOs	<a href="http://www.national.com/lido">www.national.com/lido</a>		
LED Lighting	<a href="http://www.national.com/led">www.national.com/led</a>		
PowerWise	<a href="http://www.national.com/powerwise">www.national.com/powerwise</a>		
Serial Digital Interface (SDI)	<a href="http://www.national.com/sdi">www.national.com/sdi</a>		
Temperature Sensors	<a href="http://www.national.com/tempsensors">www.national.com/tempsensors</a>		
Wireless (PLL/VCO)	<a href="http://www.national.com/wireless">www.national.com/wireless</a>		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

### LIFE SUPPORT POLICY

**NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION.** As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2007 National Semiconductor Corporation

For the most current product information visit us at [www.national.com](http://www.national.com)



**National Semiconductor  
Americas Customer  
Support Center**  
Email:  
[new.feedback@nsc.com](mailto:new.feedback@nsc.com)  
Tel: 1-800-272-9959

**National Semiconductor Europe  
Customer Support Center**  
Fax: +49 (0) 180-530-85-86  
Email: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +49 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia  
Pacific Customer Support Center**  
Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor Japan  
Customer Support Center**  
Fax: 81-3-5639-7507  
Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
Tel: 81-3-5639-7560