National Semiconductor

April 2007

DS25BR150
3.125 Gbps LVDS Buffer

General Description

The DS25BR150 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over printed circuit boards and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR150 is a buffer/repeater with very low power consumption. Other LVDS devices with similar IO characteristics and with signal conditioning features include the following products. The DS25BR110 features four levels of equalization for use as an optimized receiver device, the DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

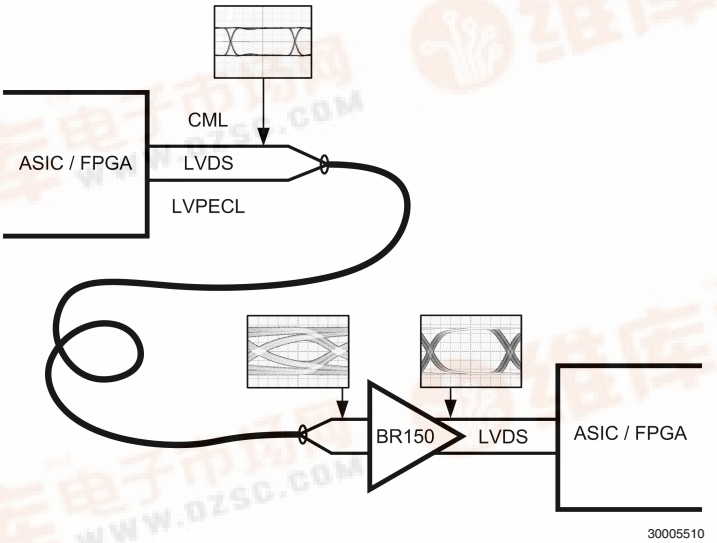
Features

- DC - 3.125 Gbps low jitter, high noise immunity, low power operation
- On-chip 100 Ω input and output termination minimizes insertion and return losses, reduces component count and minimizes board space
- 7 kV ESD on LVDS I/O pins protects adjoining components
- Small 3 mm x 3 mm LLP-8 space saving package

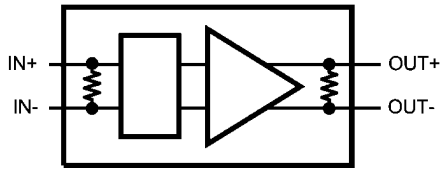
Applications

- Clock or data buffering / repeating
- OC-48 / STM-16 Clock or data buffering / repeating
- Serial ATA (SATA-150 and SATA-300)
- Fibre Channel (2GFC)
- PCI Express
- InfiniBand
- FireWire

Typical Application



Block Diagram



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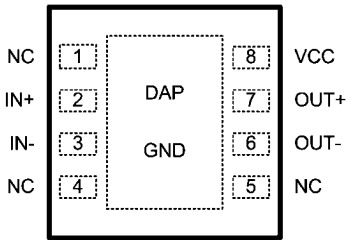
Pin Diagram



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Pin Descriptions

Pin Name	Pin Name	Pin Type	Pin Description
NC	1	NA	"NO CONNECT" pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
NC	4	NA	"NO CONNECT" pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

Ordering Codes and Configurations

NSID	Function
DS25BR150TSD	Buffer/Repeater

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVDS Input Voltage (IN+, IN−)	−0.3V to +4V
LVDS Differential Input Voltage ((IN+) - (IN−))	0V to 1V
LVDS Output Voltage (OUT+, OUT−)	−0.3V to +4V
LVDS Differential Output Voltage ((OUT+) - (OUT−))	0V to 1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SDA Package	2.08W
Derate SDA Package	16.7 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+60.0°C/W
θ_{JC}	+12.3°C/W
ESD Susceptibility	
HBM (Note 1)	≥7 kV
MM (Note 2)	≥250V
CDM (Note 3)	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current (Note 8)	OUT to GND		-25	-50	mA
		OUT to V_{CC}		7.5	50	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V_{ID}	Input Differential Voltage	V_{CM} = +0.05V or V_{CC}-0.05V	0		1	V
V_{TH}	Differential Input High Threshold			0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = 3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current			27	35	mA

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 7: Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics (Note 11)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 9, 10)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω			370	520	ps
t_{PLHD}	Differential Propagation Delay Low to High				355	520	ps
t_{SKD1}	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (Note 12)				15	100	ps
t_{SKD2}	Part to Part Skew (Note 13)				45	160	ps
t_{LHT}	Rise Time	R_L = 100Ω			80	150	ps
t_{HLT}	Fall Time				80	150	ps
JITTER PERFORMANCE (*Figure 5*)							
t_{DJ1}	Deterministic Jitter (Peak-to-Peak Value) (Note 15)	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		11	33	ps
t_{DJ2}			3.125 Gbps		15	41	ps
t_{RJ1}	Random Jitter (RMS Value) (Note 14)	V_{ID} = 350 mV V_{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1	ps
t_{RJ2}			1.5625 GHz		0.5	1	ps
t_{TJ1}	Total Jitter (Peak to Peak Value) (Note 16)	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.04	0.11	UI_{P-P}
t_{TJ2}			3.125 Gbps		0.07	0.15	UI_{P-P}

Note 9: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 10: Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 11: Specification is guaranteed by characterization and is not tested in production.

Note 12: t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 13: t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 14: Measured on a clock edge with a histogram and an acummulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

Note 15: Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

Note 16: Measured on an eye diagram with a histogram and an acummulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

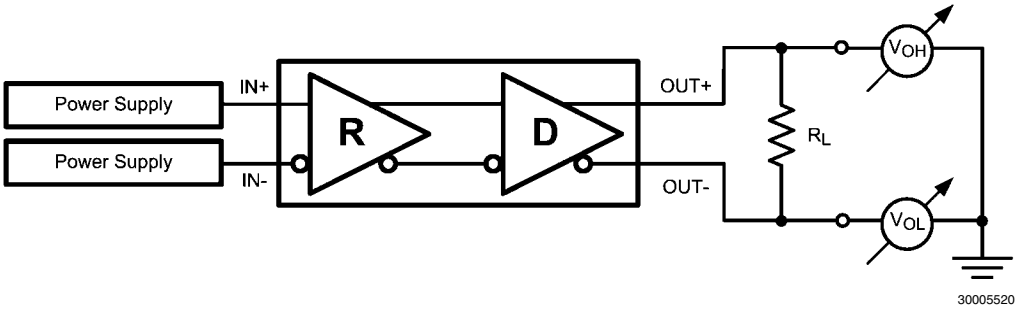


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

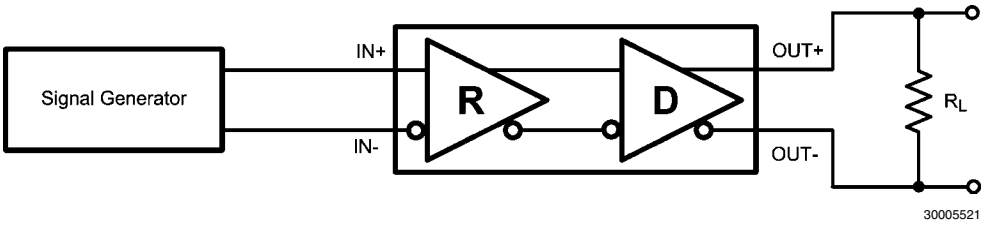


FIGURE 2. Differential Driver AC Test Circuit

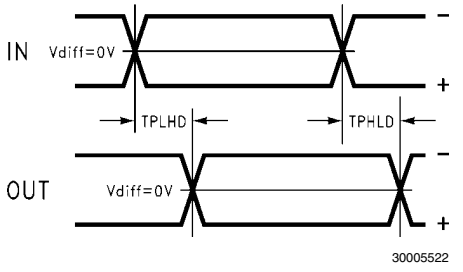


FIGURE 3. Propagation Delay Timing Diagram

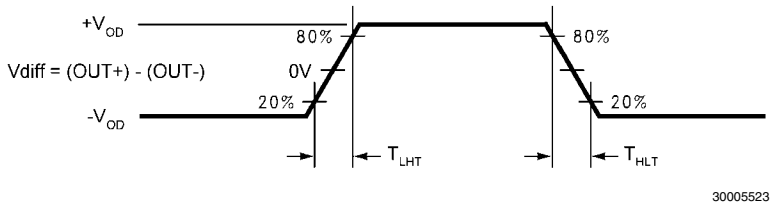


FIGURE 4. LVDS Output Transition Times

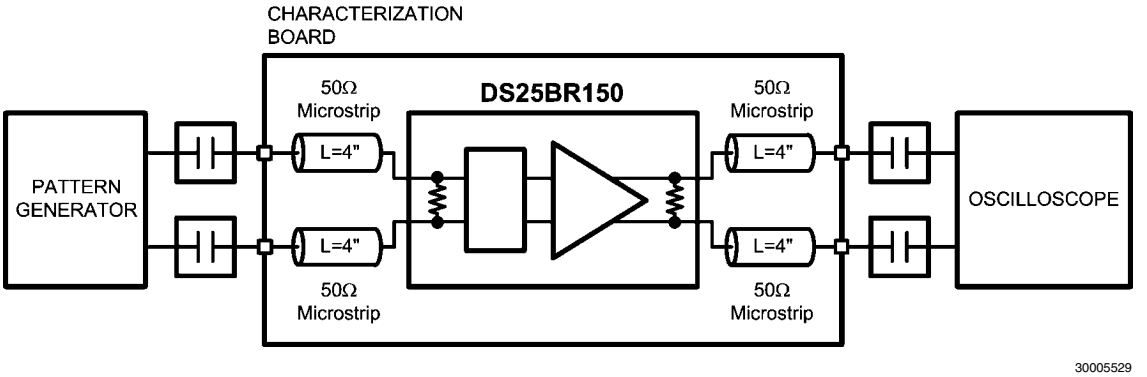
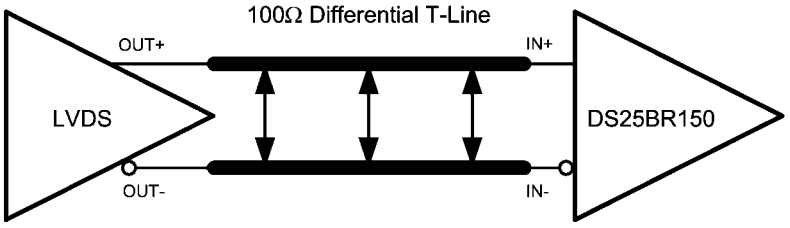


FIGURE 5. Jitter Measurements Test Circuit

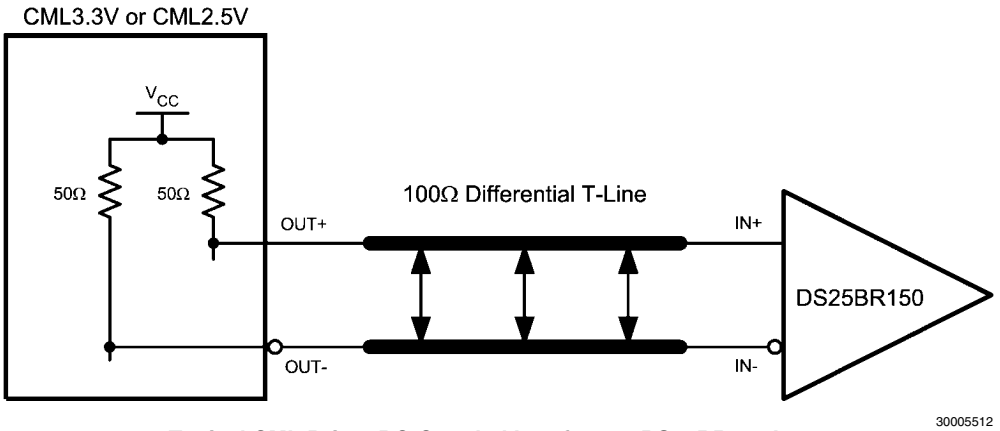
Device Operation

INPUT INTERFACING

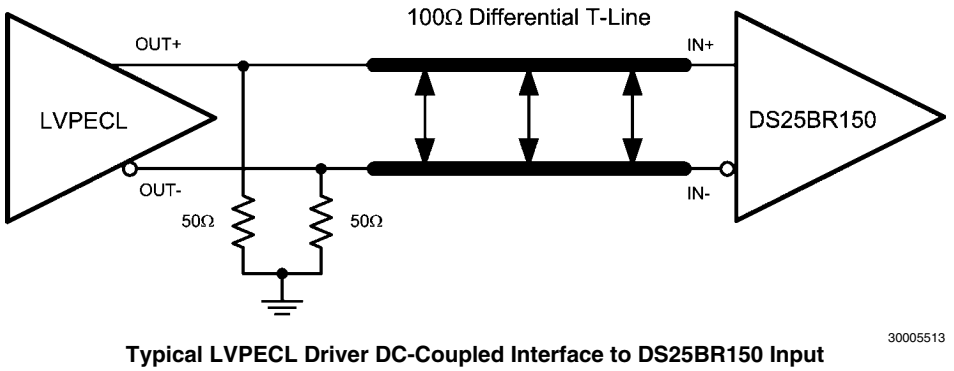
The DS25BR150 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR150 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR150 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to DS25BR150 Input



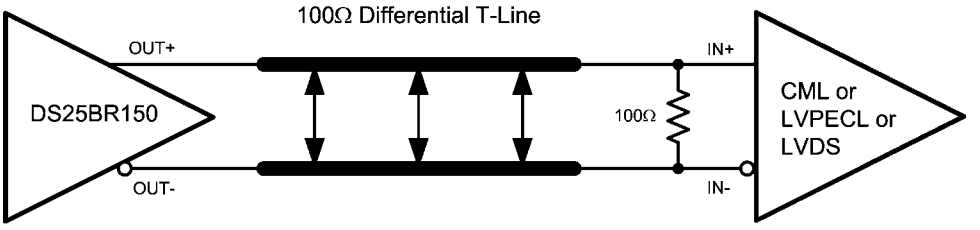
Typical CML Driver DC-Coupled Interface to DS25BR150 Input



Typical LVPECL Driver DC-Coupled Interface to DS25BR150 Input

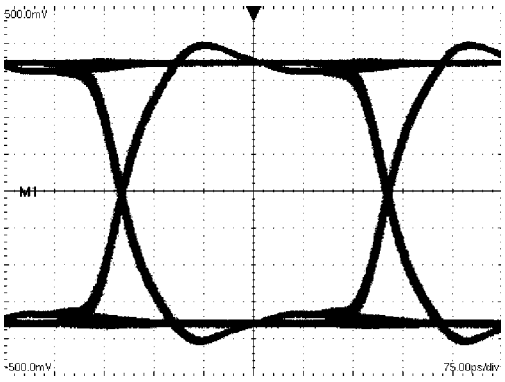
OUTPUT INTERFACING

The DS25BR150 outputs signals are compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



Typical DS25BR150 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance



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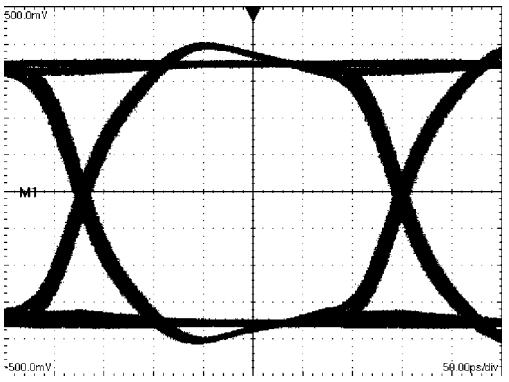
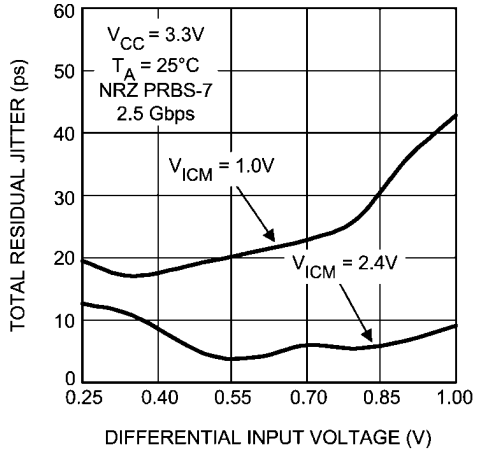
A 2.5 Gbps NRZ PRBS-7 Output Eye Diagram
V:100 mV / DIV, H:75 ps / DIV



30005530

A 3.125 Gbps NRZ PRBS-7 Output Eye Diagram
V:100 mV / DIV, H:50 ps / DIV



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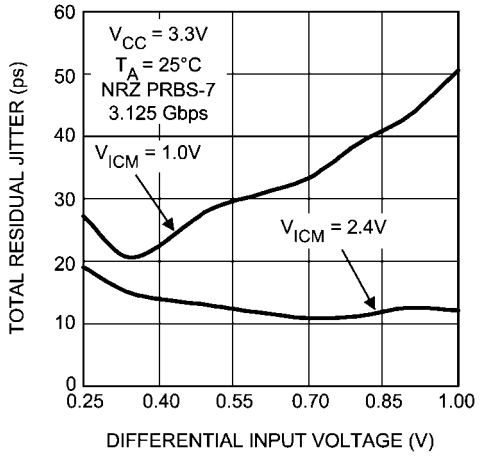
Total Jitter as a Function of Input Amplitude



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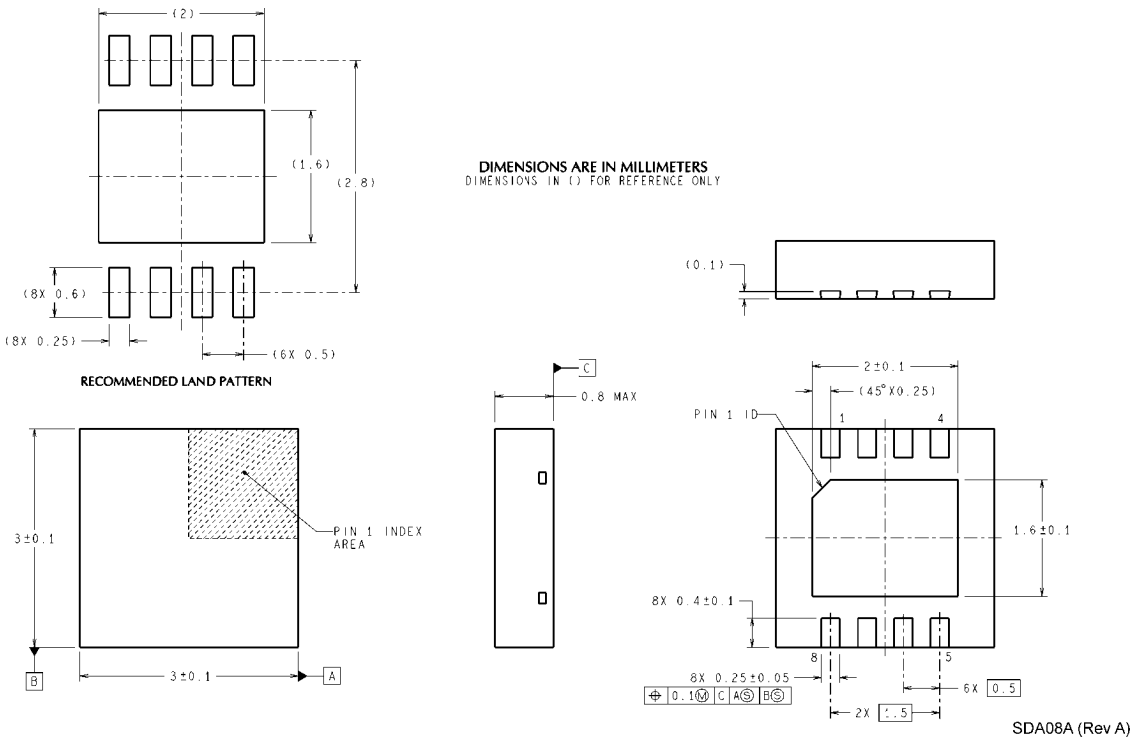
Total Jitter as a Function of Input Amplitude

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS25BR150TSD
NS Package Number SDA08A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

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