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National Semiconductor

MICROCIRCUIT DATA SHEET

MNDS26C31M-X REV 0B0

Original Creation Date: 01/23/96
Last Update Date: 05/04/01
Last Major Revision Date: 01/23/96

CMOS QUAD TRI-STATE DIFFERENTIAL LINE DRIVER

General Description

The DS26C31 is a qual differential line driver designed for digital data transmission over balanced lines. The DS26C31 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to Vcc and ground.

Industry Part Number

DS26C31

NS Part Numbers

DS26C31ME/883
DS26C31MJ/883
DS26C31MW/883
DS26C31MWG/883

Prime Die

DS26C31

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

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Features

- TTL input compatible
- Outputs won't load line when Vcc = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current

CONTROLLING DOCUMENTS:

DS26C31ME/883	5962-9163901M2A
DS26C31MJ/883	5962-9163901MEA
DS26C31MW/883	5962-9163901MFA
DS26C31MWG/883	5962-9163901MXA

(Absolute Maximum Ratings)

(Note 1, 2)

Supply Voltage (Vcc)	-0.5V to 7.0V
DC Input Voltage (Vin)	-0.5V to Vcc +0.5V
DC Output Voltage (Vout)	-0.5V to 7V
Clamp Diode Current (Iik, Iok)	± 20mA
DC Output Current, per Pin (Iout)	± 150mA
DC Vcc or Gnd Current, per Pin (Icc)	± 150mA
Storage Temperature Range (Tstg)	-65 C ≤ Ta ≤ +150 C
Lead Temperature (Tl) (Soldering, 4 seconds)	260 C

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Recommended Operating Conditions

Supply Voltage (Vcc)	4.50V to 5.50V
DC Input or Output Voltage (Vin, Vout)	0V to Vcc
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical "1" Input Voltage				2.0		V	1, 2, 3
Vil	Logical "0" Input Voltage					0.8	V	1, 2, 3
Voh	Logical "1" Output Voltage	Vin=Vih or Vil, Vcc=4.5V, Iout=-20mA			2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vin=Vih or Vil, Iout=20mA, Vcc=4.5V				0.5	V	1, 2, 3
Vt	Differential Output Voltage	Rl=100 Ohms, Vcc=4.5V	1		2.0		V	1, 2, 3
|Vt|-|$\overline{Vt}$|	Difference in Differential Output	Rl=100 Ohms, Vcc=4.5V	1			0.4	V	1, 2, 3
Vos	Common Mode Output Voltage	Rl=100 Ohms, Vcc=5.5V	1			3.0	V	1, 2, 3
|Vos-$\overline{Vos}$|	Difference in Common Mode Output	Rl=100 Ohms, Vcc=5.5V	1			0.4	V	1, 2, 3
Iin	Input Current	Vin=Vcc, Gnd, Vih, or Vil, Vcc=5.5V				± 1.0	uA	1, 2, 3
Icc	Quiescent Power Supply Current	Iout=0uA, Vin=Vcc or Gnd, Vcc=5.5V	2			500	uA	1, 2, 3
		Iout=0uA, Vin=2.4V or 0.5V, Vcc=5.5V	2			2.1	mA	1, 2, 3
Ioz	TRI-STATE Output Leakage Current	Vout=Vcc or Gnd, Enable=Vil, Vcc=5.5V, $\overline{Enable}$ = Vih				± 5.0	uA	1, 2, 3
Isc	Output Short Circuit Current	Vin=Vcc or Gnd, Vcc=5.5V	1, 3		-30	-150	mA	1, 2, 3
Ioff	Output Leakage Current "Power Off"	Vcc=0V, Vout=6V				100	uA	1, 2, 3
		Vcc=0V, Vout=0V				-100	uA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc=5V, tr <= 6nS, tf <= 6nS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Input to Output Propagation Delay					14	nS	9, 10, 11
tPHL	Input to Output Propagation Dalay					14	nS	9, 10, 11
	Skew		4			3	nS	9, 10, 11
tTLH	Output Rise Time					14	nS	9, 10, 11
tTHL	Output Fall Time					14	nS	9, 10, 11
tPZH	Output Enable Time					22	nS	9, 10, 11
tPZL	Output Enable Time					28	nS	9, 10, 11
tPHZ	Output Disable Time		5			12	nS	9, 10, 11
tPLZ	Output Disable Time		5			14	nS	9, 10, 11

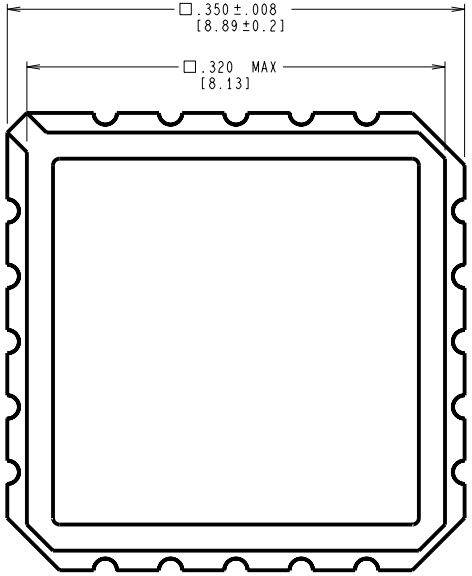
Note 1: See EIA specification RS-422 for exact test condition.
Note 2: Measure per input. All other inputs at Vcc or Gnd.
Note 3: This is a current sourced when a high output is shorted to Gnd. Only one output at a time should be shorted.
Note 4: Skew is defined as the difference in Progation Delay between complimentary output at 50% point.
Note 5: Output Disable time is the delay from Enable or $\overline{\text{Enable}}$ being switched to the output transistor turning off.

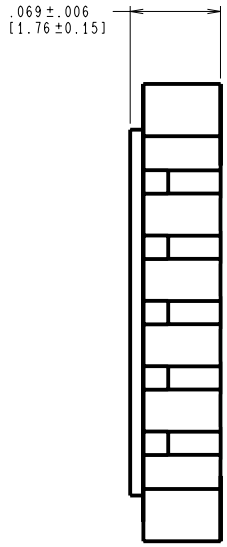
Graphics and Diagrams

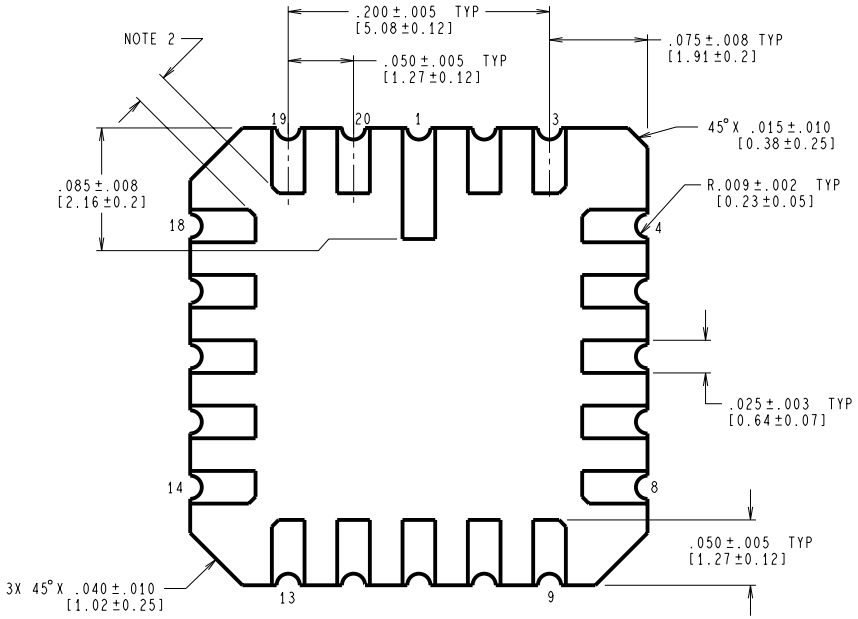
GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
P000435A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
P000436A	CERDIP (J), 16 LEAD (PIN OUT)
P000437A	LCC (E), TYPE C, 20 TERMINAL (PIN OUT)
P000442A	CERPACK (W), 16 LEAD (PIN OUT)
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/







CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45° X .020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

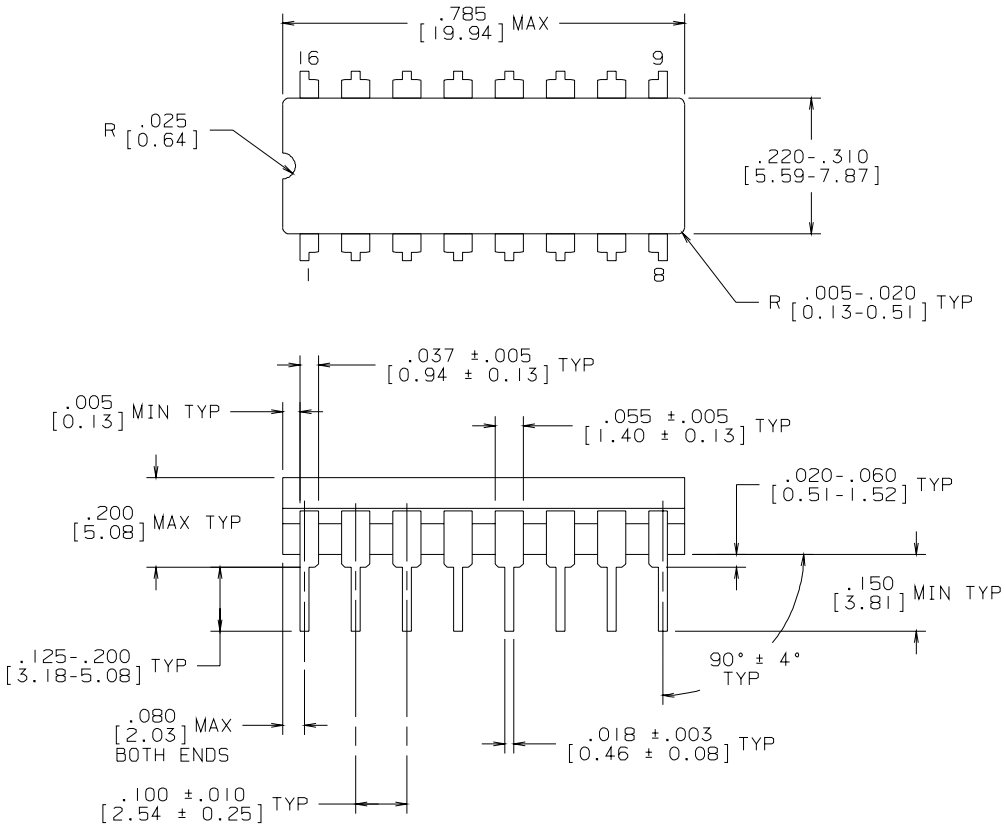
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

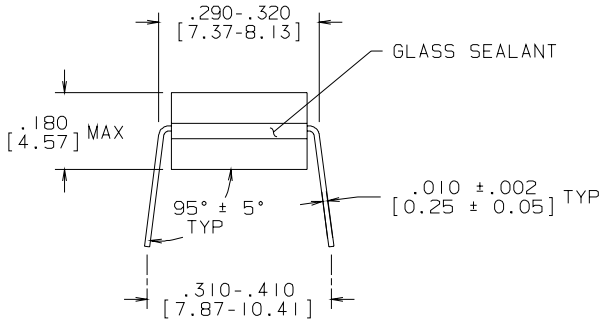
LEADLESS CHIP CARRIER,
TYPE C,
20 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/





MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

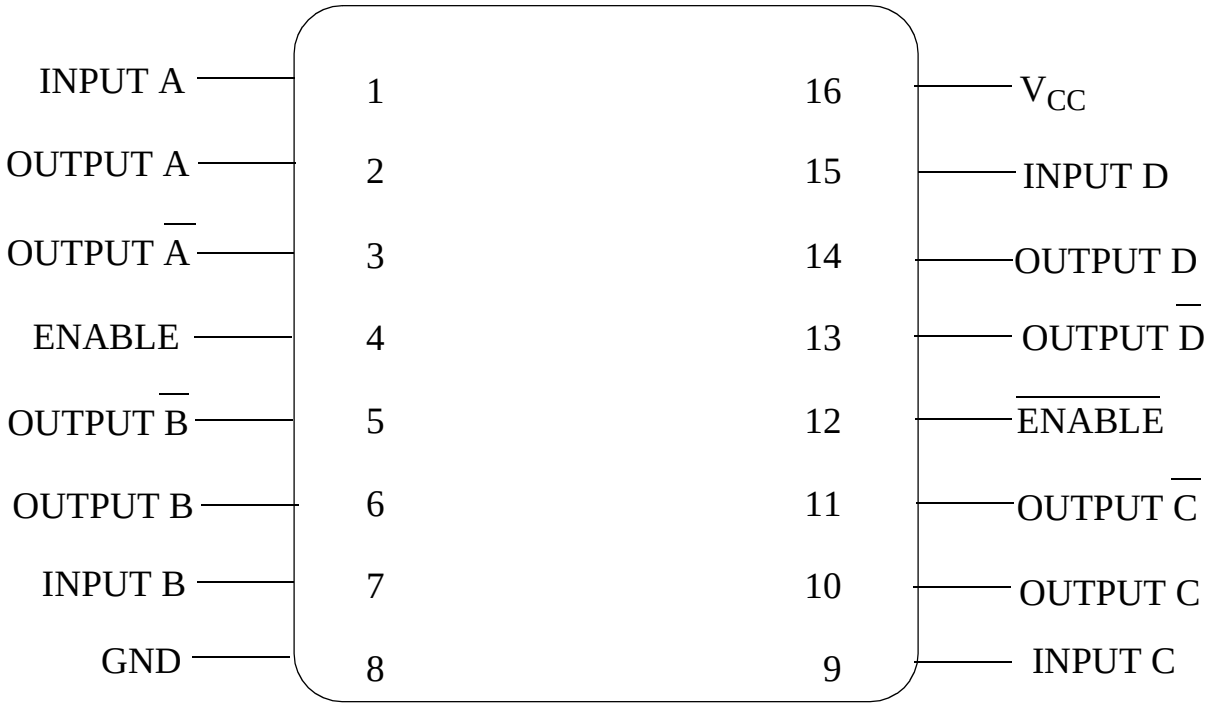
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

PROJECTION INCH [MM]

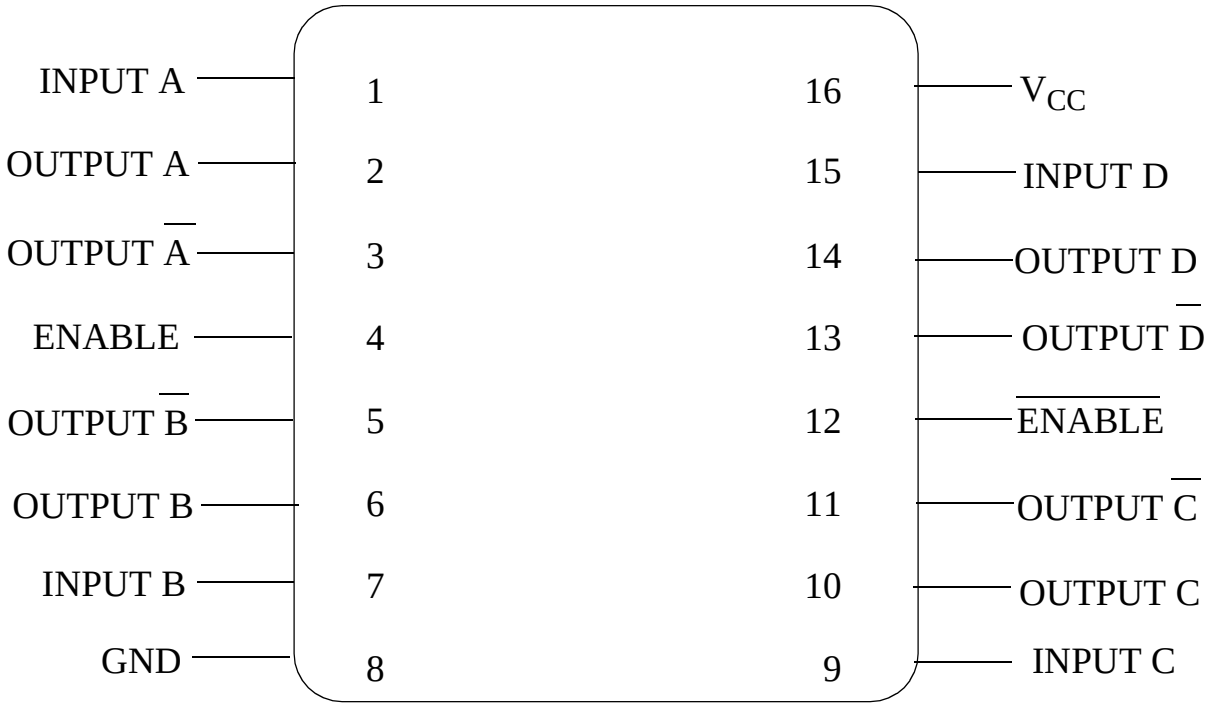
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



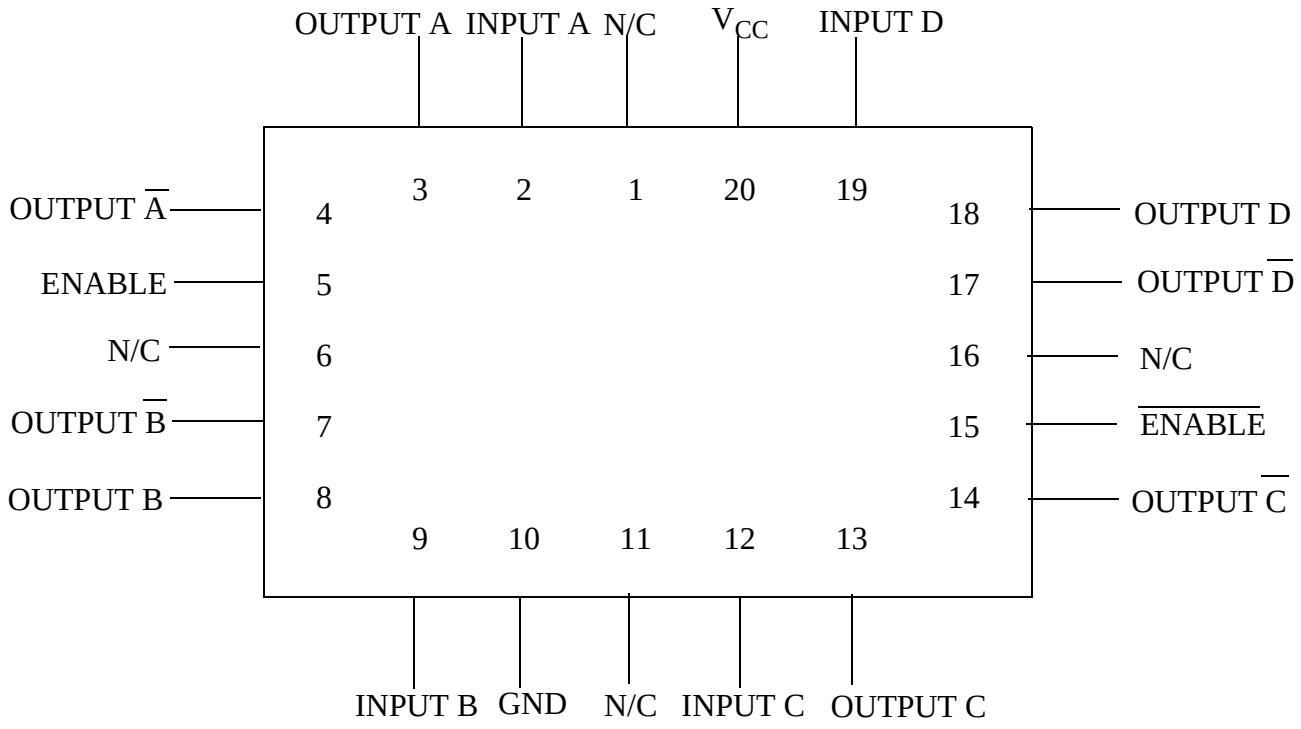
DS26C31WG
16 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000435A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



DS26C31J
16 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000436A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



DS26C31E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000437A

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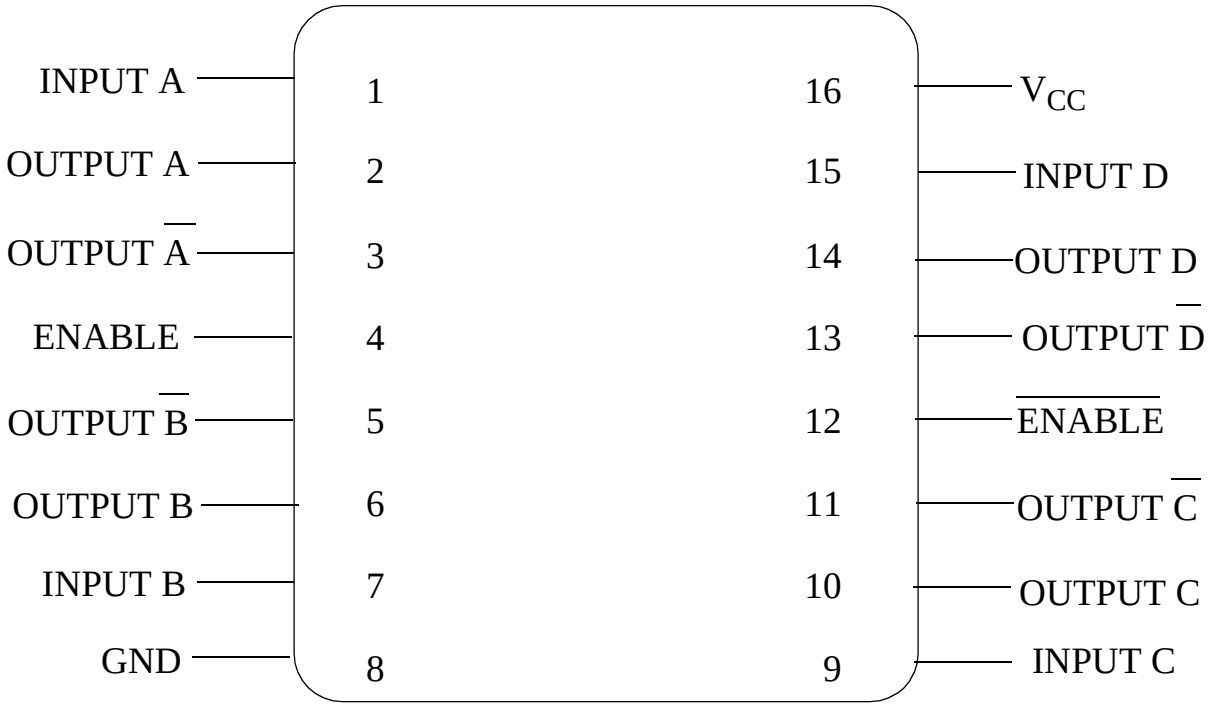
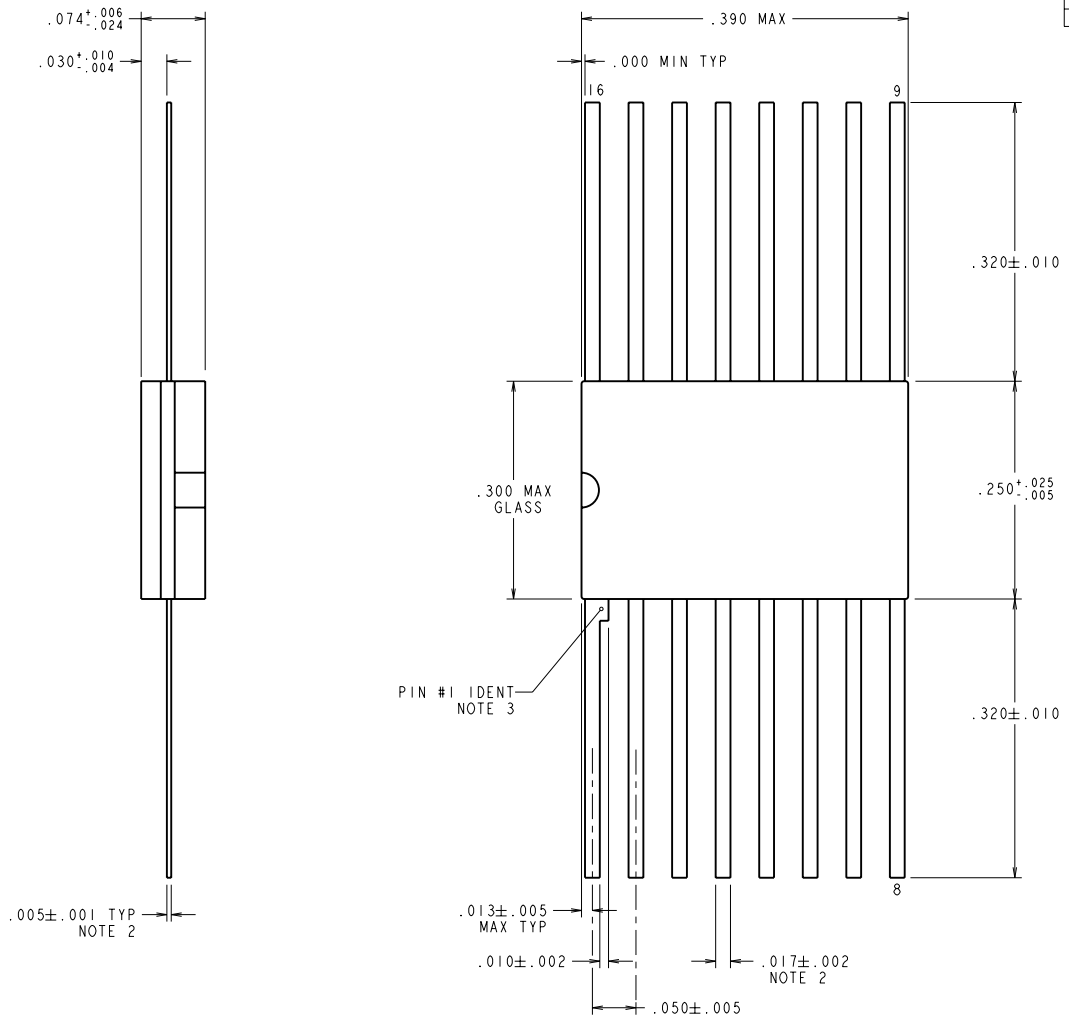
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



DS26C31W
16 - LEAD CERPACK
CONNECTION DIAGRAM
TOP VIEW
P000442A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

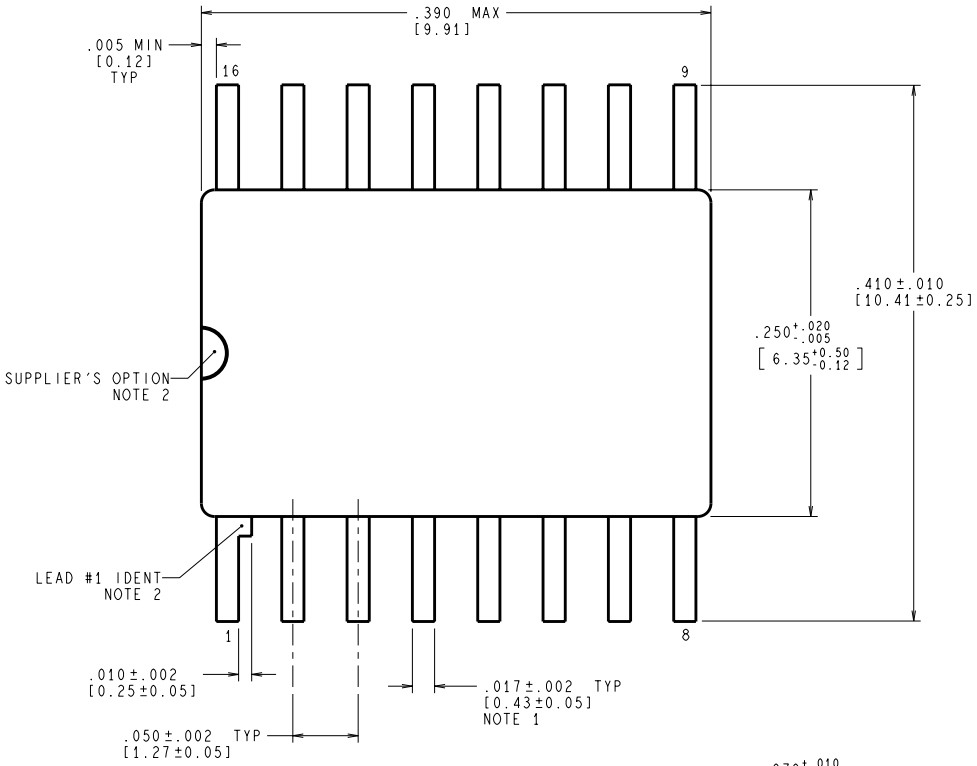
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

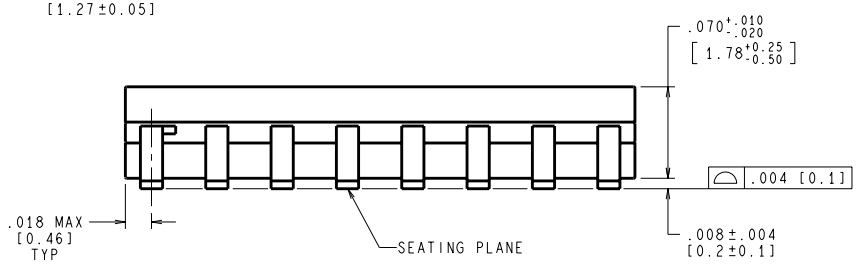
CERPACK, 16 LEAD

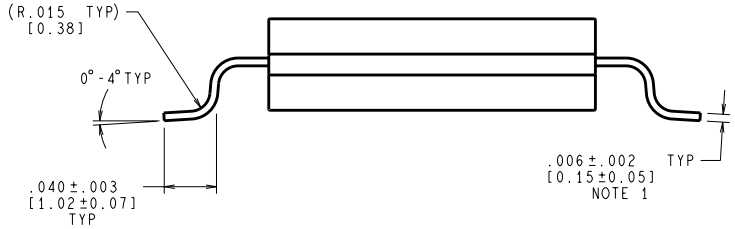
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr. Santa Clara, CA 95052-8090

CERPACK, 16 LEAD, GULL WING

PROJECTION INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0002086	05/04/01	Rose Malone	Update MDS: MNDS26C31M-X, Rev. 0A0 to MNDS26C31M-X, Rev. 0B0. Added to Main Table, Features Section and Graphics Section reference WG pkg.