Rev: 111607

DS3205
Hot-Swappable Bus Buffer for I²C, SMBus, IPMI, and ATCA

General Description

The DS3205 bus buffer enables hot insertion and extraction of boards without corruption of the backplane's 2-wire bus (I^2C, SMBus™, IPMI, etc.). When a board is inserted, the DS3205 presents high-impedance SCL and SDA connections to the backplane until V_{DD} rises above 2.5V. During normal operation, the DS3205 provides bidirectional buffering to keep backplane and board capacitances isolated.

Rise-time accelerators on each 2-wire bus pin enable the use of lower current pullup resistors while still meeting rise-time requirements.

Applications

Hot-Swappable Boards for AdvancedTCA®, CompactPCI®, VME, and Other Backplanes in Chassis-Oriented Telecom, Datacom, Computing, and Storage Systems
Capacitance Buffer
Bus Extender
Fault Isolator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
DS3205DN+	-40°C to +85°C	14 TDFN	T1433-1

+Denotes a lead-free package.

Features

- **Compliant to PICMG 3.0 IPMI I^2C Requirements**
- **Bidirectional Buffer for SCL and SDA Lines**
- **Compatible with I^2C, I^2C Fast Mode, SMBus, IPMI, and ATCA® Standards (Up to 400kHz)**
- **Prevents Corruption of System SCL and SDA Lines During Live Insertion/Removal of Boards**
- **Increases Fanout by Connecting Board Bus to Backplane Bus with < 10pF Additional Load**
- **Automatically Delays Initial Bus Connection Until Both Bus Segments Are Idle**
- **SCL and SDA Pins High-Z When V_{DD} = 0V**
- **1V Precharge on SCL and SDA Lines**
- **ENABLE Input Pin Connects or Isolates Buses**
- **READY Output Pin Indicates "Connected"**
- **$\overline{FAULT}$ Output Pin Indicates "Stuck Bus"**
- **Optional Rise-Time Accelerators on All Bus Pins**
- **Configurable Rise-Time Accelerator Slew Rate Threshold (0.8V/µs or 1.25V/µs)**
- **Supports Clock Stretching and Multiple Bus Master Arbitration and Synchronization**
- **Optionally Disconnects Board from Backplane When Bus is Stuck Low for ≥ 30ms**
- **Optionally Attempts to Recover a Stuck Bus by Clocking Board SCL**
- **±15kV ESD Protection (Human Body Model) on Bus Pins**
- **Wide Operating Voltage Range: 2.7V to 5.5V**
- **5V Tolerant I/Os**
- **Tiny 14-Pin, 3mm x 3mm TDFN Package**

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ATCA, AdvancedTCA, and CompactPCI are registered trademarks of PCI Industrial Computer Manufacturers Group (PICMG).

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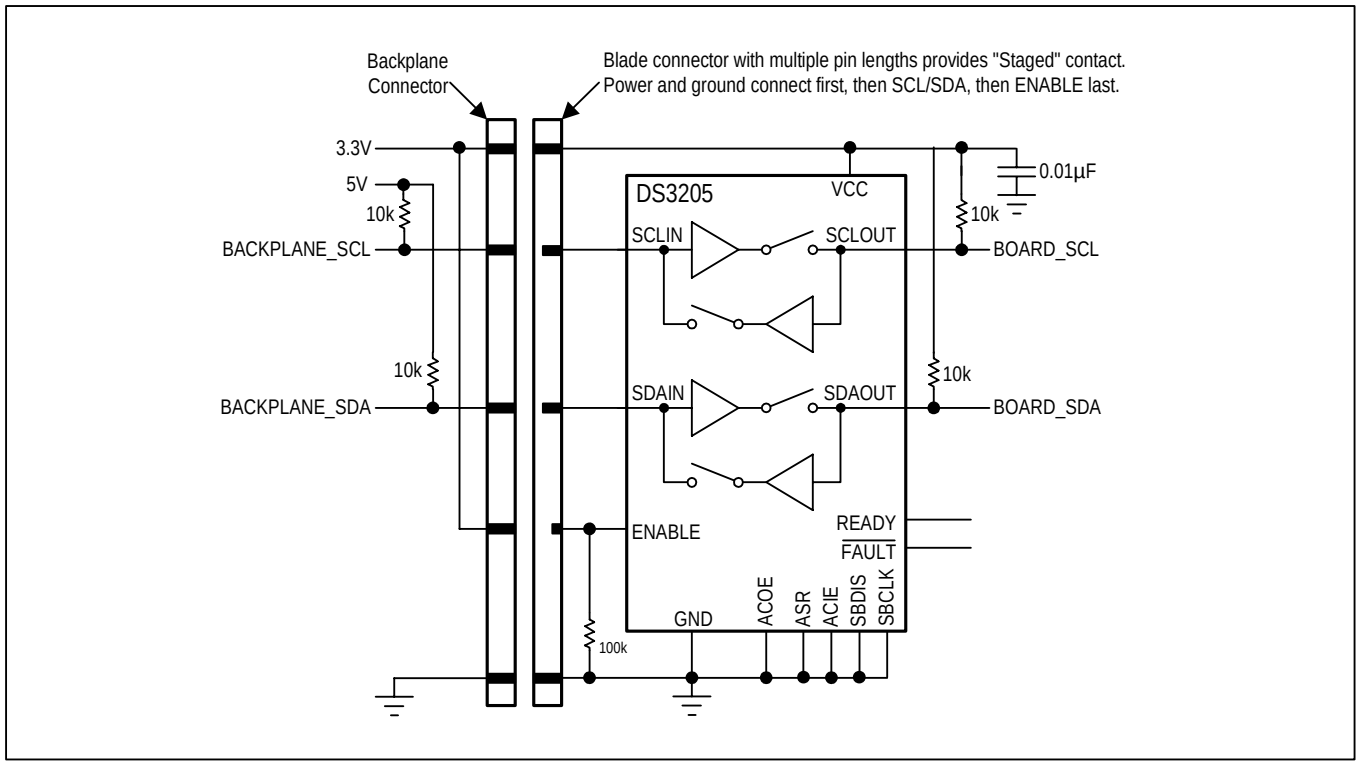
1. Typical ATCA Application

Figure 1-1 shows an ATCA blade application for the DS3205. In this application the DS3205 is used as a buffer for the Intelligent Platform Management Bus (IPMB). The IPMB is used in ATCA for communications between and management of all Field Replaceable Units (FRUs). The DS3205 is compliant with the ATCA IPMB requirements as specified in PICMG 3.0 AdvancedTCA Base Requirements.

Figure 1-1. Typical Application (ATCA Blade)



2. Applicable Diagrams

Figure 2-1. Block Diagram

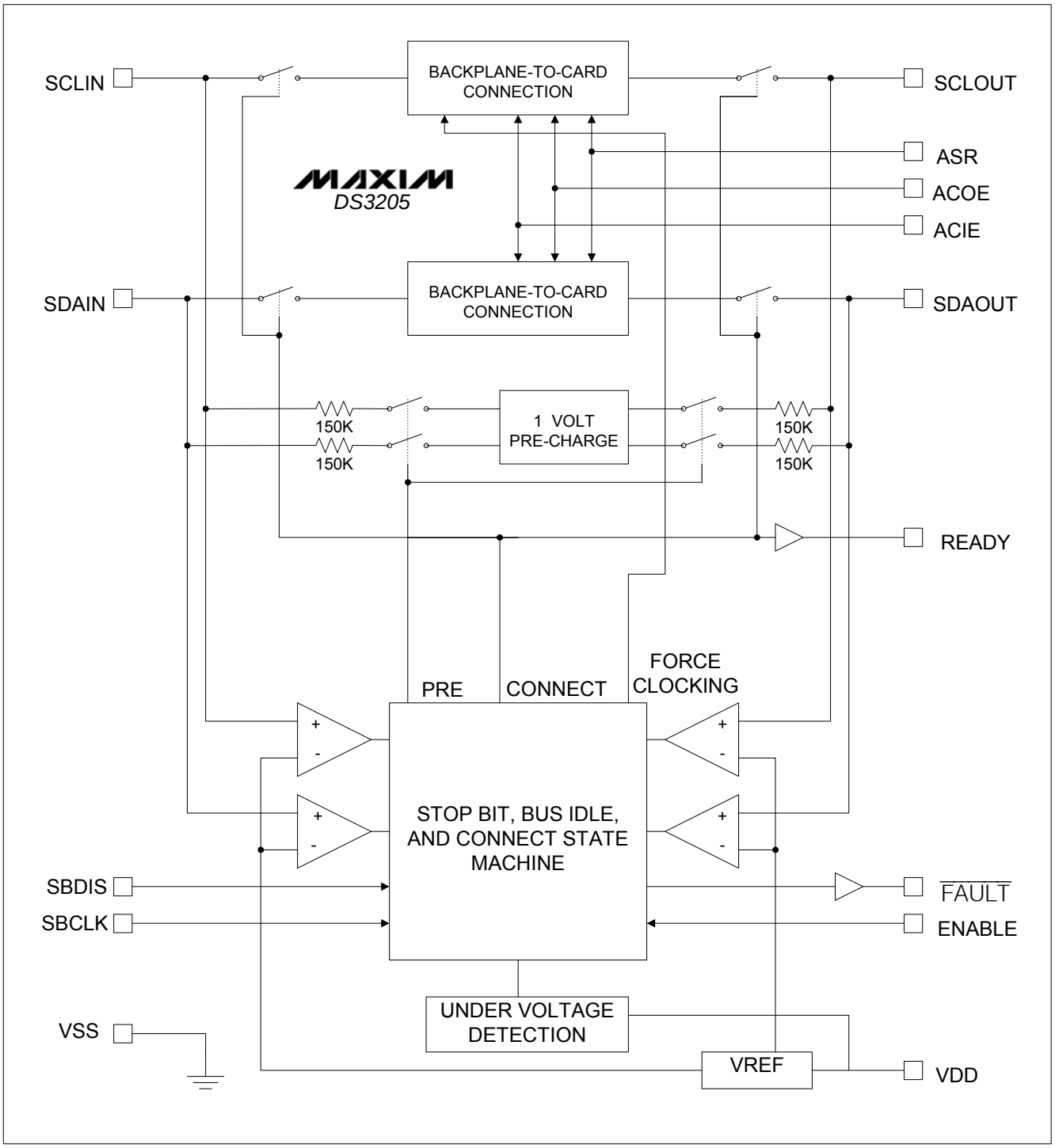


Figure 2-2. Backplane-to-Card Connection Detail

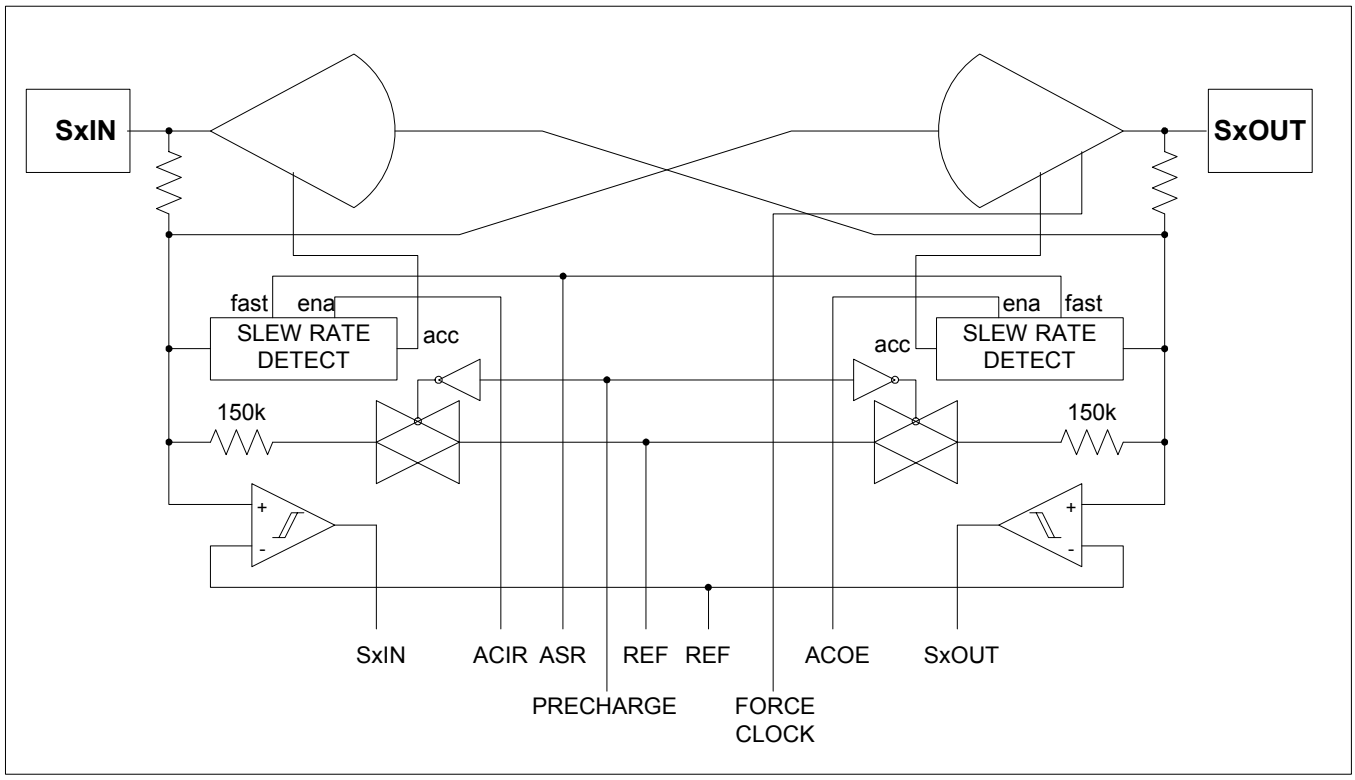
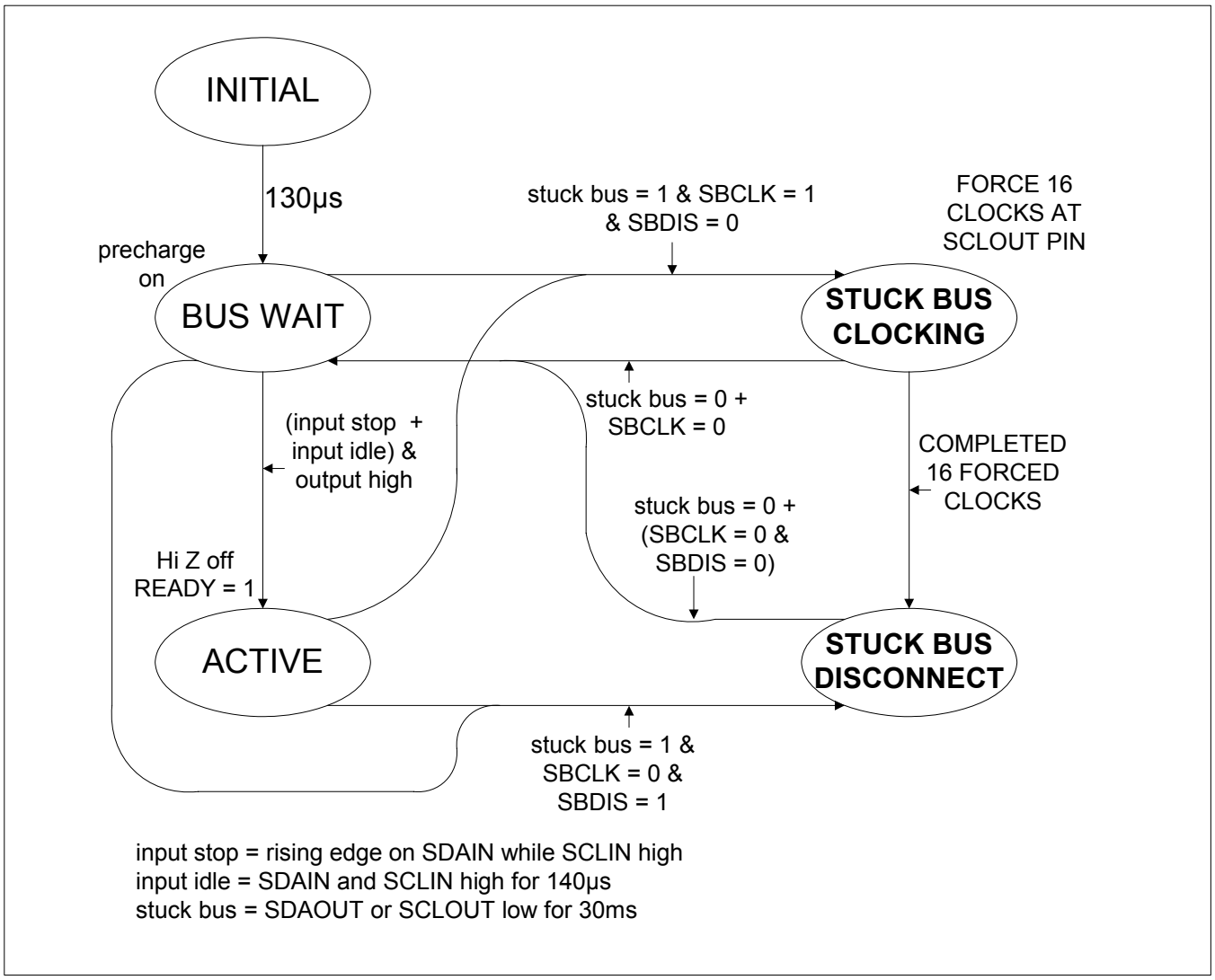


Figure 2-3. DS3205 State Diagram



3. Pin Descriptions

Table 3-1. Pin Descriptions

NAME	PIN	TYPE	FUNCTION
ENABLE	1	I	**Enable Input.** This input pin establishes the board-to-backplane connection when driven to a level above $V_{DD}/2$ (approximately) with 50mV hysteresis. 0 = Disable connection and enter low-power mode. 1 = Enable connection of backplane and board buses.
SCLOUT	2	I/O	**Serial Clock Output.** This pin is connected to the board's SCL signal.
SDAOUT	3	I/O	**Serial Data Output.** This pin is connected to the board's SDA signal.
ACIE	4	I	**Accelerator Current on Inputs Enable.** This input pin enables/disables the rise-time accelerators on the bus input pins. 0 = Disable rise-time accelerator on SCLIN and SDAIN. 1 = Enable rise-time accelerator on SCLIN and SDAIN.
ACOE	5	I	**Accelerator Current on Outputs Enable.** This input pin enables/disables the rise-time accelerators on the bus output pins. 0 = Disable rise-time accelerator on SCLOUT and SDAOUT. 1 = Enable rise-time accelerator on SCLOUT and SDAOUT.
ASR	6	I	**Accelerator Slew Rate Threshold Select.** This input pin selects the rate for the rise-time accelerators. 0 = 0.8V/µs 1 = 1.25V/µs
V_{SS}	7	P	**Ground**
READY	8	Ood	**Connected Status Indicator.** This is an open-drain output that goes high when the device is in the ACTIVE state. See the state diagram in Figure 2-3. This pin should have an external 10kΩ pullup resistor. 0 = Backplane and board buses not connected. 1 (float) = Backplane and board buses connected.
$\overline{FAULT}$	9	Ood	**Active-Low Bus Fault Indicator.** This open-drain output pin indicates a "stuck bus" condition when = 0. This pin should have an external 10kΩ pullup resistor. 0 = Either SCLOUT or SDAOUT has been low > 30ms. 1 = No stuck bus fault.
SBCLK	10	I	**Stuck Bus Clocking Enable.** Asserting this pin high causes the DS3205 to drive clock pulses onto the SCLOUT pin in an attempt to free a stuck bus when a "stuck bus" condition has been detected. See Section 4 and Figure 2-3 for more information on the stuck bus condition. 0 = Disable automatic clocking during stuck bus fault. 1 = Enable automatic clocking during stuck bus fault. **Note:** Asserting both SBDIS and SBCLK high at the same time is not valid and can produce unwanted results.
SBDIS	11	I	**Stuck Bus Disconnect Enable.** Asserting this pin high causes the DS3205 to disconnect the backplane signals from the board signals when a "stuck bus" condition has been detected. See Section 4 and Figure 2-3 for more information on the stuck bus condition. 0 = Disable automatic disconnect on stuck bus fault. 1 = Enable automatic disconnect on stuck bus fault. **Note:** Asserting both SBDIS and SBCLK high at the same time is not valid and can produce unwanted results.

NAME	PIN	TYPE	FUNCTION
SDAIN	12	I/O	**Serial Data Input.** This pin is connected to the backplane SDA signal.
SCLIN	13	I/O	**Serial Clock Input.** This pin is connected to the backplane SCL signal.
V_{DD}	14	P	**Power Supply.** 2.7V to 5.5V
EP	—	—	**Exposed Pad**

I/O = Input/Output
I = Input
Ood = Output, Open Drain
P = Power

4. Functional Description

4.1 Overview

See the DS3205 state diagram in Figure 2-3.

4.2 Startup

When the DS3205 is first powered on, it is in a low-power state with the SCLIN, SCLOUT, SDAIN, and SDAOUT pins in a high-impedance state. If the ENABLE pin is pulled high, the DS3205 waits until the supply voltage rises above approximately 2V, when the precharge circuitry becomes active and forces 1V through 150kΩ resistors into all SCL and SDA pins. The 1V precharge minimizes bus disturbances when the backplane and card are at opposing logic levels. The DS3205 then waits about 130µs for the external connections and internal circuitry to settle. After this wait time, the DS3205 enters the BUS WAIT state where it looks for either a stop bit on the input (rising edge on the SDAIN pin while SCLIN remains high) or an input bus idle condition (SDAIN and SCLIN both high for 140µs) while both SDAOUT and SCLOUT pins are high. Once these conditions are met, the precharge circuit is turned off and the DS3205 enters the ACTIVE state.

While in the ACTIVE state, the DS3205 establishes a bidirectional connection between the SDAIN and SDAOUT pins and the SCLIN and SCLOUT pins. The voltage on any bus pin is buffered and offset an additional +75mV (approximately) to the other side. Whichever side is pulled closest to ground has priority. For example, if SCLOUT is pulled closer to ground than SCIN, SCIN is driven to a voltage 75mV higher than SCOUT.

4.3 Rise-Time Accelerators

If current acceleration is enabled through the ACIE or ACOE pins, the DS3205 pulls up more strongly, shortening the rise time compared to using only the external bus pullup resistors. The pullup provided by the driver during acceleration is approximately 3.5mA instead of its usual 100µA. This acceleration current on one side of the buffer is activated when the bus voltage on the other side is greater than 0.6V and its slew rate is greater than 0.8V/µs (ASR low) or 1.2V/µs (ASR high) and the corresponding ACIE and/or ACOE pin is pulled high. The acceleration current is deactivated after the accelerated bus pin rises within 0.9V of V_{DD}. For example, if the ACOE pin is high, when the SCLIN pin rises above 0.6V with a fast slew rate, the SCLOUT pin is pulled up towards V_{DD} with more than 3mA of current. This current ceases when the SCLOUT pin rises to within 0.9V of V_{DD}.

4.4 READY Output Pin

The READY pin is pulled low whenever the DS3205 is not in its ACTIVE state. An external pullup resistor brings the READY pin high when the bidirectional connection is established.

4.5 ENABLE Input Pin

If the ENABLE pin is pulled low, the backplane side disconnects from the board side and the device enters a low-power state with the READY pin asserted low. Also, the rise-time accelerators and precharge circuitry are disabled. Setting ENABLE low causes the device to disconnect the board side from the backplane side and enter the low-power mode.

4.6 Stuck Bus Condition

If the SDAOUT and SCLOUT pins remain low for 30ms the bus is assumed to be stuck. This 30ms timeout is restarted only when the SDAOUT and SCLOUT pins are both high. The $\overline{FAULT}$ pin pulls low and remains low until the bus is unstuck. If the SBCLK pin is high, the DS3205 attempts to unstick the bus by first disconnecting all SDA and SCL pins for 50µs, then pulls down on the SCLOUT pin 16 times at a 8kHz rate. If the bus becomes unstuck during this process (SDAOUT and SCLOUT both go high), the DS3205 returns to the BUS WAIT state. The precharge circuitry becomes active, and, as soon as a stop bit or bus idle is detected on the input while both

SDAOUT and SCLOUT pins are high, the DS3205 goes to the ACTIVE state, reestablishing bidirectional buffering. If the bus remains stuck after 16 clocks, the DS3205 sits with all SDA and SCL pins precharged until SDAOUT and SCLOUT go high. If the SBCLK pin is low and the SBDIS pin is high, the DS3205 only precharges the SDA and SCL pins until the bus becomes unstuck. If neither SBCLK nor SBDIS are high, the DS3205 remains in its ACTIVE state, but the $\overline{\text{FAULT}}$ pin pulls low as an alert that the bus is stuck.

If the DS3205 is in the STUCK BUS CLOCKING state, setting the SBCLK pin low forces the part into the BUS WAIT state. If the DS3205 is in the STUCK BUS DISCONNECT state, setting the SBDIS pin low forces the part into the BUS WAIT state. These transitions are shown in the state diagram in Figure 2-3. Returning to the BUS WAIT state resets the 30ms stuck bus counter.

4.7 Bus Capacitance Requirements

A minimum of 47pF bus capacitance is required on 5V systems; 3.3V systems require a minimum of 22pF for proper operation. Buses with less capacitance should be provisioned with an added capacitor to ground in order to maintain the minimum required capacitance. The DS3205 tolerates capacitance levels slightly marginal with respect to these requirements.

4.8 Pullup Resistor

When SCLIN, SCLOUT, SDAIN, or SDAOUT is driven to a logic-low level, that pin's corresponding output pin is driven to a slightly higher level. For example, if SDAOUT is driven low, SDAIN is driven to a level according to the following formula.

$$V_{SDAIN} = V_{SDAOUT} + 75mV + (V_{DD} / R) \times 20\Omega$$

EXAMPLE:

IF R = bus pullup resistor = 10kΩ
IF V_{DD} = 3.3V
IF V_{SDAOUT} = 10mV
V_{SDAIN} = 91.6mV (typical)

5. Operating Parameters

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to V_{SS} (except V_{DD})……0.5V to 6.0V
Supply Voltage Range (V_{DD}) with Respect to V_{SS}……0.5V to 6.0V
Operating Temperature Range……-40°C to +85°C (**Note 1**)
Storage Temperature Range……-55°C to +125°C
Soldering Temperature……Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

5.1 Electrical Characteristics

Table 5-1. Power Supply

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		2.7		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5V, V_{SDAIN} = V_{SCLIN} = 0V		4	7	mA
Shutdown Current	I_{SD}	V_{ENABLE} = 0V, all other pins at V_{DD} or V_{SS}		200	500	µA

Table 5-2. Startup Characteristics

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Precharge Voltage	V_{PRE}	SDA, SCL floating (Note 1)	0.75	1.00	1.25	V
ENABLE Threshold Rising	$V_{THR (EN, RISE)}$	Enabling		V_{DD} / 2	V_{DD} x 0.7	V
ENABLE Threshold Falling	$V_{THR (EN, FALL)}$	Disabling	V_{DD} x 0.3	V_{DD} / 2		V
Enable Time	t_{EN}	ENABLE high ≥ READY		350	420	µs
Disable Time	t_{DIS}	ENABLE low ≥ READY		25	50	ns
Bus Idle Time	t_{IDLE}			350	430	µs
SDAIN to READY After STOP	t_{STOP}	(Note 2)		0.7	1.0	µs
SCLOUT/SDAOUT to READY	t_{READY}			0.6	1.0	µs

Table 5-3. I²C Bus Pins Characteristics

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input/Output Offset Voltage	V_{OS}			75		mV
ENABLE Input Current	I_{EN}	ENABLE between V_{SS} and V_{DD}	-1		+1	µA
I²C Capacitance (Note 3)	C_{BUS}	Applies to SCLIN, SDAIN, SCLOUT, SDAOUT pins; signals between -0.5V and 3.65V, V_{DD} between 0V and 5.5V		3	10	pF
Leakage Current on I²C Pins	$I_{OFF\ (BUS)}$	ENABLE = V_{SS} or V_{DD} < $V_{DD,UV}$	-10		+10	µA
Output Low Open-Drain Outputs	$V_{OL\ (OD)}$	Applies to READY and $\overline{FAULT}$ pins, I_{PULLUP} = 3mA			0.4	V
I²C Bus V_{OUTLOW}	$V_{OL\ (BUS)}$	I_{IN} = -3mA		0.3	0.5	V
I²C Bus Clock		See Table 5-5				
Bus Stuck Low Timer	t_{STUCK}	SDAOUT or SCLOUT = low	15	30	45	ms
Transient-Boosted Pullup Current	I_{PULL}	Low to high transition on SDA, SCL pins; V_{DD} = 0.3V	1			mA

Table 5-4. Device Control Pins Characteristics

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Input Threshold Voltage	$V_{THR\ (LOG)}$	Applies to SBDIS, SBCLK, ASR, ACOE, and ACIE inputs	1.6	1.8	2.0	V
Logic Input Hysteresis	V_{HYS}	Any logic input pin except ENABLE (Note 3)		50		mV
ENABLE Input Threshold		See Table 5-2				
Input Leakage	I_{IL}	Applies to SBDIS, SBCLK, ASR, ACOE, ACIE, and ENABLE	-10		+10	µA
Leakage Current on Open-Drain Outputs	$I_{OFF\ (OD)}$	Applies to READY and $\overline{FAULT}$ pins, ENABLE = V_{SS}	-10		+10	µA
Lead Capacitance	C_{IO}	READY, ENABLE, SBDIS, SBCLK, ASR, ACOE, ACIE, $\overline{FAULT}$ pins			10	pF

Table 5-5. Timing Characteristics

(V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency	f_{BUS}		0		400	kHz
Bus Free Time Between START and STOP Condition	f_{BUF}	(Note 3)	1.3			µs
Hold Time After Repeated START Condition	$t_{HD,START}$	(Note 3)	0.6			µs
Repeated START Condition Setup Time	$t_{SU,START}$	(Note 3)	0.6			µs
STOP Condition Setup Time	$t_{SU,STOP}$	(Note 3)	0.8			µs
Clock Low Period	t_{LOW}	(Note 3)	1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Clock-Data Fall Time	t_F	(Note 4)	$20 + 0.1C_B$		250	ns
Clock-Data Rise Time	t_R	(Notes 3, 4)	$20 + 0.1C_B$			ns

Note 1: Applies over full operational temperature range.

Note 2: Delays that can occur after enable and/or idle time have passed.

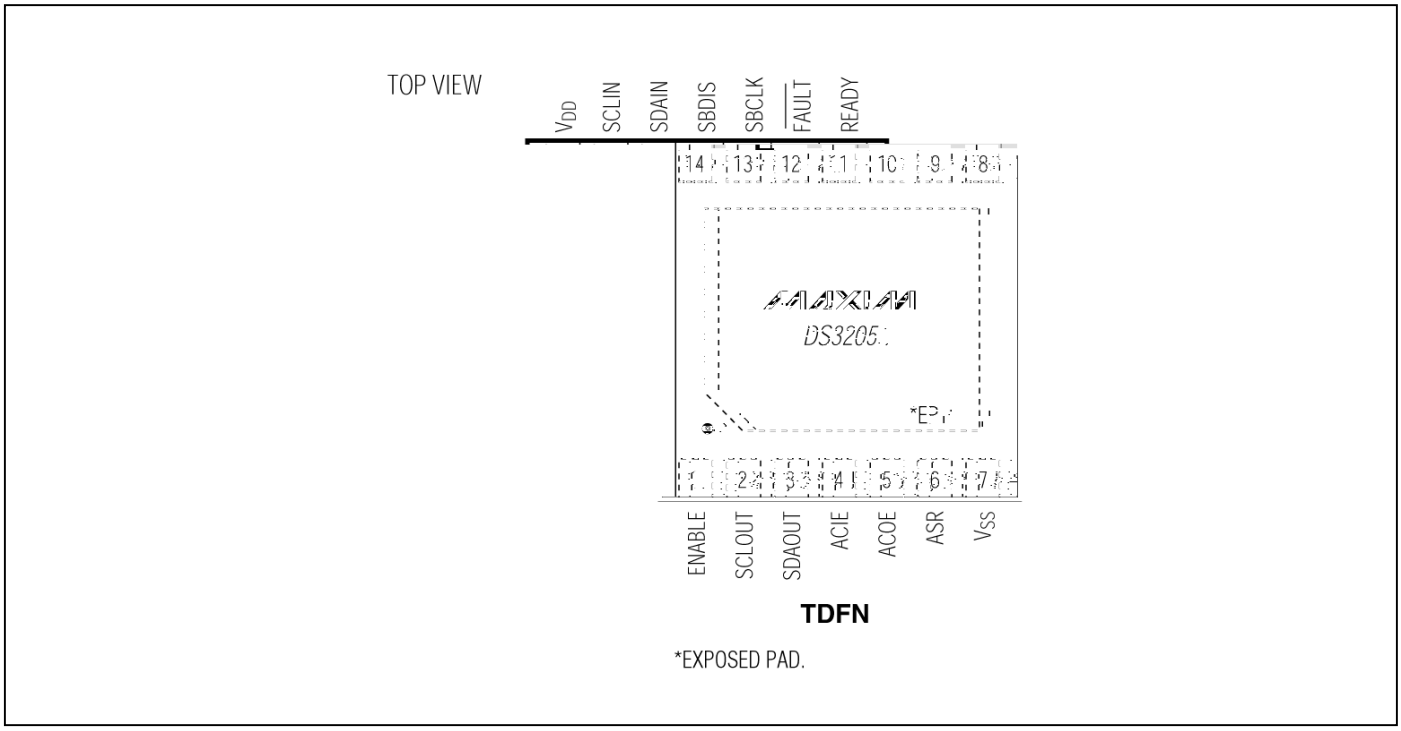
Note 3: Guaranteed by design. Not production tested.

Note 4: C_B = Total capacitance of one bus line (pF).

Note 5: I_{PULL} varies with temperature and voltage.

6. Pin Configuration

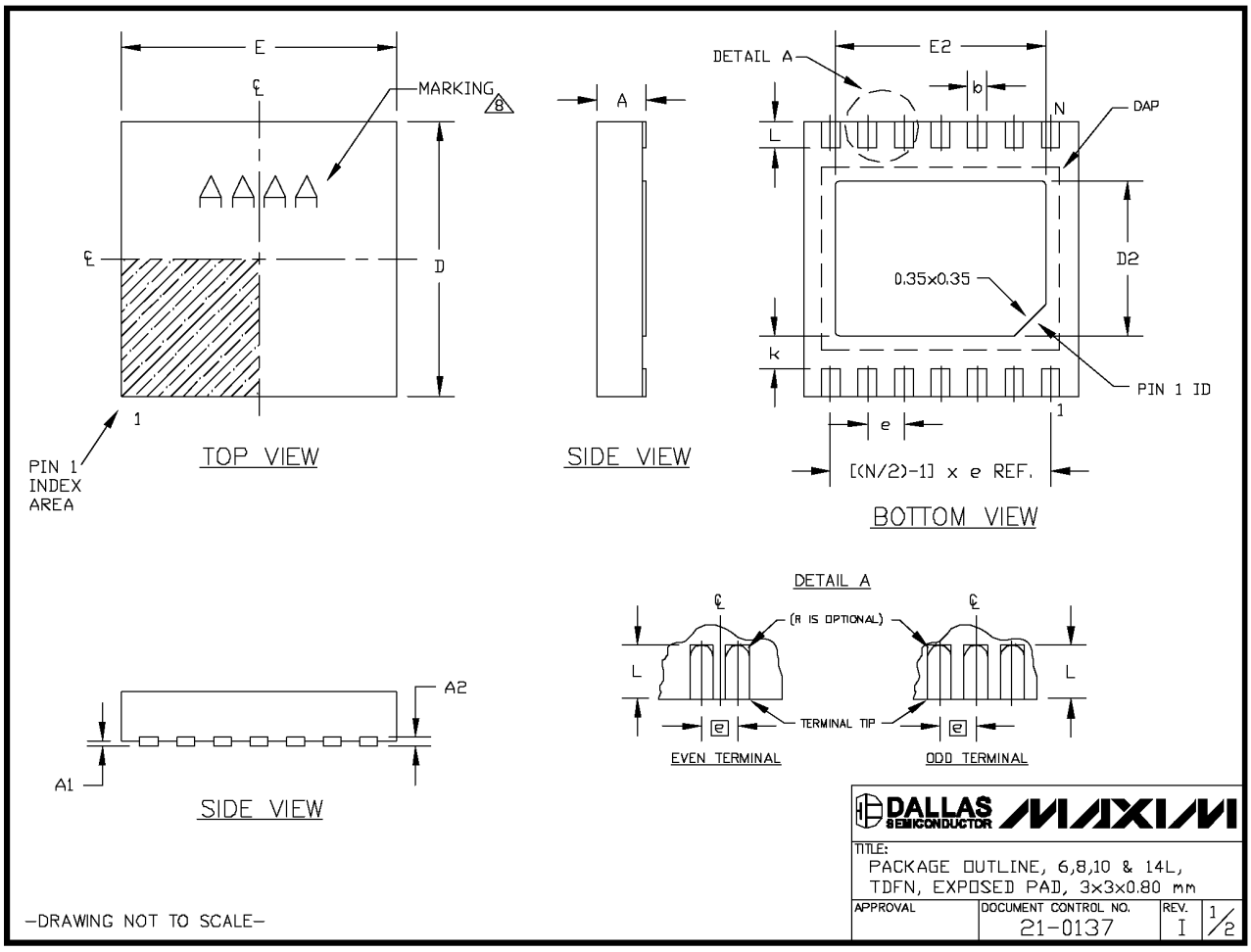
Figure 6-1. 14-Pin TDFN with Exposed Pad Pin Configuration



7. Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information. Go to www.maxim-ic.com/packages.)

7.1 14-Pin TDFN with Exposed Pad (21-0137)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L,
TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

-DRAWING NOT TO SCALE-

8. Thermal Information

Table 8-1. Thermal Properties—14-Pin TDFN Package

PARAMETER	VALUE
Target Ambient Temperature Range	-40°C to +85°C
Theta J (Die Junction Temperature Range)	-40°C to +125°C

9. Data Sheet Revision History

REVISION DATE	DESCRIPTION	PAGES CHANGED
111607	Initial data sheet release.	—

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600