National Semiconductor

November 5, 2007

DS32EV100
Programmable Single Equalizer

General Description

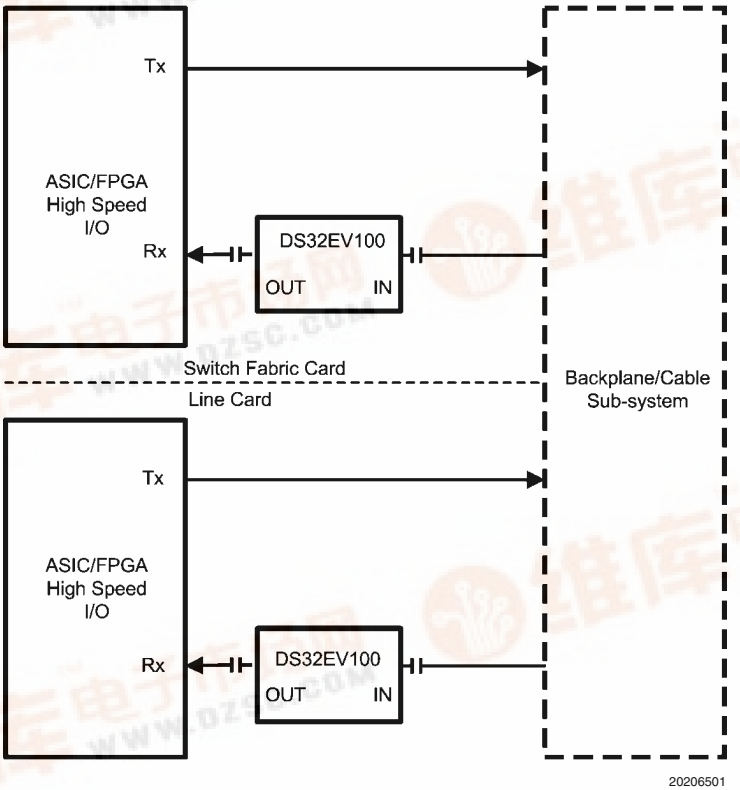
The DS32EV100 programmable equalizer provides compensation for transmission medium losses and reduces the medium-induced deterministic jitter for NRZ data channel. The DS32EV100 is optimized for operation up to 3.2 Gbps for both cables and FR4 traces. The equalizer channel has eight levels of input equalization that can be programmed by three control pins.

The equalizer supports both AC and DC-coupled data paths for long run length data patterns such as PRBS-31, and balanced codes such as 8b/10b. The device uses differential current-mode logic (CML) inputs and outputs, and is available in a 3 mm x 4 mm 14-pin leadless LLP package. Power is supplied from either a 2.5V or 3.3V supply.

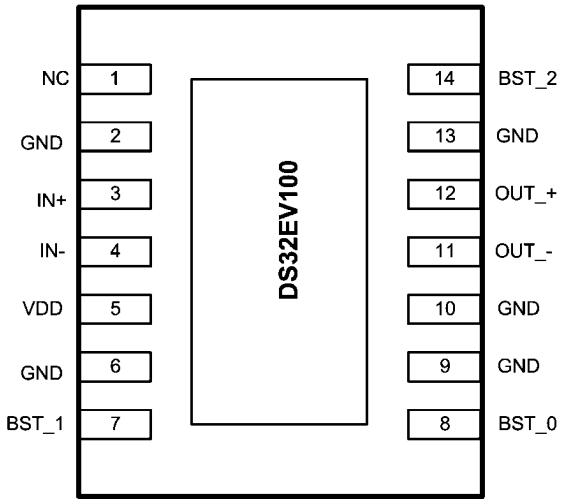
Features

- Equalizes up to 14 dB loss at 3.2 Gbps
- 8 levels of programmable equalization
- Operates up to 3.2 Gbps with 40" FR4 traces
- 0.12 UI residual deterministic jitter at 3.2 Gbps with 40" FR4 traces
- Single 2.5V or 3.3V power supply
- Supports AC or DC-Coupling with wide input common-mode
- Low power consumption: 100 mW Typ at 2.5V
- Small 3 mm x 4 mm 14-pin LLP package
- >8 kV HBM ESD
- -40 to 85°C operating temperature range

Simplified Application Diagram



Pin Diagram



Top View
3mm x 4mm 14-Pin LLP Package
Order number DS32EV100
See NS Package Number SQA14A

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
IN– IN+	4 3	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN+ and IN–.
OUT– OUT+	11 12	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT+ to V_{DD} and OUT– to V_{DD}.
EQUALIZATION CONTROL			
BST_2 BST_1 BST_0	14 7 8	I, CMOS	BST_2, BST_1, and BST_0 select the equalizer strength for EQ channel 1. BST_2 is internally pulled high. BST_1 and BST_0 are internally pulled low.
POWER			
V_{DD}	5	Power	V_{DD} = 2.5V ±5% or 3.3V ±10%. V_{DD} pins should be tied to V_{DD} plane through low inductance path. A 0.01µF bypass capacitor should be connected between each V_{DD} pin to GND planes.
GND	2, 6, 9, 10, 13	Power	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed Pad	PAD	Power	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board.
OTHER			
RSVD	1		Reserved. Leave no Connect.

Note: I = Input, O = Output

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +4.0V
CMOS Input Voltage	−0.5V to +4.0V
CMOS Output Voltage	−0.5V to +4.0V
CML Input/Output Voltage	−0.5V to +4.0V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature Soldering, 4 sec	+260°C
ESD Rating	
HBM, 1.5 kΩ, 100 pF	>8 kV
EIAJ, 0Ω, 200 pF	>250V
Thermal Resistance, θ_{JA}, No Airflow	40 °C/W

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
$V_{DD2.5}$ to GND	2.375	2.5	2.625	V
$V_{DD3.3}$ to GND	3.0	3.3	3.6	V
Ambient Temperature	−40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2,3)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
POWER						
P	Power Supply Consumption	$V_{DD2.5}$		100	150	mW
		$V_{DD3.3}$		140	200	mW
N	Supply Noise Tolerance (Note 3)	50 Hz – 100 Hz 100 Hz – 10 MHz 10 MHz – 1.6GHz		100 40 10		mV_{P-P} mV_{P-P} mV_{P-P}
LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	$V_{DD2.5}$	1.6		V_{DD}	V
		$V_{DD3.3}$	2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −3mA, $V_{DD2.5}$	2.0			V
		I_{OH} = −3mA, $V_{DD3.3}$	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA			0.4	V
I_{IN}	Input Current	V_{IN} = V_{DD}		+1.8	+15	µA
		V_{IN} = GND	−15	0		µA
I_{IN-P}	Input Leakage Current with Internal Pull-Down/Up Resistors	V_{IN} = V_{DD}, with internal pull-down resistors		+95		µA
		V_{IN} = GND, with internal pull-up resistors	−20			µA
CML RECEIVER INPUTS (IN+, IN−)						
V_{INTRE}	Input Threshold Voltage	Differential measurement at point B (FIgure 1)		120		mV_{P-P}
V_{IN}	Input Voltage Swing	AC-Coupled or DC-Coupled Requirement (Figure 1)	400		1600	mV_{P-P}
V_{DDTX}	Supply Voltage of Transmitter to EQ	DC-Coupled Requirement	1.6		V_{DD}	V
V_{ICMDC}	Input Common-Mode Voltage	DC-Coupled Requirement Differential measurement at point A (Figure 1) (Note 7)	V_{DDTX}-0.8		V_{DDTX}-0.2	V
R_{LI}	Differential Input Return Loss	100 MHz – 1.6 GHz, with fixture's effect de-embedded		10		dB

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
R_{IN}	Input Resistance	Differential Across IN+ and IN-	85	100	115	Ω
CML OUTPUTS (OUT+, OUT–)						
V_O	Output Voltage Swing	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled (Figure 2)	550		725	mV_{P-P}
V_{OCM}	Output Common-Mode Voltage	Single-ended measurement DC-Coupled with 50Ω terminations (Note 7)	V_{DD}-0.2		V_{DD}-0.1	V
t_R, t_F	Transition Time	20% to 80% of differential output voltage, measured within 1” from output pins. (Figure 2) (Note 7)	20		60	ps
R_O	Output Resistance	Single-ended to V_{DD}	42	50	58	Ω
R_{LO}	Differential Output Return Loss	100 MHz – 1.6 GHz, with fixture’s effect de-embedded. IN+ = static high.		10		dB
t_{PLHD}	Differential Low to High Propagation Delay	Propagation delay measurement at 50% VO between input to output, 100 Mbps (Figure 3) (Note 7)		240		ps
t_{PHLD}	Differential High to Low Propagation Delay			240		ps
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 3.2 Gbps	40” of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern (Note 5, 6)		0.12	0.2	UI_{P-P}
DJ2	Residual Deterministic Jitter at 2.5 Gbps	40” of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern (Note 5, 6)		0.1	0.16	UI_{P-P}
DJ3	Residual Deterministic Jitter at 1 Gbps	40” of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern (Note 5, 6)		0.05		UI_{P-P}
RJ	Random Jitter	(Note 7, 8)		0.5		ps_{rms}

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are guaranteed for a junction temperature range of –40°C to +125°C. Models are validated to Maximum Operating Voltages only.

Note 2: Typical values represent most likely parametric norms at V_{DD} = 3.3V or 2.5V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Note 5: Specification is guaranteed by characterization at optimal boost setting and is not tested in production.

Note 6: Deterministic jitter is measured at the differential outputs (point C of Figure 1), minus the deterministic jitter before the test channel (point A of Figure 1). Random jitter is removed through the use of averaging or similar means.

Note 7: Measured with clock-like {11111 00000} pattern.

Note 8: Random jitter contributed by the equalizer is defined as sqrt ($J_{OUT}^2 - J_{IN}^2$). J_{OUT} is the random jitter at equalizer outputs in ps_{rms}, see point C of Figure 1; J_{IN} is the random jitter at the input of the equalizer in ps_{rms}, see point B of Figure 1.

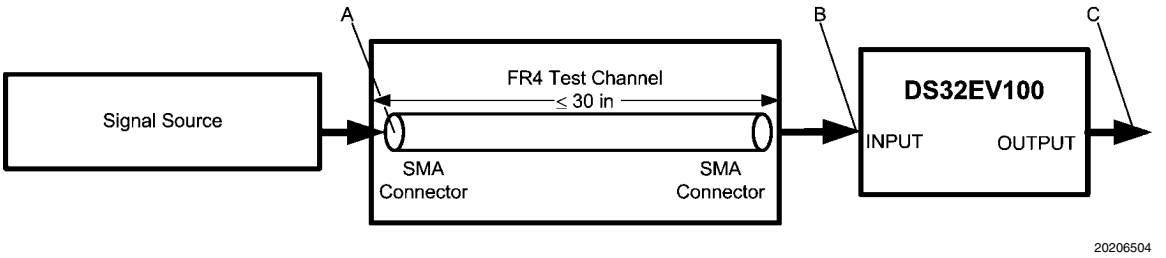


FIGURE 1. Test Setup Diagram

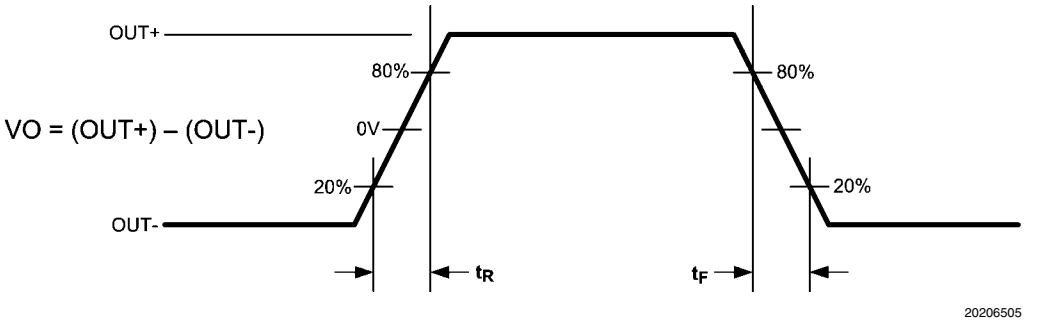


FIGURE 2. CML Output Transition Times

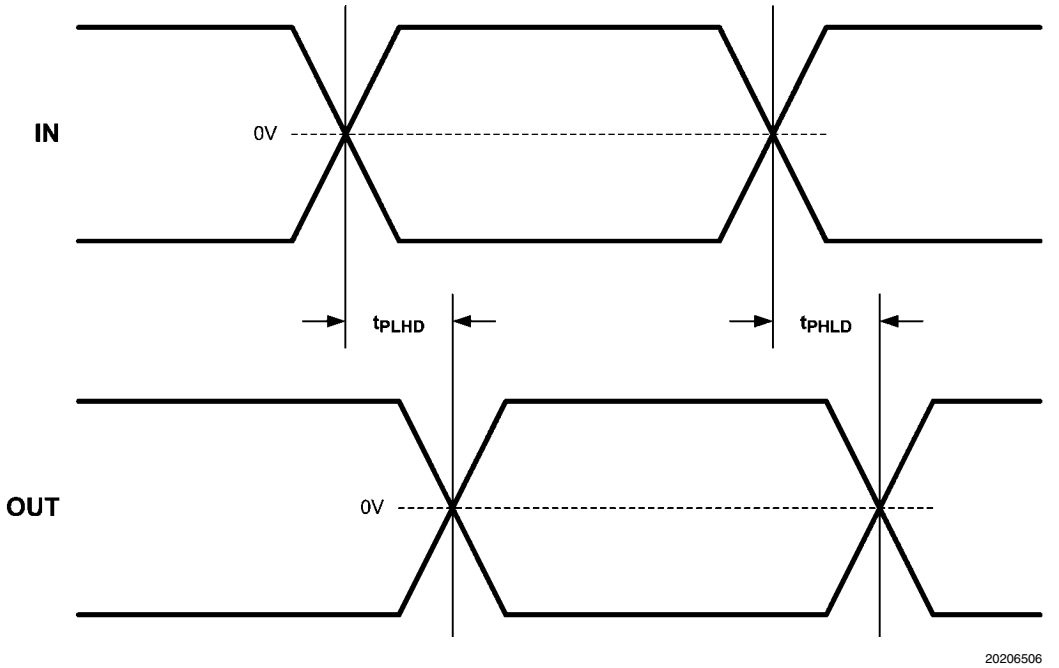


FIGURE 3. Propagation Delay Timing Diagram

DS32EV100 Application Information

The DS32EV100 is a programmable equalizer optimized for operation up to 3.2 Gbps for backplane and cable applications. The equalizer channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a CML driver as shown in Figure 4.

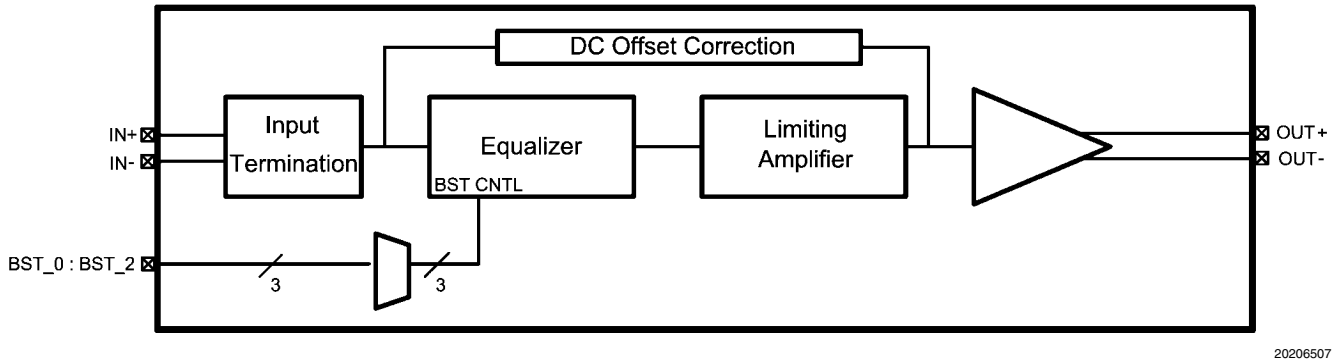


FIGURE 4. Simplified Block Diagram

EQUALIZER BOOST CONTROL

The equalizer channel supports eight programmable levels of equalization boost, and is controlled by the Boost Set pins (BST_[2:0]) in accordance with Table 1. The eight levels of boost settings enables the DS32EV100 to address a wide range of media loss and data rates.

TABLE 1. EQ Boost Control Table

6 mil Microstrip FR4 Trace Length (in)	24 AWG Twin-AX Cable Length (m)	Channel Loss 1.6 GHz (dB)	[BST_2, BST_1, BST_0]
0	0	0	0 0 0
5	2	3	0 0 1
10	3	6	0 1 0
15	4	7	0 1 1
20	5	8	1 0 0
25	6	10	1 0 1
30	7	12	1 1 0
40	10	14	1 1 0

GENERAL RECOMMENDATIONS

The DS32EV100 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high-speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route CML lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the CML signals away from other signals and noise sources on the printed circuit board. See AN-1187 for additional information on LLP packages.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS32EV100 is provided with an adequate power supply. First, the supply (V_{DD}) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS32EV100. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS32EV100.

Typical Performance Eye Diagrams and Curves

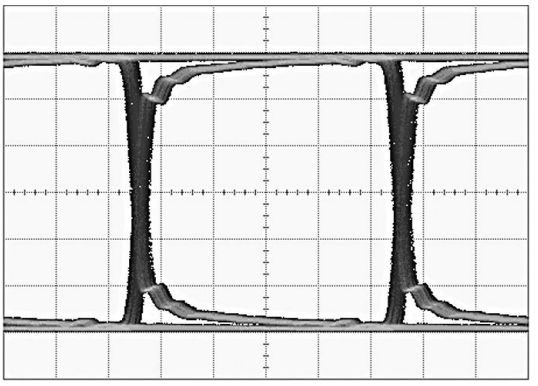


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Figure 5. Equalized Signal (40 in FR4, 1 Gbps, PRBS 7, 0x07 Setting)

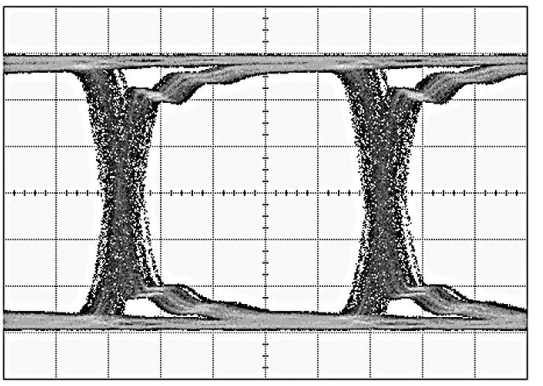

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Figure 6. Equalized Signal (40 in FR4, 2.5 Gbps, PRBS 7, 0x07 Setting)

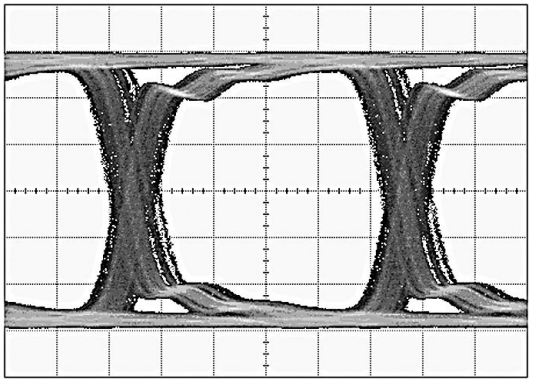

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Figure 7. Equalized Signal (40 in FR4, 3.2Gbps, PRBS 7, 0x07 Setting)

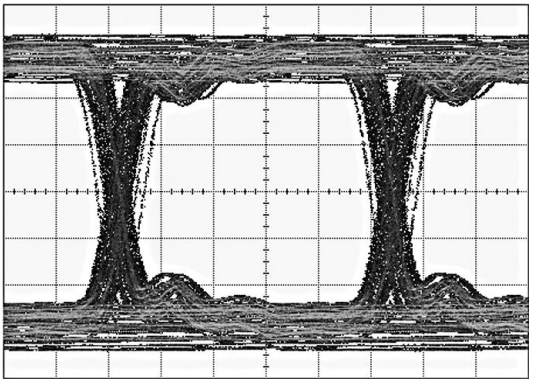

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Figure 8. Equalized Signal (10m 24 AWG Twin-AX Cable, 3.2 Gbps, PRBS 7, 0x07 Setting)

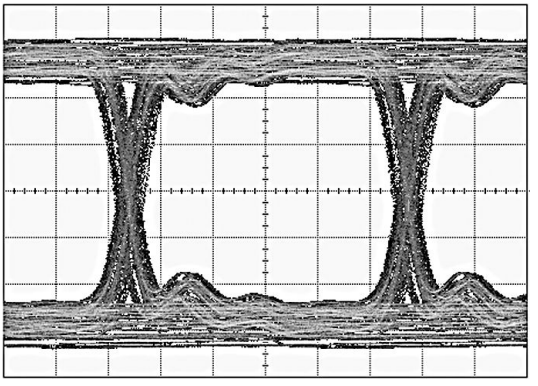

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Figure 9. Equalized Signal (32 in Tyco XAUI Backplane, 3.125 Gbps, PRBS 7, 0x07 Setting

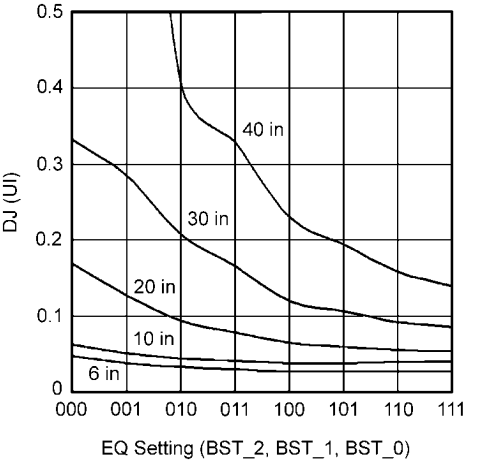

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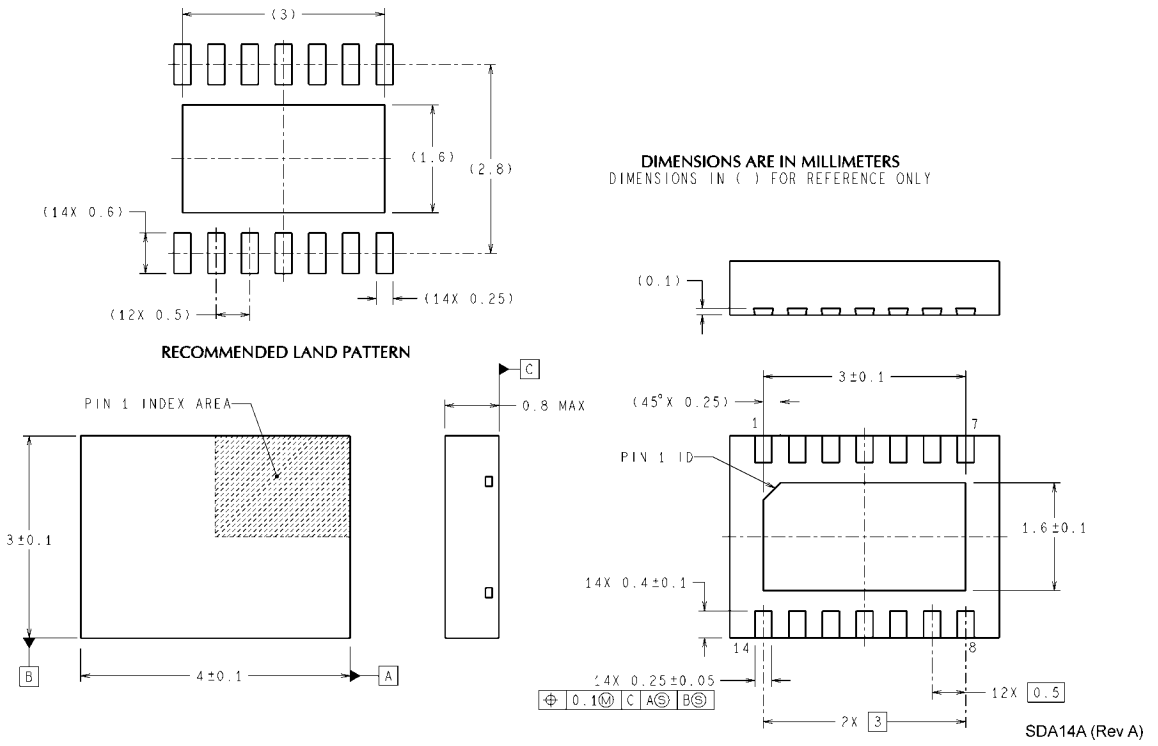
Figure 10. DJ vs. EQ Setting (3.2 Gbps)

Physical Dimensions inches (millimeters) unless otherwise noted



14-Pin Leadless LLP Package
Order Number DS32EV100
NS Package Number SDA14A

Notes

Notes

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