National Semiconductor

February 2005

DS36C200I
Dual High Speed Bi-Directional Differential Transceiver

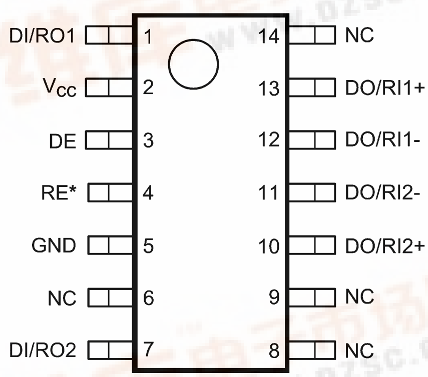
General Description

The DS36C200I is a dual transceiver device optimized for high data rate and low power applications. This device provides a single chip solution for a dual high speed bi-directional interface. Also, both control pins may be routed together for single bit control of datastreams. Both control pins are adjacent to each other for ease of routing them together. The DS36C200I is compatible with IEEE 1394 physical layer and may be used as an economical solution with some considerations. Please reference the application information on 1394 for more information. The device is in a 14-lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 210 mV. The receiver offers ±100 mV threshold sensitivity, in addition to common-mode noise protection.

Features

- Industrial Temperature Range -40˚C to +85˚C
- Optimized for DSS to DVHS interface link
- Compatible IEEE 1394 signaling voltage levels
- Operates above 100 Mbps
- Bi-directional transceivers
- 14-lead SOIC and TSSOP packages
- Ultra low power dissipation
- ±100 mV receiver sensitivity
- Low differential output swing typical 210 mV
- High impedance during power off

Connection Diagrams



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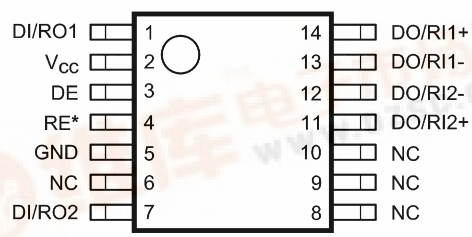
Note: * denotes active LOW pin

Order Number DS36C200IMA
See NS Package Number M14A



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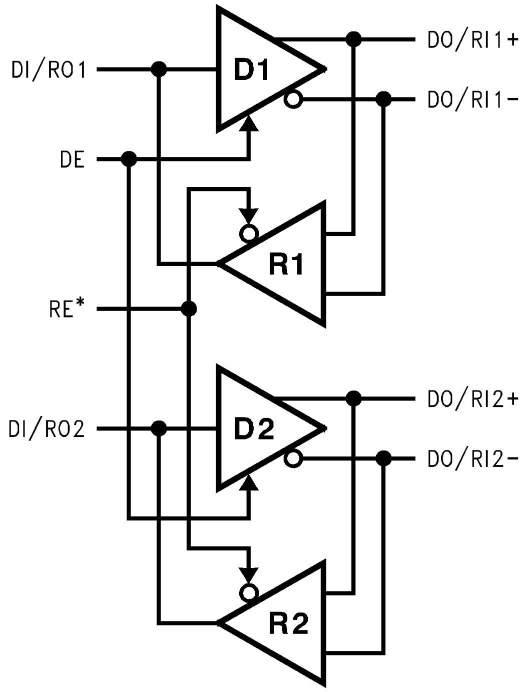
Note: * denotes active LOW pin

Order Number DS36C200IMT
See NS Package Number MTC14

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Enable Input Voltage	
(DE, RE*)	−0.3V to (V_{CC} + 0.3V)
Voltage (DI/RO)	−0.3V to +5.9V
Voltage (DO/RI±)	−0.3V to +5.9V
Package Thermal Resistance Ratings (Note 8)	
M14A (θ_{J-A})	105˚C/W
M14A (θ_{J-C})	25˚C/W
MTC14 (θ_{J-A})	135˚C/W
MTC14 (θ_{J-C})	35˚C/W
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range	
(Soldering, 4 sec.)	+260˚C
ESD Rating (Note 4)	
(HBM, 1.5 kΩ, 100 pF)	≥ 3.5 kV
(EIAJ, 0 Ω, 200 pF)	≥ 300V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	0		2.4	V
Operating Free Air Temperature (T_A)	-40	25	+85	˚C

Electrical Characteristics (Notes 2, 3, 7)

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS (RE* = V_{CC})							
V_{OD}	Output Differential Voltage	R_L = 55Ω, (*Figure 1*)	DO+, DO−	172	210	285	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	4	35	mV
V_{OH}	Output High Voltage				1.36		V
V_{OL}	Output Low Voltage				1.15		V
V_{OS}	Offset Voltage			1.0	1.25	1.6	V
ΔV_{OS}	Offset Magnitude Change			0	5	25	mV
I_{OZD}	TRI-STATE Leakage	V_{OUT} = V_{CC} or GND		−10	±1	+10	µA
I_{OXD}	Power-Off Leakage	V_{OUT} = 5.5V or GND, V_{CC} = 0V		−10	±1	+10	µA
I_{OSD}	Output Short Circuit Current	V_{OUT} = 0V			−4	−9	mA
DIFFERENTIAL RECEIVER CHARACTERISTICS (DE = GND)							
V_{TH}	Input Threshold High	V_{CM} = 0V to 2.3V	RI+, RI−			+100	mV
V_{TL}	Input Threshold Low			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V or 0V		−10	±1	+10	µA
V_{OH}	Output High Voltage	I_{OH} = −400 µA	RO	3.8	4.9		V
		Inputs Open		3.8	4.9		V
		Inputs Terminated, R_t = 55Ω		3.8	4.9		V
		Inputs Shorted, V_{ID} = 0V			4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA, V_{ID} = −200 mV			0.1	0.4	V
I_{OSR}	Output Short Circuit Current	V_{OUT} = 0V		−15	−60	−100	mA
DEVICE CHARACTERISTICS							
V_{IH}	Input High Voltage		DI, DE RE*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V			±1	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{CCD}	Power Supply Current	No Load, DE = RE* = V_{CC}	V_{CC}		3	7	mA
		R_L = 55Ω, DE = RE* = V_{CC}			11	17	mA
I_{CCR}		DE = RE* = 0V			6	10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and V_{ID}.

Note 3: All typicals are given for V_{CC} = +5.0V and T_A = +25˚C.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 3.5 kV

Electrical Characteristics (Notes 2, 3, 7) (Continued)

EIAJ (0Ω, 200 pF) ≥ 300V

Note 5: C_L includes probe and fixture capacitance.

Note 6: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r ≤ 1 ns, t_f ≤ 1 ns (0%–100%).

Note 7: The DS36C200I is a current mode device and will meet the datasheet specifications only with a resistive load applied to the driver outputs.

Note 8: Package Thermal Resistance Ratings are for 2-Layer, 2 ounce Cu, FR-14, printed circuit board, tested per JEDEC.

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 5, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 55Ω, C_L = 10 pF (*Figure 2* and *Figure 3*)	1.0	2.5	5.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	2.6	5.5	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	0.1	2	ns
t_{TLH}	Transition Time Low to High		0	0.5	2	ns
t_{THL}	Transition Time High to Low		0	0.5	2	ns
t_{PHZ}	Disable Time High to Z	R_L = 55Ω (*Figure 4* and *Figure 5*)	0.3	5	20	ns
t_{PLZ}	Disable Time Low to Z		0.3	5	20	ns
t_{PZH}	Enable Time Z to High		0.3	10	30	ns
t_{PZL}	Enable Time Z to Low		0.3	10	30	ns
DIFFERENTIAL RECEIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 10 pF, V_{ID} = 200 mV (*Figure 6* and *Figure 7*)	1.5	5	10	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	4.6	10	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	0.4	3	ns
t_r	Rise Time		0	1.5	7	ns
t_f	Fall Time		0	1.5	7	ns
t_{PHZ}	Disable Time High to Z	C_L = 10 pF (*Figure 8* and *Figure 9*)	1	5	20	ns
t_{PLZ}	Disable Time Low to Z		1	5	20	ns
t_{PZH}	Enable Time Z to High		0.3	10	30	ns
t_{PZL}	Enable Time Z to Low		0.3	10	30	ns

Parameter Measurement Information

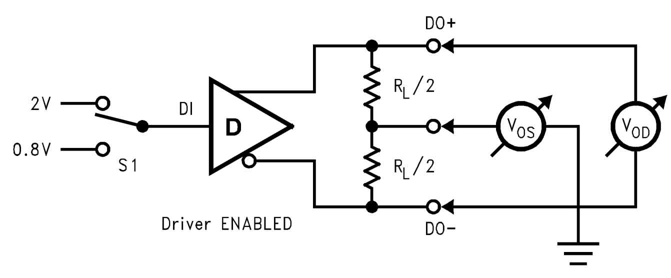


FIGURE 1. Differential Driver DC Test Circuit

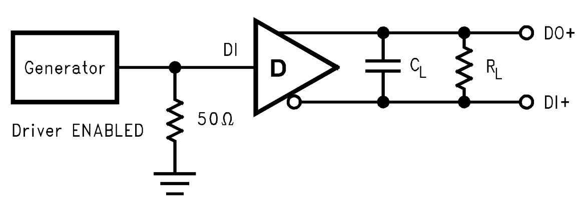


FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)

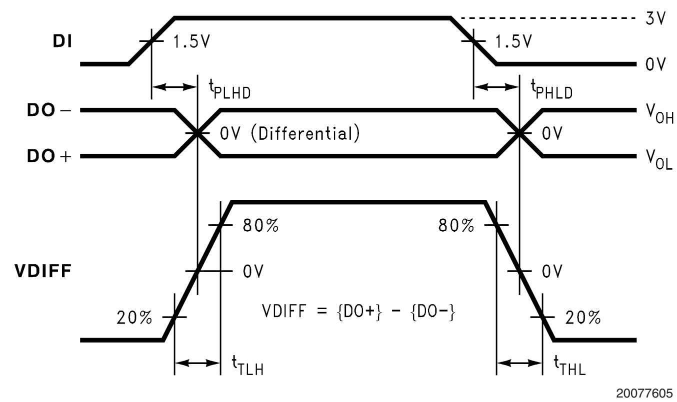


FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

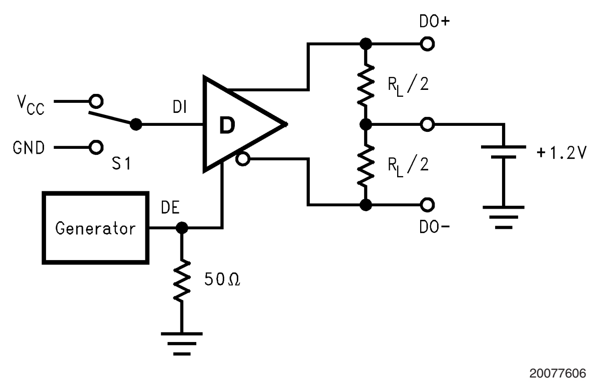


FIGURE 4. Driver TRI-STATE Delay Test Circuit

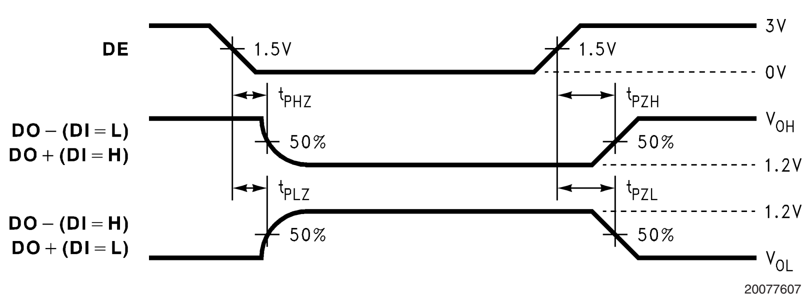


FIGURE 5. Driver TRI-STATE Delay Waveforms

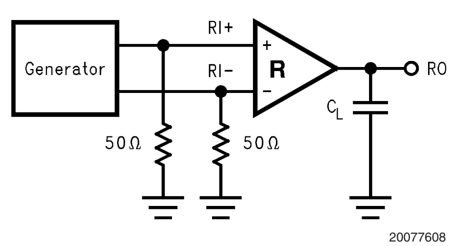


FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)

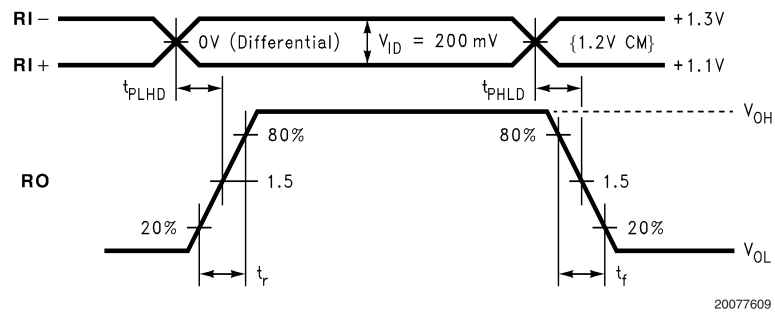


FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

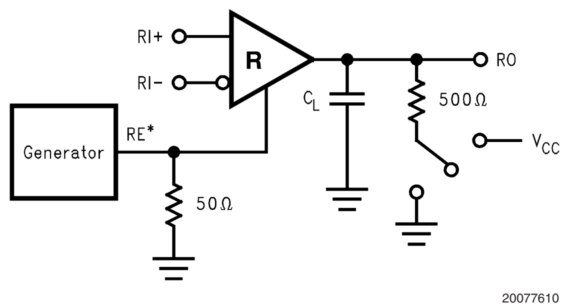


FIGURE 8. Receiver TRI-STATE Delay Test Circuit

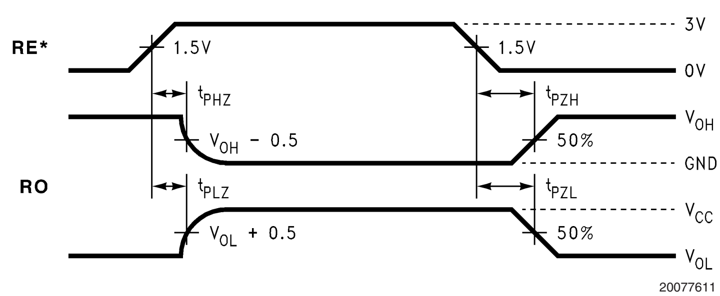


FIGURE 9. Receiver TRI-STATE Delay Waveforms

Application Information

TRUTH TABLES

The DS36C200I has two enable pins DE and RE*, however, the driver and receiver should never be enabled simultaneously. Enabling both could cause multiple channel contention between the receiver output and the driving logic. It is recommended to route the enables together on the PC board. This will allow a single bit [DE/RE*] to control the chip. This DE/RE* bit toggles the DS36C200I between Receive mode and Transmit mode. When the bit is asserted HIGH the device is in Transmit mode. When the bit is asserted LOW the device is in Receive mode. The mode determines the function of the I/O pins: DI/RO, DO/RI+, and DO/RI−.Please note that some of the pins have been identified by its function in the corresponding mode in the three tables below. For example, in Transmit mode the DO/RI+ pin is identified as DO+. This was done for clarity in the tables only and should not be confused with the pin identification throughout the rest of this document. Also note that a logic low on the DE/RE* bit corresponds to a logic low on both the DE pin and the RE* pin. Similarly, a logic high on the DE/RE* bit corresponds to a logic high on both the DE pin and the RE* pin.

Receive Mode

Input(s)		Input/Output	
DE	**RE***	**[RI+] − [RI−]**	**RO**
L	L	> +100 mV	H
L	L	< −100 mV	L
L	L	100 mV > & > −100 mV	X
L	H	X	Z

Application Information (Continued)

Transmit Mode

Input(s)		Input/Output		
DE	**RE***	**DI**	**DO+**	**DO−**
H	H	L	L	H
H	H	H	H	L
H	H	2 > & > 0.8	X	X

Input(s)		Input/Output		
DE	**RE***	**DI**	**DO+**	**DO−**
L	H	X	Z	Z

H = Logic high level
L = Logic low level
X = Indeterminate state
Z = High impedance state

TABLE 1. Device Pin Descriptions

Pin # M14A Package	Pin # MTC14 Package	Name (In mode only)	Mode	Description
3	3	DE	Transmit	Driver Enable: When asserted low driver is disabled. And when asserted high driver is enabled.
1, 7	1, 7	DI1, DI2		TTL/CMOS driver input pins
10, 13	11, 14	DO2+, DO1+		Non-inverting driver output pin
11, 12	12, 13	DO2−, DO1−		Inverting driver output pin
4	4	RE*	Receive	Receiver Enable: When asserted low receiver is enabled. And when asserted high receiver is disabled.
1, 7	1, 7	RO1, RO2		Receiver output pin
10, 13	11,14	RI2+, RI1+		Positive receiver input pin
11, 12	12, 13	RI2−, RI1−		Negative receiver input pin
5	5	Gnd	Transmit and Receive	Ground pin
2	2	V_{CC}		Positive power supply pin, +5V ± 10%
6, 8, 9, 14	6, 8, 9, 10	NC		No Connect

IEEE 1394

The DS36C200I drives and receives IEEE 1394 physical layer signal levels. The current mode driver is capable of driving a 55Ω load with V_{OD} between 172 mV and 285 mV. The DS36C200I is not designed to work with a link layer controller IC requiring full 1394 physical layer compliancy to the standard. No clock generator, no arbitration, and no encode/decode logic is provided with this device. For a 1394 link where speed sensing, bus arbitration, and other functions are not required, a controller and the DS36C200I will provide a cost effective, high speed dedicated link. This is shown in *Figure 10*. In applications that require fully compliant 1394 protocol, a link layer controller and physical layer controller will be required as shown in *Figure 10*. The physical layer controller supports up to three DS36C200I devices (not shown).

The DS36C200I drivers are current mode drivers and intended to work with two 110Ω termination resistors in parallel with each other. The termination resistors should match the characteristic impedance of the transmission media. The drivers are current mode devices therefore the resistors are required. Both resistors are required for half duplex operation and should be placed as close to the DO/RI+ and DO/RI− pins as possible at opposite ends of the bus. However, if your application only requires simplex operation, only one termination resistor is required. In addition, note the voltage levels will vary from those in the datasheet due to different loading. Also, AC or unterminated configurations are not used with this device. Multiple node configurations are possible as long as transmission line effects are taken into account. Discontinuities are caused by mid-bus stubs, connectors, and devices that affect signal integrity.

The differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.8 mA, a minimum of 3.1 mA, and a maximum of 5.2 mA. The current mode **requires** that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 11*. The 3.8 mA loop current will develop a differential voltage of 210 mV across the 55Ω termination resistor which the receiver detects with a 110 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (210 mV – 100 mV = 110 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in *Figure 7*.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other

Application Information (Continued)

existing RS-422 drivers.

Fail-safe Feature:

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1. **Open Input Pins.** The DS36C200I is a dual transceiver device, and if an application requires only one receiver, the unused channel inputs should be left OPEN. Do not tie the receiver inputs to ground or any other voltages. The input is biased by internal high value pull up or pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output will again be in a HIGH state, even with the end of the cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable will offer better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output will remain in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

If there is more than 10mV of differential noise, the receiver may switch or oscillate. If this condition can happen in your application, you may wish to add external fail-safe resistors to create a larger noise margin. External lower value pull up and pull down resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry.

Additional information on fail-safe biasing of LVDS devices may be found in AN-1194.

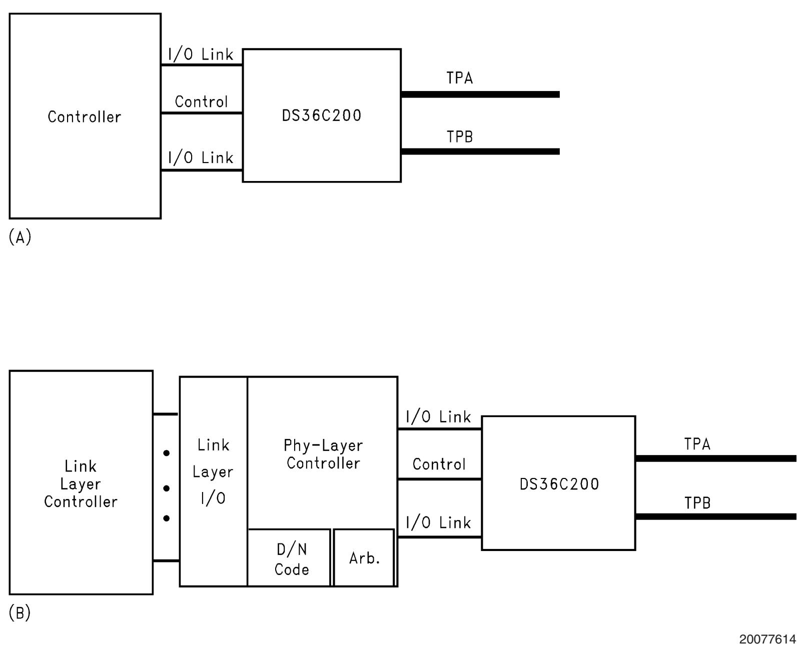


FIGURE 10. (A) Dedicated IEEE 1394 Link
(B) Full IEEE 1394 Compliant Link

Application Information (Continued)

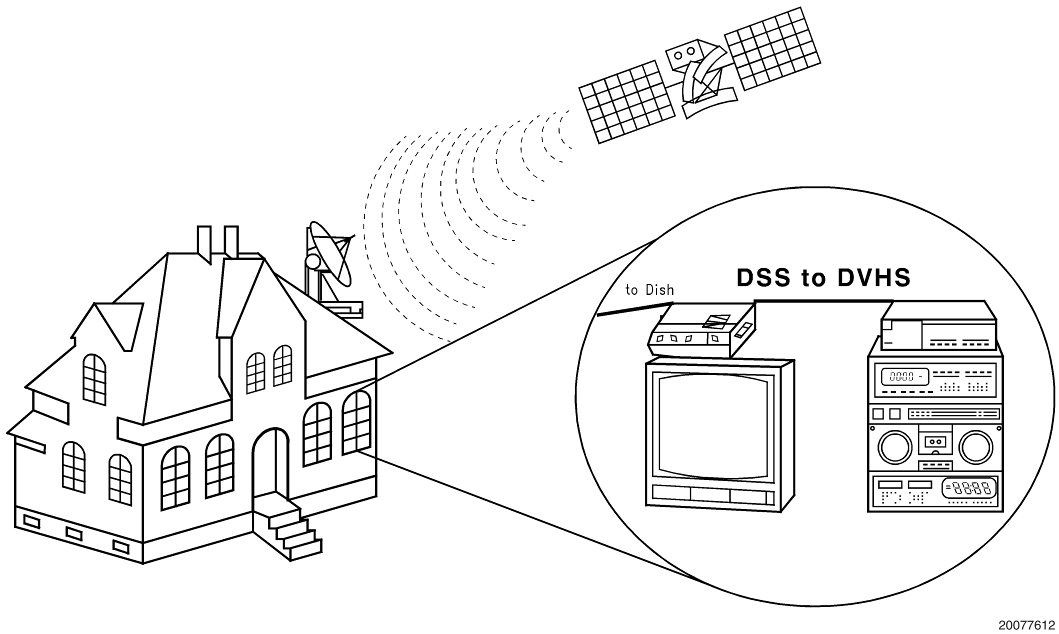


FIGURE 11. Typical in Home Application

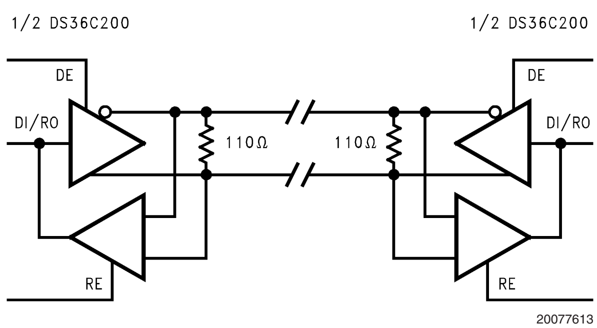
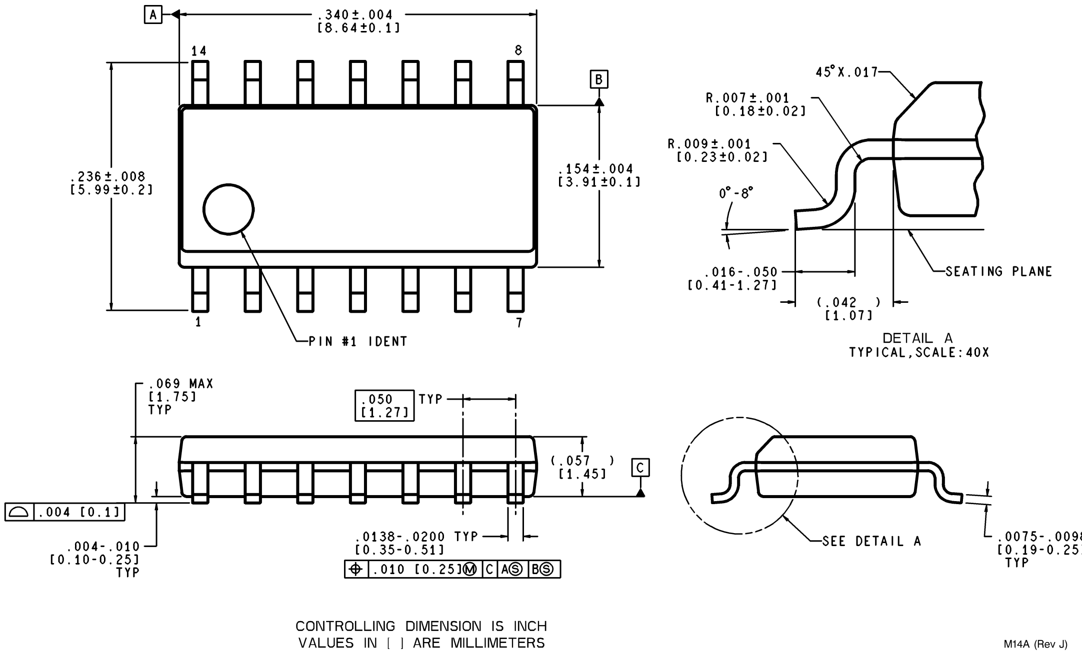


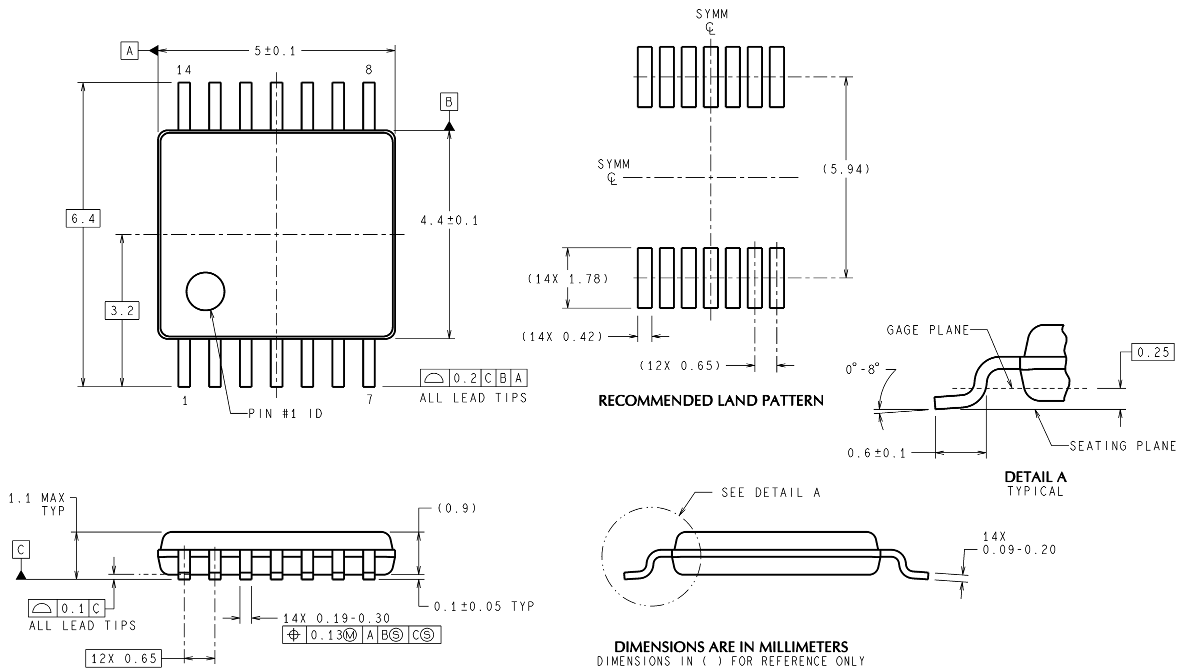
FIGURE 12. Typical Interface Connection (Note 7)

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS36C200IMA
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTC14 (Rev D)

14-Lead Molded TSSOP Package, JEDEC
Order Number DS36C200IMT
NS Package Number MTC14

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