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DS42MB100 4.25 Gbps 2:1/1:2 CML Mux/Buffer with Transmit De-Emphasis and Receive Equalization

DS42MB100

4.25 Gbps 2:1/1:2 CML Mux/Buffer with Transmit De-Emphasis and Receive Equalization

General Description

The DS42MB100 is a signal conditioning 2:1 multiplexer and 1:2 fan-out buffer designed for use in backplane redundancy or cable driving applications. Signal conditioning features include input equalization and programmable output de-emphasis that enable data communication in FR4 backplane up to 4.25 Gbps. Each input stage has a fixed equalizer to reduce ISI distortion from board traces.

All output drivers have four selectable levels of de-emphasis to compensate for transmission losses from long FR4 backplane or cable attenuation reducing deterministic jitter. The de-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs and driver outputs are internally terminated with 100Ω differential terminating resistors.

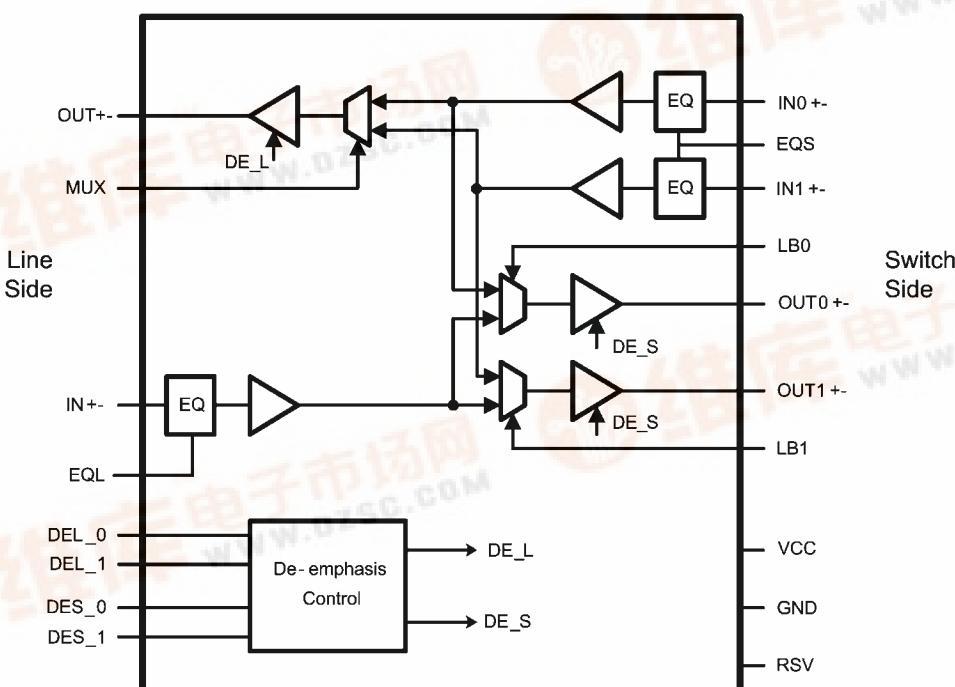
Features

- 2:1 multiplexer and 1:2 buffer
- 0.25 – 4.25 Gbps fully differential data paths
- Fixed input equalization
- Programmable output de-emphasis
- Independent de-emphasis controls
- Programmable loopback modes
- On-chip terminations
- HBM ESD rating 5.5 kV on all pins
- +3.3V supply
- Lead-less LLP-36 package
- -40°C to +85°C operating temperature range

Applications

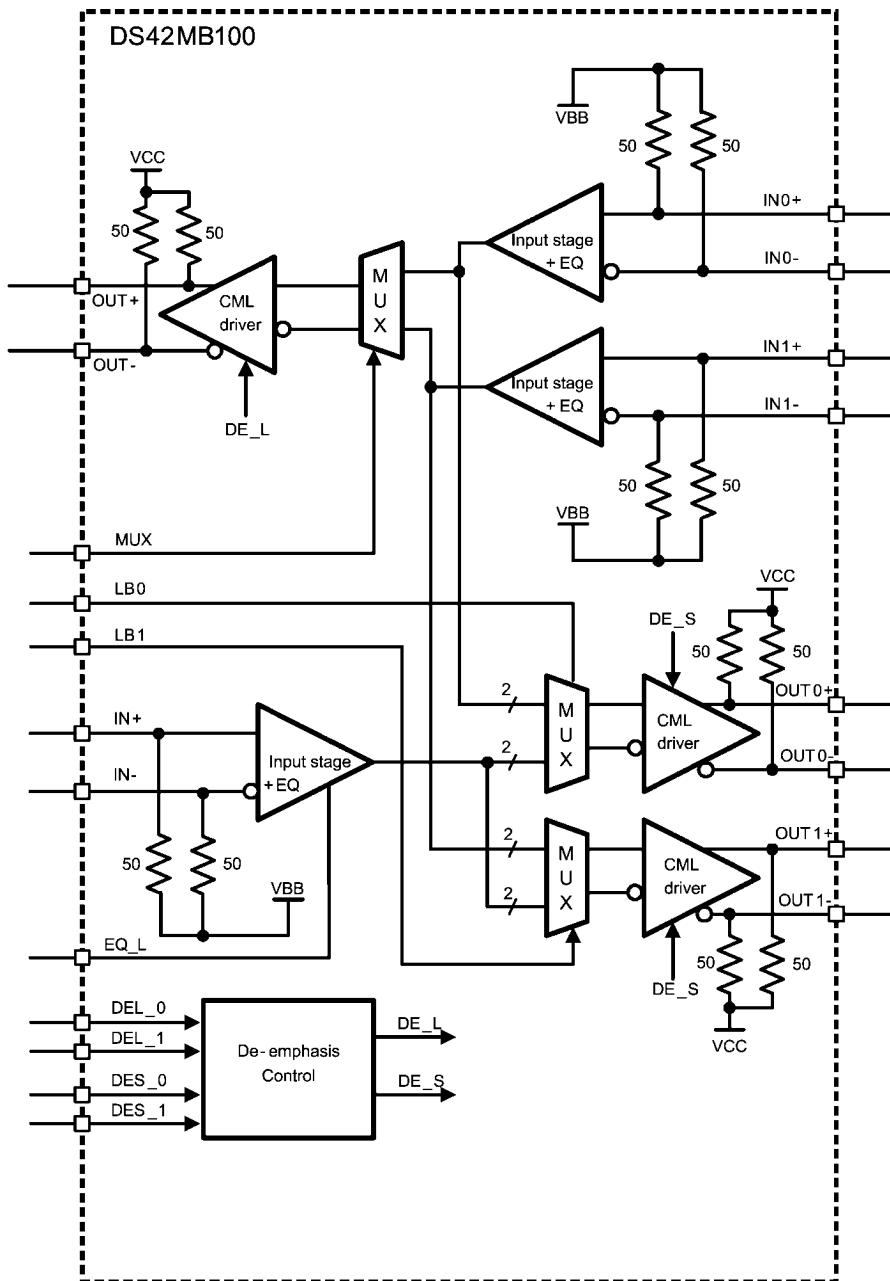
- Backplane driver or cable driver
- Redundancy and signal conditioning applications
- CPRI/OBSAI

Functional Block Diagram

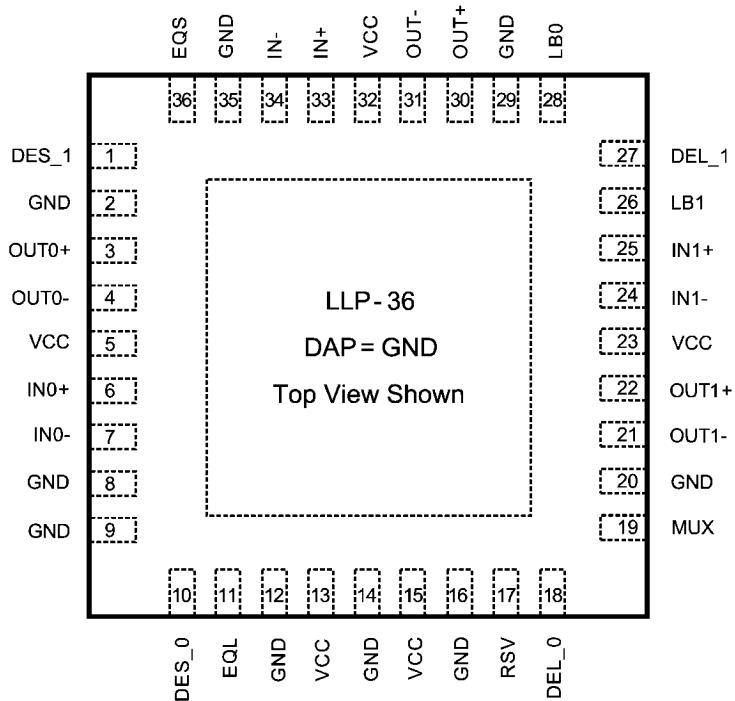


20209001

Simplified Block Diagram



Connection Diagram



20209003

Pin Descriptions

| Pin Name | Pin Number | I/O | Description |
|---|---------------------------------|-----|--|
| LINE SIDE HIGH SPEED DIFFERENTIAL IO's | | | |
| IN+ | 30 | I | Inverting and non-inverting differential inputs at the line side. IN+ and IN- have an internal 50Ω connected to an internal reference voltage. |
| IN- | 31 | | |
| OUT+ | 30 | O | Inverting and non-inverting differential outputs at the line side. OUT+ and OUT- have an internal 50Ω connected to V _{CC} . |
| OUT- | 31 | | |
| SWITCH SIDE HIGH SPEED DIFFERENTIAL IO's | | | |
| OUT0+ | 3 | O | Inverting and non-inverting differential outputs of mux0 at the switch side. OUT0+ and OUT0- have an internal 50Ω connected to V _{CC} . |
| OUT0- | 4 | | |
| OUT1+ | 22 | O | Inverting and non-inverting differential outputs of mux1 at the switch side. OUT1+ and OUT1- have an internal 50Ω connected to V _{CC} . |
| OUT1- | 21 | | |
| IN0+ | 6 | I | Inverting and non-inverting differential inputs to the mux at the switch side. IN0+ and IN0- have an internal 50Ω connected to an internal reference voltage. |
| IN0- | 7 | | |
| IN1+ | 25 | I | Inverting and non-inverting differential inputs to the mux at the switch side. IN1+ and IN1- have an internal 50Ω connected to an internal reference voltage. |
| IN1- | 24 | | |
| CONTROL (3.3V LVCMOS) | | | |
| MUX | 19 | I | A logic low at MUX_S0 selects mux_0 to switch B. MUX_S0 is internally pulled high. Default state for mux_0 is switch A. |
| EQL | 11 | | A logic low enables the EQ. EQL is internally pulled high. Default is with EQ disabled. |
| EQS | 36 | I | A logic low enables the EQ. EQS is internally pulled high. Default is with EQ disabled. |
| DEL_0 | 18 | I | DEL_0 and DEL_1 select the output de-emphasis of the line side drivers (OUT±). |
| DEL_1 | 27 | | DEL_0 and DEL_1 are internally pulled high. |
| DES_0 | 10 | I | DES_0 and DES_1 select the output de-emphasis of the switch side drivers (OUT0±, OUT1±). |
| DES_1 | 1 | | DES_0 and DES_1 are internally pulled high. |
| LB0 | 28 | I | A logic low at LB0 enables the internal loopback path from IN0± to OUT0±. LB0 is internally pulled high. |
| LB1 | 26 | I | A logic low at LB1 enables the internal loopback path from IN1± to OUT1±. LB1 is internally pulled high. |
| RSV | 17 | I | Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor. |
| POWER | | | |
| V _{CC} | 5, 13, 15, 23, 32 | P | <p>V_{CC} = 3.3V ± 5%. The maximum current consumption under worst voltage, temperature, and process variation conditions does not exceed 170mA.</p> <p>Each V_{CC} pin should be connected to the V_{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V_{CC} pin.</p> <p>It is recommended to have a 0.01 μF or 0.1 μF, X7R, size-0402 bypass capacitor from each V_{CC} pin to ground plane.</p> |
| GND | 2, 8, 9, 12, 14, 16, 20, 29, 35 | P | Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin. |
| GND | DAP | P | DAP is the metal contact at the bottom side, located at the center of the LLP package. It should be connected to the GND plane with at least 16 via to lower the ground impedance and improve the thermal performance of the package. |

Note: I = Input, O = Output, P = Power

Functional Description

The DS25MB100 is a signal conditioning 2:1 multiplexer and a 1:2 buffer designed to support port redundancy up to 2.5 Gbps. Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB of transmission loss from a short backplane trace (about 10 inches backplane). The output driver has de-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane, and minimize the deterministic jitter caused by the amplitude dis-

parity. The DS25MB100 provides four steps of user-selectable de-emphasis ranging from 0, -3, -6 and -9 dB to handle different lengths of backplane. *Figure 1* shows a driver de-emphasis waveform. The de-emphasis duration is 188ps nominal, corresponds to 0.47 bit-width at 2.5 Gbps. The de-emphasis levels of switch-side and line-side can be individually programmed.

The high speed inputs are self-biased to about 1.3V and are designed for AC coupling. The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL and CML.

TABLE 1. Logic Table For Multiplex Controls

| MUX_S0 | Mux Function |
|-------------|--------------------------------|
| 0 | MUX select switch input, IN1±. |
| 1 (default) | MUX select switch input, IN0±. |

TABLE 2. Logic Table For Loopback Controls

| LB0 | Loopback Function |
|-------------|-------------------------------------|
| 0 | Enable loopback from IN0± to OUT0±. |
| 1 (default) | Normal mode. Loopback disabled. |
| LB1 | Loopback Function |
| 0 | Enable loopback from IN1± to OUT1±. |
| 1 (default) | Normal mode. Loopback disabled. |

TABLE 3. Line-Side De-Emphasis Controls

| DEL_[1:0] | De-Emphasis Level in mV _{PP} (VODB) | De-Emphasis Level in mV _{PP} (VODPE) | De-Emphasis in dB (VODPE/VODB) | Typical FR4 Board Trace |
|---------------|--|---|--------------------------------|-------------------------|
| 0 0 | 1300 | 1300 | 0 | 10 inches |
| 0 1 | 1300 | 920 | -3 | 20 inches |
| 1 0 | 1300 | 650 | -6 | 30 inches |
| 1 1 (default) | 1300 | 461 | -9 | 40 inches |

TABLE 4. Switch-Side De-Emphasis Controls

| DES_[1:0] | De-Emphasis Level in mV _{PP} (VODB) | De-Emphasis Level in mV _{PP} (VODPE) | De-Emphasis in dB (VODPE/VODB) | Typical FR4 Board Trace |
|---------------|--|---|--------------------------------|-------------------------|
| 0 0 | 1300 | 1300 | 0 | 10 inches |
| 0 1 | 1300 | 920 | -3 | 20 inches |
| 1 0 | 1300 | 650 | -6 | 30 inches |
| 1 1 (default) | 1300 | 461 | -9 | 40 inches |

TABLE 5. EQ Controls for the Line Switch Sides

| EQL/EQS | Loopback Function |
|-------------|-------------------------------------|
| 0 | Enable equalization. |
| 1 (default) | Normal mode. Equalization disabled. |

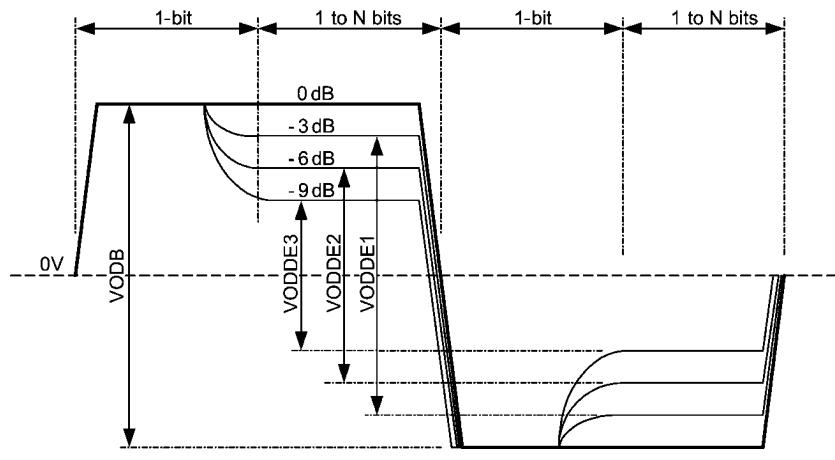


FIGURE 1. Driver De-Emphasis Differential Waveform (Showing All 4 De-Emphasis Steps)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------------------|
| Supply Voltage (V_{CC}) | -0.3V to 4V |
| CMOS/TTL Input Voltage | -0.3V to (V_{CC} + 0.3V) |
| CML Input/Output Voltage | -0.3V to (V_{CC} + 0.3V) |
| Junction Temperature | +150°C |
| Storage Temperature | -65°C to +150°C |
| Lead Temperature Soldering, 4 seconds | +260°C |
| Thermal Resistance, θ_{JA} (Note 8) | 26.2°C/W |
| Thermal Resistance, θ_{JC-top} | 3.3°C/W |

| | |
|---------------------------------|----------|
| Thermal Resistance, Φ_{JB} | 11.1°C/W |
| ESD Rating (Note 10) | |
| HBM, 1.5 kΩ, 100 pF | 6 kV |
| CDM | 1.25 kV |
| MM | 350V |

Recommended Operating Ratings

| | Min | Typ | Max | Units |
|---------------------------------------|------|-----|-------|------------------|
| Supply Voltage (V_{CC} -GND) | 3.13 | 3.3 | 3.465 | V |
| | 5 | | | |
| Supply Noise Amplitude 10 Hz to 2 GHz | | | 100 | mV _{PP} |
| Ambient Temperature | -40 | | 85 | °C |
| Case Temperature | | | 100 | °C |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|---|---|---|------|--------------|----------------|-------------------|
| LVCMOS DC SPECIFICATIONS | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{CC} + 0.3 | V |
| V_{IL} | Low Level Input Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | High Level Input Current $V_{IN} = V_{CC}$ | | -10 | | 10 | μA |
| I_{IL} | Low Level Input Current $V_{IN} = GND$ | | 75 | 94 | 124 | μA |
| R_{PU} | Pull-High Resistance | | | 35 | | kΩ |
| RECEIVER SPECIFICATIONS | | | | | | |
| V_{ID} | Differential Input Voltage Range (Note 9) | AC Coupled Differential Signal | | | | |
| | | Below 1.25 Gbps | 100 | | 1750 | mV _{P-P} |
| | | Between 1.25 Gbps–3.125 Gbps | 100 | | 1560 | mV _{P-P} |
| | | Above 3.125 Gbps | 100 | | 1200 | mV _{P-P} |
| This parameter is not tested at production. | | | | | | |
| V_{ICM} | Common Mode Voltage at Receiver Inputs | Measured at receiver inputs reference to ground. | | 1.3 | | V |
| R_{ITD} | Input Differential Termination (Note 3) | On-chip differential termination between IN+ or IN-. | 84 | 100 | 116 | Ω |
| R_{ITSE} | Input Termination (single-end) | On-chip termination IN+ or IN- to GND for frequency > 100 MHz. | | 50 | | Ω |
| DRIVER SPECIFICATIONS | | | | | | |
| V_{VODB} | Output Differential Voltage Swing without De-Emphasis (Note 4) | $R_L = 100Ω \pm 1\%$ $DES_1=DES_0=0$ $DEL_1=DEL_0=0$ Driver de-emphasis disabled. Running K28.7 pattern at 4.25 Gbps. See <i>Figure 5</i> for test circuit. | 1100 | 1300 | 1500 | mV _{P-P} |
| | | | | | | |
| V_{VDE} | Output De-Emphasis Voltage Ratio $20 \times \log(V_{ODP}/V_{VODB})$ | $R_L = 100Ω \pm 1\%$ Running K28.7 pattern at 4.25 Gbps $DEx_{[1:0]}=00$ $DEx_{[1:0]}=01$ $DEx_{[1:0]}=10$ $DEx_{[1:0]}=11$ x=S for switch side de-emphasis control x=L for line side de-emphasis control See <i>Figure 1</i> on waveform. See <i>Figure 5</i> for test circuit. | | 0 | | dB |
| | | | | -3 | | dB |
| | | | | -6 | | dB |
| | | | | -9 | | dB |

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|---------------------------|--|---|------|-----------------|-------------|-------------------------|
| T_{DE} | De-Emphasis Width | Tested at -9 dB de-emphasis level, DEx[1:0]=11 x=S for switch side de-emphasis control x=L for line side de-emphasis control See <i>Figure 4</i> on measurement condition. | 125 | 188 | 250 | ps |
| R_{OTSE} | Output Termination (Note 3) | On-chip termination from OUT+ or OUT- to V_{CC} | 42 | 50 | 58 | Ω |
| R_{OTD} | Output Differential Termination | On-chip differential termination between OUT+ and OUT- | | 100 | | Ω |
| ΔR_{OTSE} | Mis-Match in Output Termination Resistors | Mis-match in output terminations at OUT+ and OUT- | | | 5 | % |
| V_{OCM} | Output Common Mode Voltage | | | 2.7 | | V |
| POWER DISSIPATION | | | | | | |
| P_D | Power Dissipation | $V_{DD} = 3.3V @ 25^\circ C$ All outputs terminated by $100\Omega \pm 1\%$. $DEL_{[1:0]}=0$, $DES_{[1:0]}=0$ Running PRBS 2 ⁷ -1 pattern at 4.25 Gbps | | 0.45 | | W |
| AC CHARACTERISTICS | | | | | | |
| t_R | Differential Low to High Transition Time | Measured with a clock-like pattern at 4.25 Gbps, between 20% and 80% of the differential output voltage. De-emphasis disabled. | | 85 | | ps |
| t_F | Differential High to Low Transition Time | Transition time is measured with fixture as shown in <i>Figure 5</i> , adjusted to reflect the transition time at the output pins. | | 85 | | ps |
| t_{PLH} | Differential Low to High Propagation Delay | Measured at 50% differential voltage from input to output. | | | 1 | ns |
| t_{PHL} | Differential High to Low Propagation Delay | | | | 1 | ns |
| t_{SKP} | Pulse Skew | $ t_{PHL} - t_{PLH} $ | | | 20 | ps |
| t_{SKO} | Output Skew (Note 7) | Difference in propagation delay among data paths in the same device. | | | 100 | ps |
| t_{SKPP} | Part-to-Part Skew | Difference in propagation delay between the same output from devices operating under identical condition. | | | 100 | ps |
| t_{SM} | Mux Switch Time | Measured from V_{IH} or V_{IL} of the mux-control or loopback control to 50% of the valid differential output. | | 1.8 | 6 | ns |
| RJ | Device Random Jitter (Note 5) | See <i>Figure 5</i> for test circuit. Alternating-1-0 pattern. EQ and de-emphasis disabled. At 0.25 Gbps At 1.25 Gbps At 4.25 Gbps | | | 2 2 2 | psrms psrms psrms |
| DJ | Device Deterministic Jitter (Note 6) | See <i>Figure 5</i> for test circuit. EQ and de-emphasis disabled Between 0.25 and 2.5 Gbps with PRBS7 pattern for DS25MB100 @ -40°C to 85°C | | | 35 | pspp |
| DR | Maximum Data Rate (Note 9) | Tested with alternating-1-0 pattern | 0.25 | | 4.25 | Gbps |

Note 1: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters measured at $V_{CC} = 3.3V$, $T_A = 25^\circ C$, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

Note 3: IN+ and IN- are generic names refer to one of the many pairs of complimentary inputs of the DS42MB100. OUT+ and OUT- are generic names refer to one of the many pairs of the complimentary outputs of the DS42MB100. Differential input voltage V_{ID} is defined as $|IN+ - IN-|$. Differential output voltage V_{OD} is defined as $|OUT+ - OUT-|$.

Note 4: K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000}

K28.5 pattern is a 20-bit repeating pattern of +K28.5 and -K28.5 code groups {110000 0101 001111 1010}

Note 5: Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation $\sqrt{(RJ_{OUT}^2 - RJ_{IN}^2)}$, where RJ_{OUT} is the total random jitter measured at the output of the device in psrms, RJ_{IN} is the random jitter of the pattern generator driving the device.

Note 6: Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation $(DJ_{OUT} - DJ_{IN})$, where DJ_{OUT} is the total peak-to-peak deterministic jitter measured at the output of the device in pspp, DJ_{IN} is the peak-to-peak deterministic jitter of the pattern generator driving the device.

Note 7: t_{SKO} is the magnitude difference in the propagation delays among data paths between switch A and switch B of the same port and similar data paths between port 0 and port 1. An example is the output skew among data paths from SIA_0± to LO_0±, SIB_0± to LO_0±, SIA_1± to LO_1± and SIB_1± to LO_1±. Another example is the output skew among data paths from LI_0± to SOA_0±, LI_0± to SOB_0±, LI_1± to SOA_1± and LI_1± to SOB_1±. t_{SKO} also refers to the delay skew of the loopback paths of the same port and between similar data paths between port 0 and port 1. An example is the output skew among data paths SIA_0± to SOA_0±, SIB_0± to SOB_0±, SIA_1± to SOA_1± and SIB_1± to SOB_1±.

Note 8: Thermal resistances are based on having 16 thermal relief vias on the DAP pad under the 0 airflow condition.

Note 9: This parameter is guaranteed by design and/or characterization. It is not tested in production.

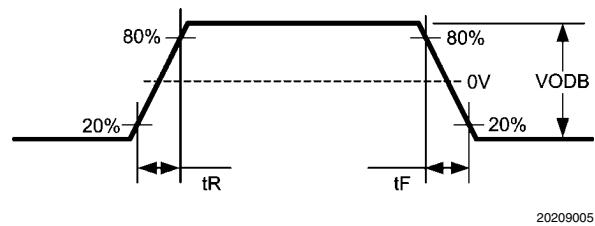
Note 10: ESD tests conform to the following standards:

Human Body Model applicable standard: MIL-STD-883, Method 3015.7

Machine Model applicable standard: JESD22-A115-A (ESD MM standard of JEDEC)

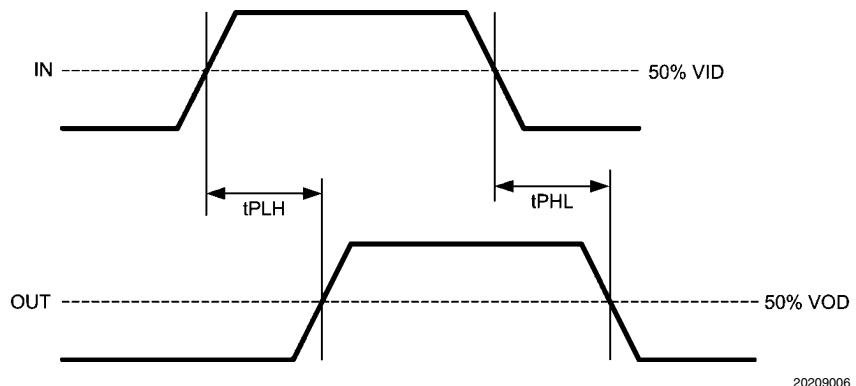
Field-induced Charge Device Model: Applicable standard JESD22-C101-C (ESD FICDM standard of JEDEC)

Timing Diagrams



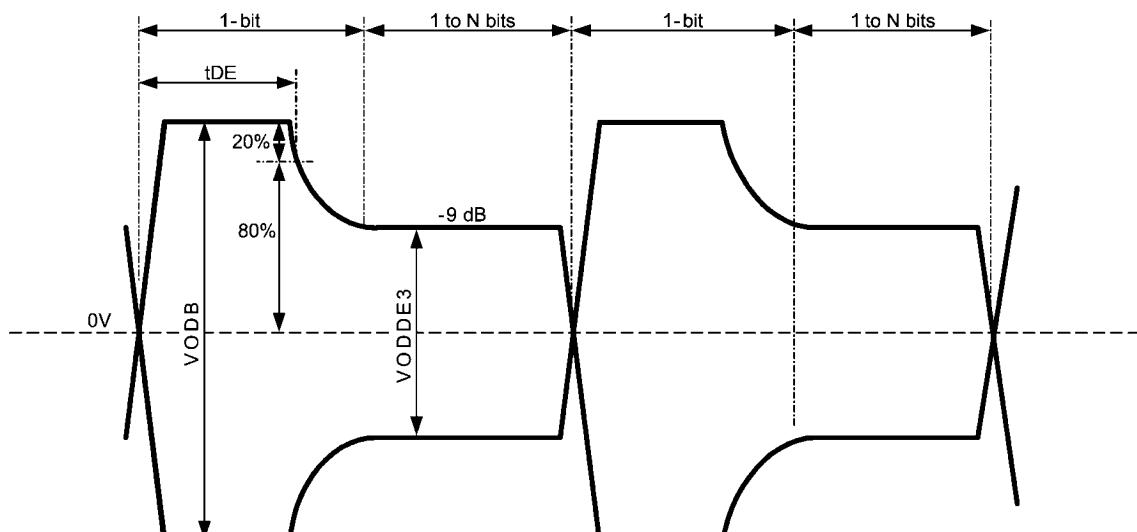
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FIGURE 2. Driver Output Transition Time



20209006

FIGURE 3. Propagation Delay From Input To Output



20209007

FIGURE 4. Test Condition For Output De-Emphasis Duration

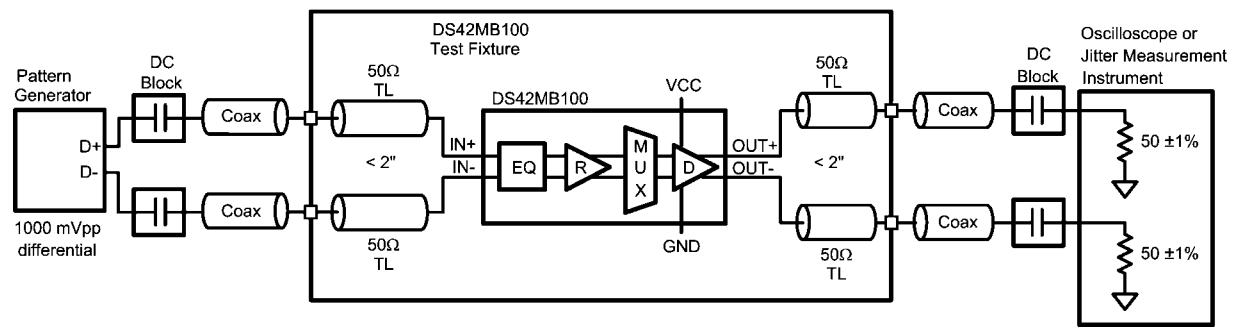
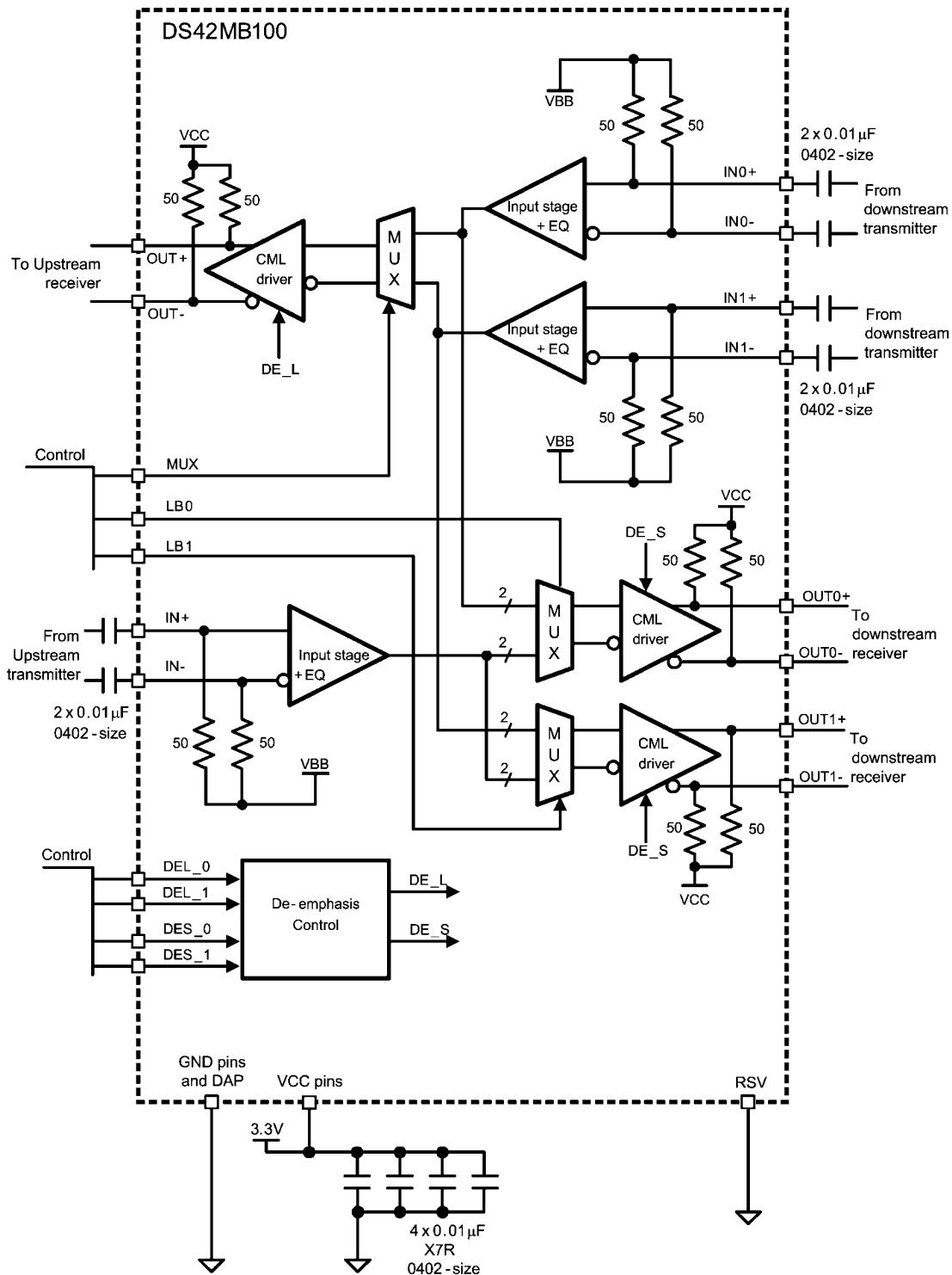


FIGURE 5. AC Test Circuit

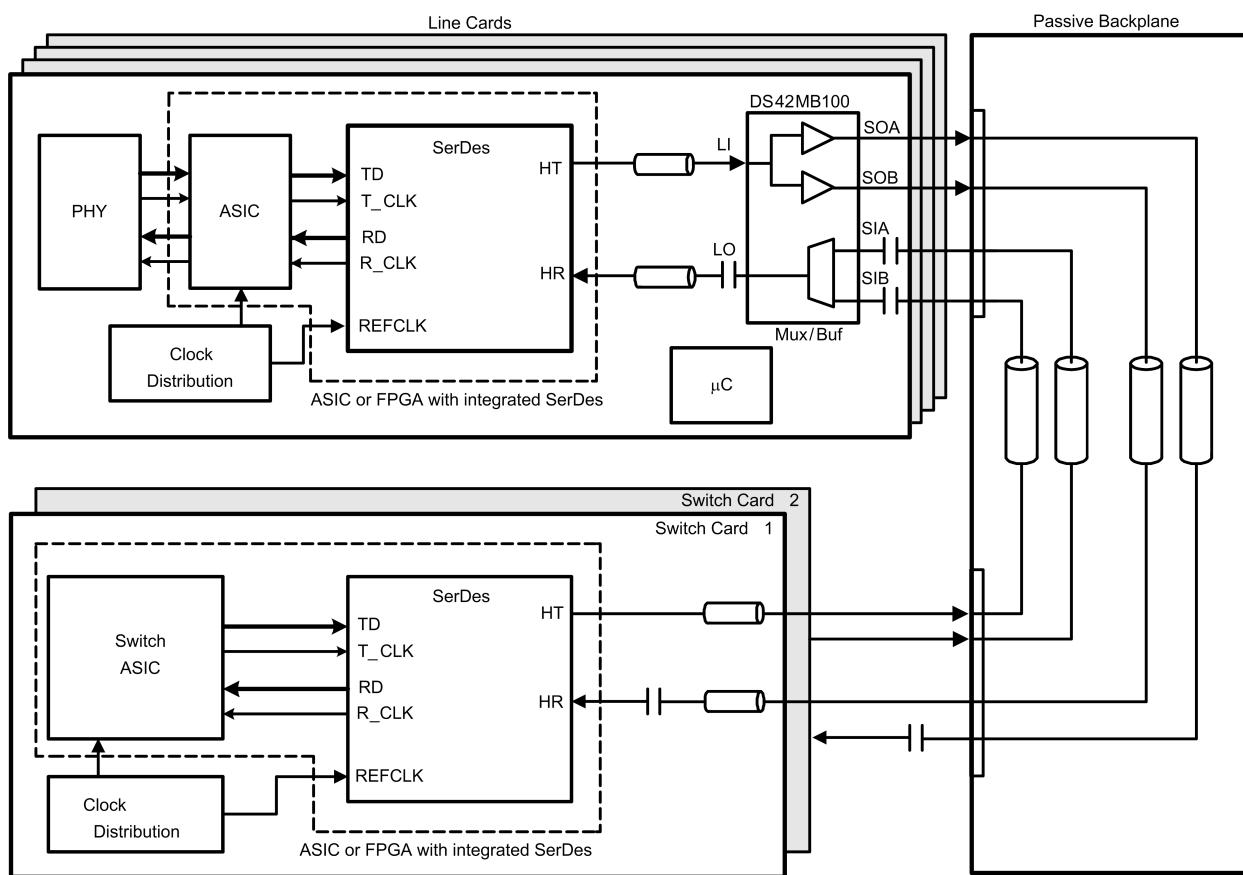
20209008

Application Information



20209009

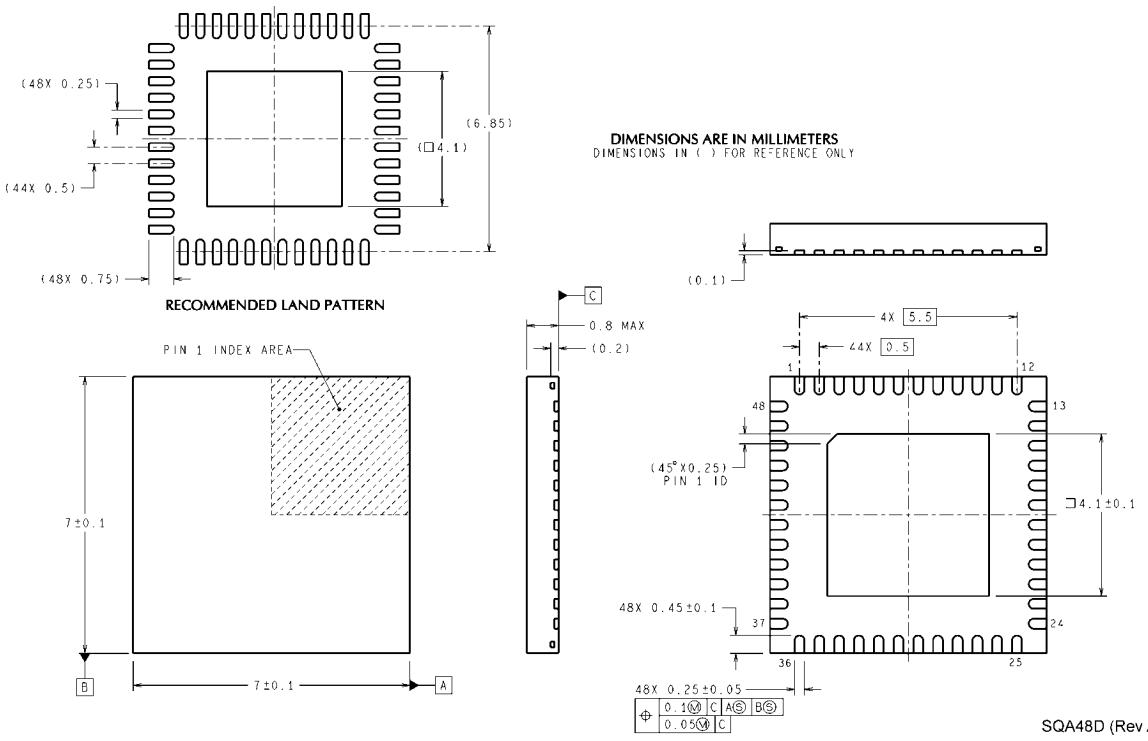
FIGURE 6. Application Diagram



20209010

FIGURE 7. Chassis Based Network Switch System With Redundancy

Physical Dimensions

 inches (millimeters) unless otherwise noted

LLP-36 Package
Order Number DS42MB100TSQ
NS Package Number SQA36A

SQA48D (Rev A)

Notes

DS42MB100

Notes

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