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DALLAS SEMICONDUCTOR MAXIM

# DS75LV
## Digital Thermometer and Thermostat

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## DESCRIPTION

This low-voltage (1.7V to 3.7V) digital thermometer and thermostat provides 9-, 10-, 11-, or 12-bit digital temperature readings over a -55°C to +125°C range with ±2°C accuracy over a -25°C to +100°C range. At power-up, the DS75LV defaults to 9-bit resolution for software compatibility with the LM75. Communication with the DS75LV is achieved through a simple 2-wire serial interface. Three address pins allow up to eight DS75LV devices to operate on the same 2-wire bus, which greatly simplifies distributed temperature-sensing applications.

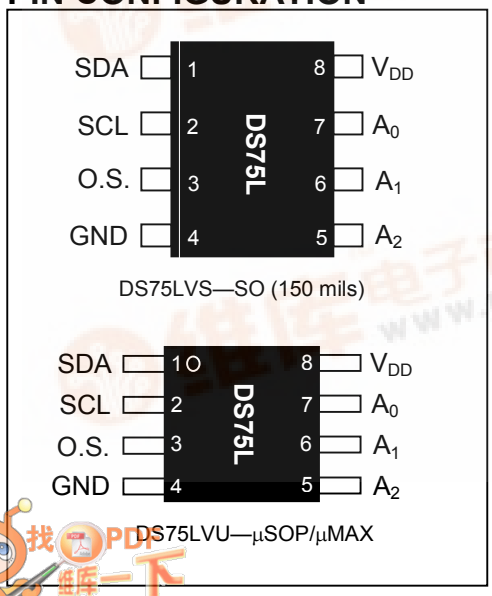
The DS75LV thermostat has a dedicated open-drain output (O.S.) and programmable fault tolerance, which allows the user to define the number of consecutive error conditions that must occur before O.S is activated. There are two thermostatic operating modes that control thermostat operation based on user-defined trip-points ($T_{OS}$ and $T_{HYST}$).

A block diagram of the DS75LV is shown in Figure 1 and detailed pin descriptions are given in Table 2.

## APPLICATIONS

Personal Computers
Cellular Base Stations
Office Equipment
Any Thermally Sensitive System

## PIN CONFIGURATION




## FEATURES

- **Operating Range from 1.7V to 3.7V**
- **Temperature Measurements Require No External Components**
- **Measures Temperatures from -55°C to +125°C (-67°F to +257°F)**
- **±2°C Accuracy Over a -25°C to +100°C Range**
- **Thermometer Resolution is User-Configurable from 9 (Default) to 12 Bits (0.5°C to 0.0625°C Resolution)**
- **9-Bit Conversion Time is 25ms (Max)**
- **Thermostatic Settings are User-Definable**
- **Data Read/Write Occurs Through a 2-Wire Serial Interface (SDA and SCL Pins)**
- **Data Lines Filtered Internally for Noise Immunity (50ns Deglitch)**
- **Bus Timeout Feature Prevents Lockup Problems on 2-Wire Interface**
- **Multidrop Capability Simplifies Distributed Temperature-Sensing Applications**
- **Pin/Software Compatible with the LM75**
- **Available in 8-Pin µSOP (µMAX) and SO Packages**

## ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| DS75LVS+ | -55°C to +125°C | DS75LV (150-mil) 8-SO |
| DS75LVS+T&R | -55°C to +125°C | DS75LV (150-mil) 8-SO, 2500 Piece Tape-and-Reel |
| DS75LVU+ | -55°C to +125°C | DS75LV 8-µSOP (µMAX) |
| DS75LVU+T&R | -55°C to +125°C | DS75LV 8-µSOP (µMAX), 3000 Piece Tape-and-Reel |

*Ordering Information continued at the end of the data sheet.*

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## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on $V_{DD}$, Relative to Ground | -0.3V to +4.0V |
| Voltage on Any Other Pin, Relative to Ground | -0.3V to +6.0V |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -55°C to +125°C |
| Soldering Temperature | 260°C for 10 seconds |

*These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

The Dallas Semiconductor DS75LV is built to the highest quality standards and manufactured for long-term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, the DS75LV is not exposed to environmental stresses, such as burn-in, that some industrial applications require. For specific reliability information on this product, please contact the factory in Dallas at (972) 371-4448.

## DC ELECTRICAL CHARACTERISTICS

(-55°C to +125°C; 1.7V ≤ $V_{DD}$ ≤ 3.7V.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | (Note 10) | 1.7 | 3.7 | V |
| Thermometer Error (Note 2) | $T_{ERR}$ | -25 to +100 | | ± 2.0 | °C |
| | | -55 to +125 | | ± 3.0 | |
| Input Logic High | $V_{IH}$ | (Note 1) | 0.7 × $V_{DD}$ | 5.5 | V |
| Input Logic Low | $V_{IL}$ | (Note 1) | -0.5 | 0.3 × $V_{DD}$ | V |
| SDA Output Logic Low Voltage (Note 1) | $V_{OL1}$ | 3mA sink current | 0 | 0.4 | V |
| | $V_{OL2}$ | 6mA sink current | 0 | 0.6 | |
| O.S. Saturation Voltage | $V_{OL}$ | 4mA sink current (Notes 1, 2) | | 0.8 | V |
| Input current each I/O pin | | 0.4 < $V_{I/O}$< 0.9 $V_{DD}$ | -10 | +10 | µA |
| I/O Capacitance | $C_{I/O}$ | | | 10 | pF |
| Standby Current | $I_{DD1}$ | (Notes 3, 4) | | 2 | µA |
| Active Current (Notes 3, 4) | $I_{DD}$ | Active Temp Conversions | | 1000 | µA |
| | | Communication only | | 100 | |

## AC ELECTRICAL CHARACTERISTICS

(-55°C to +125°C; 1.7V ≤ $V_{DD}$ ≤ 3.7V.)

| PARAMETER | SYMBOL | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution | | | 9 | | 12 | bits |
| Temperature Conversion Time | $t_{CONVT}$ | 9-bit conversions | | | 25 | ms |
| | | 10-bit conversions | | | 50 | |
| | | 11-bit conversions | | | 100 | |
| | | 12-bit conversions | | | 200 | |
| SCL Frequency | $f_{SCL}$ | | | | 400 | KHz |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$ | (Note 5) | 1.3 | | | µs |
| START and Repeated START Hold Time from | $t_{HD:STA}$ | (Notes 5, 6) | 600 | | | ns |

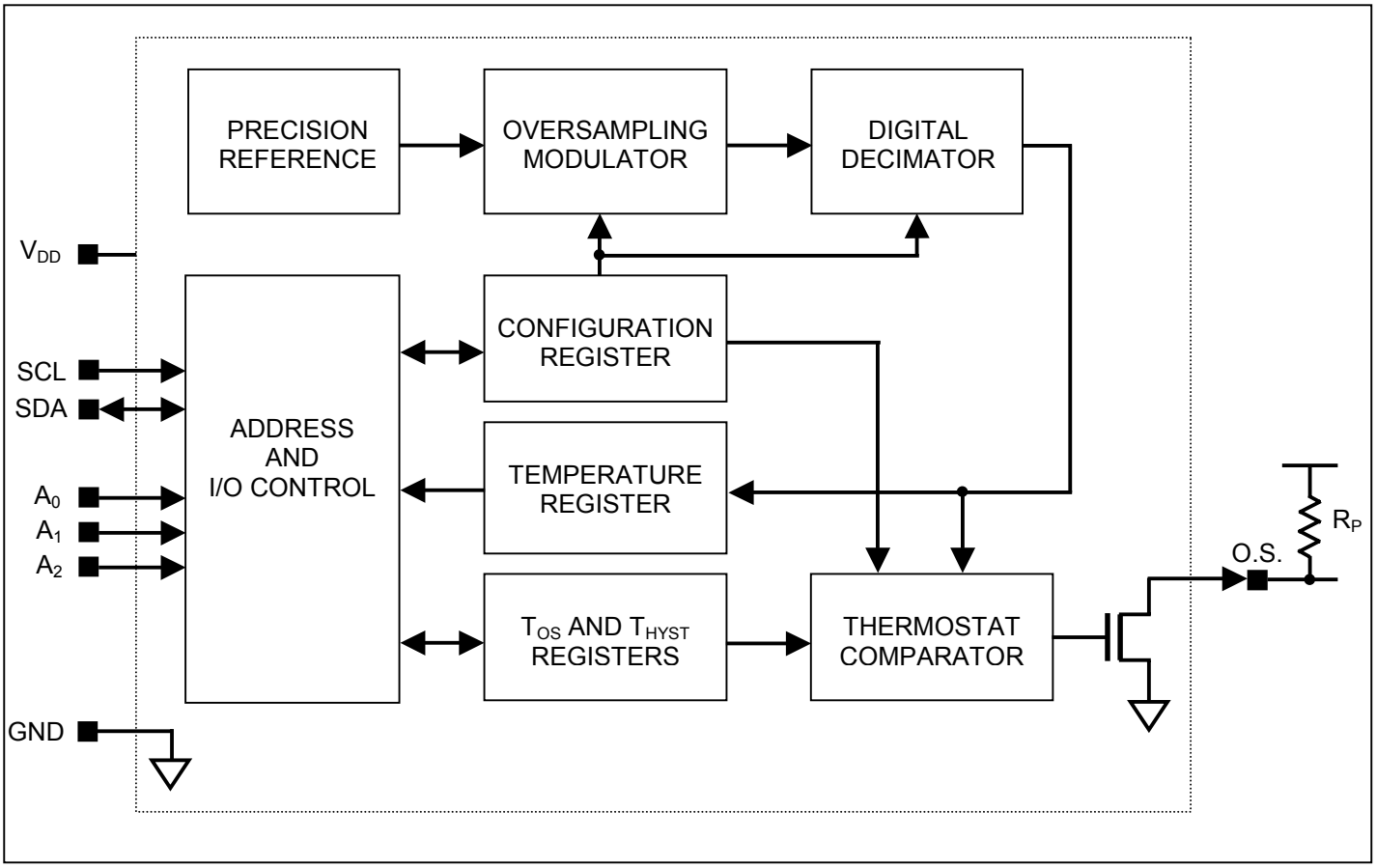
| | | | | | |
|---|---|---|---|---|---|
| Falling SCL | | | | | |
| Low Period of SCL | $t_{LOW}$ | (Note 5) | 1.3 | | µs |
| High Period of SCL | $t_{HIGH}$ | (Note 5) | 0.6 | | µs |
| Repeated START Condition Setup Time to Rising SCL | $t_{SU:STA}$ | (Note 5) | 600 | | ns |
| Data-Out Hold Time from Falling SCL | $t_{HD:DAT}$ | (Notes 5, 8) | 0 | 0.9 | µs |
| Data-In Setup Time to Rising SCL | $t_{SU:DAT}$ | (Note 5) | 100 | | ns |
| Rise Time of SDA and SCL (Receive) | $t_R$ | (Notes 5, 7) | $20 + 0.1C_B$ | 300 | ns |
| Fall Time of SDA and SCL (Receive) | $t_F$ | (Notes 5, 7) | $20 + 0.1C_B$ | 300 | ns |
| Spike Suppression Filter Time (Deglitch Filter) | $t_{SS}$ | | 0 | 50 | ns |
| STOP Setup Time to Rising SCL | $t_{SU:STO}$ | (Note 5) | 600 | | ns |
| Capacitive Load for Each Bus Line | $C_B$ | | | 400 | pF |
| Input Capacitance | $C_I$ | | 5 | | pF |
| Serial Interface Reset Time | $t_{TIMEOUT}$ | SDA time low (Note 9) | 75 | 325 | ms |

**Note 1:** All voltages are referenced to ground.
**Note 2:** Internal heating caused by O.S. loading will cause the DS75LV to read approximately 0.5°C higher if O.S. is sinking the max rated current.
**Note 3:** $I_{DD}$ specified with O.S. pin open.
**Note 4:** $I_{DD}$ specified with $V_{DD}$ at 3.0V and SDA, SCL = 3.0V, 0°C to 70°C.
**Note 5:** See Timing Diagram in Figure 2. All timing is referenced to 0.9 x $V_{DD}$ and 0.1 x $V_{DD}$.
**Note 6:** After this period, the first clock pulse is generated.
**Note 7:** For example, if $C_B$ = 300pF, then $t_R$[min] = $t_F$[min] = 50ns.
**Note 8:** The DS75LV provides an internal hold time of at least 75ns on the SDA signal to bridge the undefined region of SCL's falling edge.
**Note 9:** This time-out applies only when the DS75LV is holding SDA low. Other devices can hold SDA low indefinitely and the DS75LV will not reset.
**Note 10:** The DS75LV has a maximum operating voltage of 3.7V. Contact Dallas Semiconductor for information on the availability of a 3.7V to 5.5V version of the DS75LV.

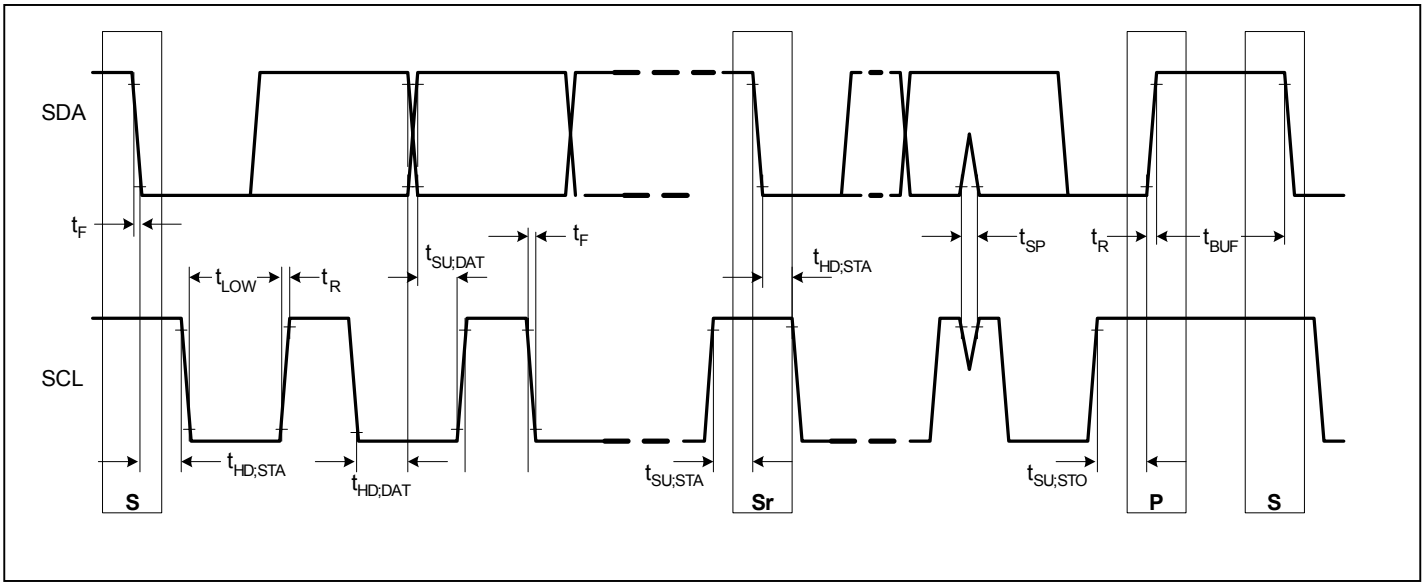
## Table 1. Detailed Pin Description

| PIN | SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1 | SDA | **Data Input/Output**. For 2-wire serial communication port. Open-drain. |
| 2 | SCL | **Clock Input**. 2-wire serial communication port. |
| 3 | O.S. | **Thermostat Output**. Open-drain. |
| 4 | GND | **Ground** |
| 5 | $A_2$ | **Address Input** |
| 6 | $A_1$ | **Address Input** |
| 7 | $A_0$ | **Address Input** |
| 8 | $V_{DD}$ | **Supply Voltage.** +1.7V to +3.7V supply pin. |

## Figure 1. DS75LV Functional Block Diagram




## Figure 2. Timing Diagram



## OPERATION—MEASURING TEMPERATURE

The DS75LV measures temperature using a bandgap temperature sensing architecture. An on-board delta-sigma analog-to-digital converter (ADC) converts the measured temperature to a digital value that is calibrated in degrees centigrade; for Fahrenheit applications a lookup table or conversion routine must be used. The DS75LV is factory-calibrated and requires no external components to measure temperature.

At power-up the DS75LV immediately begins converting temperature to a digital value. The resolution of the digital output data is user-configurable to 9, 10, 11, or 12 bits, corresponding to temperature increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively, with 9-bit default resolution at power-up. The resolution is controlled via the R0 and R1 bits in the configuration register as explained in the *CONFIGURATION REGISTER* section of this data sheet. Note that the conversion time doubles for each additional bit of resolution.

After each temperature measurement and analog-to-digital conversion, the DS75LV stores the temperature as a 16-bit two's complement number in the 2-byte temperature register (see Figure 3). The sign bit (S) indicates if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The most recently converted digital measurement can be read from the temperature register at any time. Since temperature conversions are performed in the background, reading the temperature register does not affect the operation in progress.

Bits 3 through 0 of the temperature register are hardwired to 0. When the DS75LV is configured for 12-bit resolution, the 12 MSbs (bits 15 through 4) of the temperature register will contain temperature data. For 11-bit resolution, the 11 MSbs (bits 15 through 5) of the temperature register will contain data, and bit 4 will read out as 0. Likewise, for 10-bit resolution, the 10 MSbs (bits 15 through 6) will contain data, and for 9-bit the 9 MSbs (bits 15 through 7) will contain data, and all unused LSbs will contain 0s. Table 3 gives examples of 12-bit resolution digital output data and the corresponding temperatures.

### Figure 3. Temperature, $T_{OS}$, and $T_{HYST}$ Register Format

| | bit 15 | bit 14 | bit 13 | bit 12 | bit 11 | bit 10 | bit 9 | bit 8 |
|---|---|---|---|---|---|---|---|---|
| **MS Byte** | S | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
| **LS Byte** | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | 0 | 0 | 0 | 0 |

### Table 2. 12-Bit Resolution Temperature/Data Relationship

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | DIGITAL OUTPUT (HEX) |
|---|---|---|
| +125 | 0111 1101 0000 0000 | 7D00h |
| +25.0625 | 0001 1001 0001 0000 | 1910h |
| +10.125 | 0000 1010 0010 0000 | 0A20h |
| +0.5 | 0000 0000 1000 0000 | 0080h |
| 0 | 0000 0000 0000 0000 | 0000h |
| -0.5 | 1111 1111 1000 0000 | FF80h |
| -10.125 | 1111 0101 1110 0000 | F5E0h |
| -25.0625 | 1110 0110 1111 0000 | E6F0h |
| -55 | 1100 1001 0000 0000 | C900h |

## SHUTDOWN MODE

For power-sensitive applications, the DS75LV offers a low-power shutdown mode. The SD bit in the configuration register controls shutdown mode. When SD is changed to 1, the conversion in progress will be completed and the result stored in the temperature register after which the DS75LV will go into a low-power standby state. The O.S. output will be cleared if the thermostat is operating in interrupt mode and O.S will remain unchanged in comparator mode. The 2-wire interface remains operational in shutdown mode, and writing a 0 to the SD bit returns the DS75LV to normal operation.

## OPERATION—THERMOSTAT

The DS75LV thermostat has two operating modes, comparator mode and interrupt mode, which activate and deactivate the open-drain thermostat output (O.S.) based on user-programmable trip-points ($T_{OS}$ and $T_{HYST}$). The DS75LV powers up with the thermostat in comparator mode, active-low O.S. polarity, over-temperature trip-point ($T_{OS}$) register set to 80□C, and the hystoresis trip-point ($T_{HYST}$) register set to 75□C. If these power-up settings are compatible with the application, the DS75LV can be used as a standalone thermostat (i.e., no 2–wire communication required). If interrupt mode operation, active-high O.S. polarity or different $T_{OS}$ and $T_{HYST}$ values are desired, they must be programmed after power-up, so standalone operation is not possible.

In both operating modes, the user can program the thermostat fault tolerance, which sets how many consecutive temperature readings (1, 2, 4, or 6) must fall outside of the thermostat limits before the thermostat output is triggered. The fault tolerance is set by the F1 and F0 bits in the configuration register. At power-up the fault tolerance is set to 1.

The data format of the $T_{OS}$ and $T_{HYST}$ registers is identical to that of the temperature register (see Figure 3), i.e., a two-byte two's complement representation of the trip-point temperature in degrees centigrade with bits 3 through 0 hardwired to 0. After every temperature conversion, the measurement is compared to the values stored in the $T_{OS}$ and $T_{HYST}$ registers. The O.S. output is updated based on the result of the comparison and the operating mode of the IC. The number of $T_{OS}$ and $T_{HYST}$ bits used during the thermostat comparison is equal to the conversion resolution set by the R1 and R0 bits in the configuration register. For example, if the resolution is 9 bits, only the 9 MSbs of $T_{OS}$ and $T_{HYST}$ will be used by the thermostat comparator.

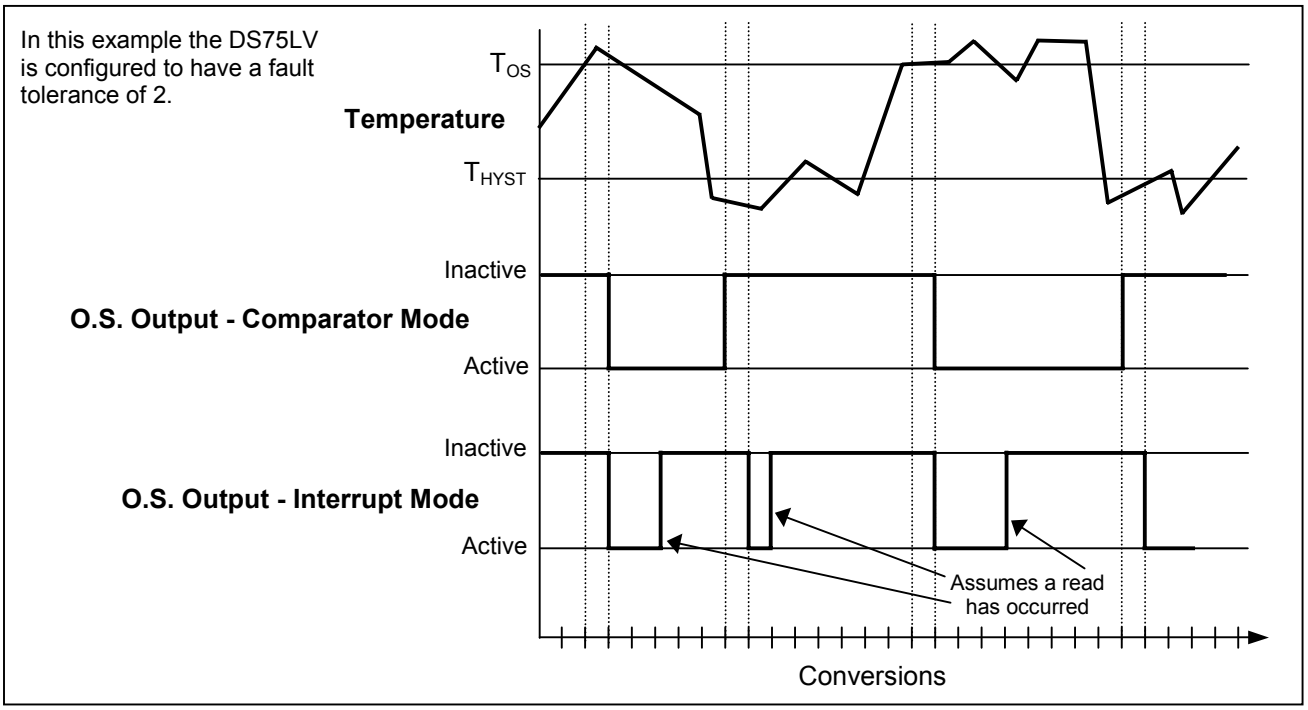
The active state of the O.S. output can be changed via the POL bit in the configuration register. The power-up default is active low.

If the user does not wish to use the thermostat capabilities of the DS75LV, the O.S. output should be left floating. Note that if the thermostat is not used, the $T_{OS}$ and $T_{HYST}$ registers can be used for general storage of system data.

**Comparator Mode:** When the thermostat is in comparator mode, O.S. can be programmed to operate with any amount of hystoresis. The O.S. output becomes active when the measured temperature exceeds the $T_{OS}$ value a consecutive number of times as defined by the F1 and F0 fault tolerance (FT) bits in the configuration register. O.S. then stays active until the first time the temperature falls below the value stored in $T_{HYST}$. Putting the device into shutdown mode does not clear O.S. in comparator mode. Thermostat comparator mode operation with FT = 2 is illustrated in Figure 4.

**Interrupt Mode:** In interrupt mode, the O.S. output first becomes active when the measured temperature exceeds the $T_{OS}$ value a consecutive number of times equal to the FT value in the configuration register. Once activated, O.S. can only be cleared by either putting the DS75LV into shutdown mode or by reading from any register (temperature, configuration, $T_{OS}$, or $T_{HYST}$ ) on the device. Once O.S. has been deactivated, it will only be reactivated when the measured temperature falls below the $T_{HYST}$ value a consecutive number of times equal to the FT value. Again, O.S can only be cleared by putting the device into shutdown mode or reading any register. Thus, this interrupt/clear process is cyclical between $T_{OS}$ and $T_{HYST}$ events (i.e, $T_{OS}$, clear, $T_{HYST}$, clear, $T_{OS}$, clear, $T_{HYST}$, clear, etc.). Thermostat interrupt mode operation with FT = 2 is illustrated in Figure 4.

## Figure 4. O.S. OUTPUT Operation Example




## CONFIGURATION REGISTER

The configuration register allows the user to program various DS75LV options such as conversion resolution, thermostat fault tolerance, thermostat polarity, thermostat operating mode, and shutdown mode. The configuration register is arranged as shown in Figure 5 and detailed descriptions of each bit are provided in Table 4. The user has read/write access to all bits in the configuration register except the MSb, which is a reserved read-only bit. The entire register is volatile, and thus powers–up in its default state.

## Figure 5. Configuration Register

| MSb | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | LSb |
|---|---|---|---|---|---|---|---|
| 0 | R1 | R0 | F1 | F0 | POL | TM | SD |

## Table 3. Configuration Register Bit Descriptions

| BIT NAME | FUNCTIONAL DESCRIPTION |
|---|---|
| **0**<br>Reserved | Power-up state = 0<br>The master can write to this bit, but it will always read out as a 0. |
| **R1**<br>Conversion Resolution Bit 1 | Power-up state = 0<br>Sets conversion resolution (see Table 5) |
| **R0**<br>Conversion Resolution Bit 0 | Power-up state = 0<br>Sets conversion resolution (see Table 5) |
| **F1**<br>Thermostat Fault Tolerance Bit 1 | Power-up state = 0<br>Sets the thermostat fault tolerance (see Table 6). |
| **F0**<br>Thermostat Fault Tolerance Bit 0 | Power-up state = 0<br>Sets the thermostat fault tolerance (see Table 6). |
| **POL**<br>Thermostat Output (O.S.) Polarity | Power-up state = 0<br>POL = 0 — O.S. is active low.<br>POL = 1 — O.S. is active high. |
| **TM**<br>Thermostat Operating Mode | Power-up state = 0<br>TM = 0 — Comparator mode.<br>TM = 1 — Interrupt mode.<br>See the *OPERATION–Thermostat* section for a detailed description of these modes. |
| **SD**<br>Shutdown | Power-up state = 0<br>SD = 0 — Active conversion and thermostat operation.<br>SD = 1 — Shutdown mode.<br>See the *SHUTDOWN MODE* section for a detailed description of this mode. |

## Table 4. Resolution Configuration

| R1 | R0 | THERMOMETER RESOLUTION | MAX CONVERSION TIME |
|---|---|---|---|
| 0 | 0 | 9-bit | 150ms |
| 0 | 1 | 10-bit | 300ms |
| 1 | 0 | 11-bit | 600ms |
| 1 | 1 | 12-bit | 1200ms |

## Table 5. Fault Tolerance Configuration

| F1 | F0 | CONSECUTIVE OUT-OF-LIMITS CONVERSIONS TO TRIGGER O.S. |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

## REGISTER POINTER

The four DS75LV registers each have a unique two-bit pointer designation, which is defined in Table 7. When reading from or writing to the DS75LV, the user must "point" the DS75LV to the register that is to be accessed. When reading from the DS75LV, once the pointer is set, it will remain pointed at the same register until it is changed. For example, if the user desires to perform consecutive reads from the temperature register, then the pointer only has to be set to the temperature register one time, after which all reads will automatically be from the temperature register until the pointer value is changed. When writing to the DS75LV, the pointer value must be refreshed each time a write is performed, even if the same register is being written to twice in a row.

At power-up, the pointer defaults to the temperature register location. The temperature register can be read immediately without resetting the pointer.

Changes to the pointer setting are accomplished as described in the *2-WIRE SERIAL DATA BUS* section of this data sheet.

### Table 6. Pointer Definition

| REGISTER | P1 | P0 |
|---|---|---|
| Temperature | 0 | 0 |
| Configuration | 0 | 1 |
| $T_{HYST}$ | 1 | 0 |
| $T_{OS}$ | 1 | 1 |

## 2-WIRE SERIAL DATA BUS

The DS75LV communicates over a standard bi-directional 2-wire serial data bus that consists of a serial clock (SCL) signal and serial data (SDA) signal. The DS75LV interfaces to the bus via the SCL input pin and open-drain SDA I/O pin. All communication is MSb first.

The following terminology is used to describe 2-wire communication:

**Master Device:** Microprocessor/microcontroller that controls the slave devices on the bus. The master device generates the SCL signal and START and STOP conditions.

**Slave:** All devices on the bus other than the master. The DS75LV always functions as a slave.

**Bus Idle or Not Busy:** Both SDA and SCL remain high. SDA is held high by a pullup resistor when the bus is idle, and SCL must either be forced high by the master (if the SCL output is push-pull) or pulled high by a pullup resistor (if the SCL output is open-drain).

**Transmitter:** A device (master or slave) that is sending data on the bus.

**Receiver:** A device (master or slave) that is receiving data from the bus.

**START Condition:** Signal generated by the master to indicate the beginning of a data transfer on the bus. The master generates a START condition by pulling SDA from high to low while SCL is high (see Figure 6). A "repeated" START is sometimes used at the end of a data transfer (instead of a STOP) to indicate that the master will perform another operation.

**STOP Condition:** Signal generated by the master to indicate the end of a data transfer on the bus. The master generates a STOP condition by transitioning SDA from low to high while SCL is high (see Figure 6). After the STOP is issued, the master releases the bus to its idle state.

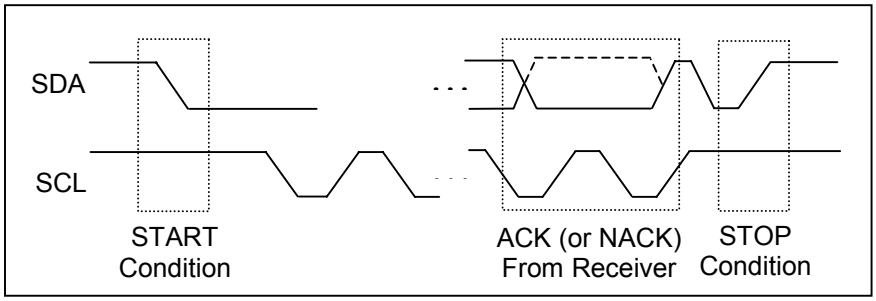
**Acknowledge (ACK):** When a device (either master or slave) is acting as a receiver, it must generate an acknowledge (ACK) on the SDA line after receiving every byte of data. The receiving device performs an ACK by pulling the SDA line low for an entire SCL period (see Figure 6). During the ACK clock cycle, the transmitting device must release SDA. A variation on the ACK signal is the "not acknowledge" (NACK). When the master device is acting as a receiver, it uses a NACK instead of an ACK after the last data byte to indicate that it is finished receiving data. The master indicates a NACK by leaving the SDA line high during the ACK clock cycle.

**Slave Address:** Every slave device on the bus has a unique 7-bit address that allows the master to access that device. The DS75LV's 7-bit bus address is 1 0 0 1 $A_2$ $A_1$ $A_0$, where $A_2$, $A_1$ and $A_0$ are user-selectable via the corresponding input pins. The three address pins allow up to eight DS75LVs to be multi-dropped on the same bus.

**Address Byte:** The control byte is transmitted by the master and consists of the 7-bit slave address plus a read/write (R/$\overline{W}$) bit (see Figure 7). If the master is going to read data from the slave device then R/$\overline{W}$ = 1, and if the master is going to write data to the slave device then R/$\overline{W}$ = 0.

**Pointer Byte:** The pointer byte is used by the master to tell the DS75LV which register is going to be accessed during communication. The six MSbs of the pointer byte (see Figure 8) are always 0 and the two LSbs correspond to the desired register as shown in Table 7.

## Figure 6. Start, Stop, and ACK Signals




## Figure 7. Address Byte

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | $A_2$ | $A_1$ | $A_0$ | R/$\overline{W}$ |

## Figure 8. Pointer Byte

| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | P1 | P0 |

## GENERAL 2-WIRE INFORMATION

- All data is transmitted MSb first over the 2-wire bus.
- One bit of data is transmitted on the 2-wire bus each SCL period.
- A pullup resistor is required on the SDA line and, when the bus is idle, both SDA and SCL must remain in a logic-high state.
- All bus communication must be initiated with a START condition and terminated with a STOP condition. During a START or STOP is the only time SDA is allowed to change states while SCL is high. At all other times, changes on the SDA line can only occur when SCL is low: SDA must remain stable when SCL is high.
- After every 8-bit (1-byte) transfer, the receiving device must answer with an ACK (or NACK), which takes one SCL period. Therefore, nine clocks are required for every one-byte data transfer.

**Writing to the DS75LV**— To write to the DS75LV, the master must generate a START followed by an address byte containing the DS75LV bus address. The value of the R/W bit must be a 0, which indicates that a write is about to take place. The DS75LV will respond with an ACK after receiving the address byte. The master then sends a pointer byte which tells the DS75LV which register is being written to. The DS75LV will again respond with an ACK after receiving the pointer byte. Following this ACK the master device must immediately begin transmitting data to the DS75LV. When writing to the configuration register, the master must send one byte of data (see Figure 9b), and when writing to the $T_{OS}$ or $T_{HYST}$ registers the master must send two bytes of data (see Figure 9c). After receiving each data byte, the DS75LV will respond with an ACK, and the transaction is finished with a STOP from the master.

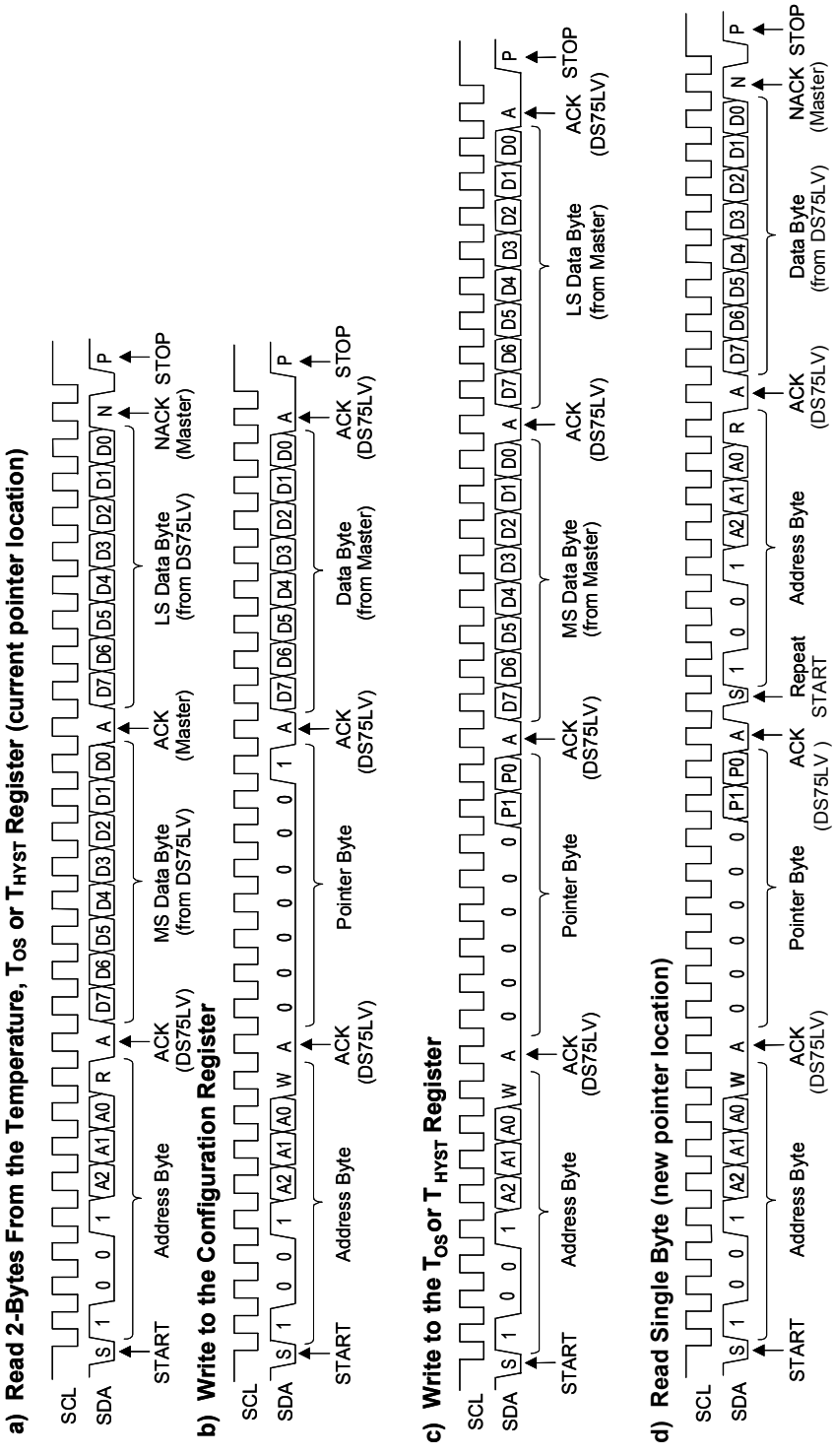
**Software POR**—The soft power on reset (POR) command is 54h. The master sends a START followed by an address byte containing the DS75LV bus address. The R/W bit must be a 0. The DS75LV will respond with an ACK. If the next byte is a 0x54, the DS75LV will reset as if power had been cycled. No ACK will be send by the IC after the POR command is received.

**Reading from the DS75LV**—When reading from the DS75LV, if the pointer was already pointed to the desired register during a previous transaction, the read can be performed immediately without changing the pointer setting. In this case the master sends a START followed by an address byte containing the DS75LV bus address. The R/W bit must be a 1, which tells the DS75LV that a read is being performed. After the DS75LV sends an ACK in response to the address byte, the DS75LV will begin transmitting the requested data on the next clock cycle. When reading from the configuration register, the DS75LV will transmit one byte of data, after which the master must respond with a NACK followed by a STOP (see Figure 9e). For two-byte reads (i.e., from the Temperature, $T_{OS}$ or $T_{HYST}$ register), the DS75LV will transmit two bytes of data, and the master must respond to the first data byte with an ACK and to the second byte with a NACK followed by a STOP (see Figure 9a). If only the most significant byte of data is needed, the master can issue a NACK followed by a STOP after reading the first data byte in which case the transaction will be the same as for a read from the configuration register.

If the pointer is not already pointing to the desired register, the pointer must first be updated as shown in Figure 9d, which shows a pointer update followed by a single-byte read. The value of the R/W bit in the initial address byte is a 0 (“write”) since the master is going to write a pointer byte to the DS75LV. After the DS75LV responds to the address byte with an ACK, the master sends a pointer byte that corresponds to the desired register. The master must then perform a repeated start followed by a standard one or two byte read sequence (with R/W =1) as described in the previous paragraph.

**Bus Timeout**—The DS75LV has a bus timeout feature that prevents communication errors from leaving the IC in a state where SDA is held low disrupting other devices on the bus. If the DS75LV holds the SDA line low for a period of $t_{TIMEOUT}$, its bus interface will automatically reset and release the SDA line. Bus communication frequency must be fast enough to prevent a reset during normal operation. The bus timeout feature only applies to when the DS75LV is holding SDA low. Other devices can hold SDA low for an undefined period without causing the interface to reset.

## Figure 9. 2-Wire Interface Timing



## ORDERING INFORMATION

| PART | TEMP RANGE | PACKAGE MARKING | PIN-PACKAGE |
|---|---|---|---|
| DS75LVS+ | -55°C to +125°C | DS75L* | DS75LV (150-mil) 8-SO |
| DS75LVS+T&R | -55°C to +125°C | DS75L* | DS75LV (150-mil) 8-SO, 2500 Piece Tape-and-Reel |
| DS75LVU+ | -55°C to +125°C | DS75L** | DS75LV 8-µSOP (µMAX) |
| DS75LVU+T&R | -55°C to +125°C | DS75L** | DS75LV 8-µSOP (µMAX), 3000 Piece Tape-and-Reel |
| DS75LVS | -55°C to +125°C | DS75L | DS75LV (150-mil) 8-SO |
| DS75LVS/T&R | -55°C to +125°C | DS75L | DS75LV (150-mil) 8-SO, 2500 Piece Tape-and-Reel |
| DS75LVU | -55°C to +125°C | DS75L | DS75LV 8-µSOP (µMAX) |
| DS75LVU/T&R | -55°C to +125°C | DS75L | DS75LV 8-µSOP (µMAX), 3000 Piece Tape-and-Reel |

** A "+" symbol is also marked on the package near the pin 1 indicator.*

***The DS75LV has a maximum operating voltage of 3.7V. Contact Dallas Semiconductor for information on the availability of a 3.7V to 5.5V version of the DS75LV.*

## PACKAGE INFORMATION

(For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)