National Semiconductor

PRELIMINARY
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DS90C241/DS90C124
5-35MHz DC-Balanced 24-Bit LVDS Serializer and Deserializer

General Description

The DS90C241/124 Chipset translates a 24-bit parallel bus into a fully transparent data/control LVDS serial stream with embedded clock information. This single serial stream simplifies transferring a 24-bit bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

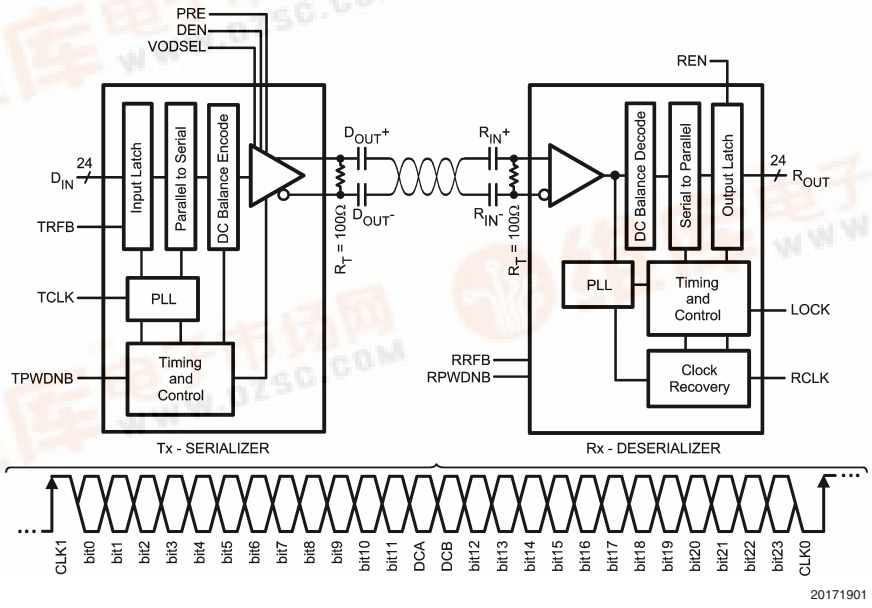
The DS90C241/124 incorporates LVDS signaling on the high-speed I/O. LVDS provides a low power and low noise environment for reliably transferring data over a serial transmission path. By optimizing the serializer output edge rate for the operating frequency range EMI is further reduced.

In addition the device features pre-emphasis to boost signals over longer distances using lossy cables. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects.

Features

- 5 MHz–35 MHz clock embedded and DC-Balancing 1:24 and 24:1 data transmissions
- User defined pre-emphasis driving ability through external resistor on LVDS outputs and capable to drive up to 10 meters shielded twisted-pair cable
- User selectable clock edge for parallel data on both TX and RX
- Supports AC-coupling interface
- Individual power-down controls for both TX and RX
- Embedded clock CDR (clock and data recovery) on RX and no external source of reference clock needed
- All codes RDL (random data lock) to support hot-pluggable applications
- LOCK output flag to ensure data integrity at RX side
- Balanced T_{SETUP}/T_{HOLD} between RCLK and RDATA on RX side
- PTO (progressive turn-on) LVTTL O/P to minimize the SSO effects
- All LVTTL inputs and control pins have internal pulldown except PRE
- On-chip filters for PLLs on TX and RX
- 48 pin TQFP package for both TX and RX
- Pure CMOS .35 µm process
- Power supply range 3.3V ± 10%
- Temperature range −40˚C to +105˚C
- 8 kV HBM ESD structure

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage	−0.3V to (V_{CC} +0.3V)
LVCMOS/LVTTL Output Voltage	−0.3V to (V_{CC} +0.3V)
LVDS Receiver Input Voltage	−0.3V to 3.9V
LVDS Driver Output Voltage	−0.3V to 3.9V
LVDS Output Short Circuit Duration	10 ms
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 seconds)	+260˚C
Maximum Package Power Dissipation Capacity Package De-rating:	
48L TQFP	$1/\theta_{JA}$ ˚CW above +25˚C
DS90C241	
θ_{JA}	45.8 (4L*); 75.4 (2L*) ˚C/W
θ_{JC}	21.0˚C/W
DS90C124	
θ_{JA}	45.4 (4L*); 75.0 (2L*)˚C/W
θ_{JC}	21.1˚C/W
	**JEDEC*
ESD Rating (HBM)	>8 kV
ESD Rating (ISO10605)	DS90C241 meets ISO 10605
Contact Discharge (D_{OUT+}, D_{OUT-}) to GND	±10 kV
Air Discharge (D_{OUT+}, D_{OUT-}) to GND	±30 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	˚C
Clock Rate	5		35	MHz
Supply Noise			±100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS							
V_{IH}	High Level Voltage		**Tx:** DIN[0:23], TCLK, DEN, TRFB, DCAOFF, DCBOFF, VODSEL **Rx:** RRFB, REN	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.7	−1.2	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±2	+10	µA
			Tx: TPWDNB **Rx:** RPWDNB	−20	±5	+20	µA
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA	ROUT[0:23], RCLK, LOCK	2.3	3.0	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA		GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−110	mA
I_{OZ}	TRI-STATE® Output Current	RPWRDN = 0.8V, V_{OUT} = 0V or V_{CC}	ROUT[0:23], RCLK, LOCK	−15	±0.4	+15	µA
LVDS DC SPECIFICATIONS							
V_{TH}	Differential Threshold High Voltage	V_{CM} = +1.2V	R_{IN+}, R_{IN-}			+100	mV
V_{TL}	Differential Threshold Low Voltage			−100			mV
I_{IN}	Input Current	V_{IN} = 2.4V, V_{CC} = 3.6V or 0V				±100	µA
		V_{IN} = 0V, V_{CC} = 3.6V or 0V				±100	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVDS DC SPECIFICATIONS							
V_{OD}	Output Differential Voltage $(D_{OUT+})-(D_{OUT-})$ *(Figure 16)*	R_L = 100Ω, w/o pre-emphasis VODSEL = L (VODSEL = H)	D_{OUT+}, D_{OUT-}	250 (500)	400 (800)	600 (1200)	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω, w/o pre-emphasis			10	50	mV
V_{OS}	Offset Voltage	R_L = 100Ω, w/o pre-emphasis		1.05	1.2	1.25	V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω, w/o pre-emphasis			10	50	mV
I_{OS}	Output Short Circuit Current	DOUT = 0V, DIN = H, TPWRDND = 2.4V		−35	−50	−70	mA
I_{OZ}	TRI-STATE Output Current	TPWRDND = 0.8V, DOUT = 0V or V_{DD}		−10	±1	10	µA
SER/DES SUPPLY CURRENT (DVDD*, PVDD* and AVDD* pins) ***Digital, PLL, and Analog VDDs***							
I_{CCT}	Serializer (Tx) Total Supply Current (includes load current)	R_L = 100Ω Pre-emphasis = OFF Checker-board pattern VODSEL=L *(Figure 1)*	f = 35 MHz		105		mA
		R_L = 100Ω RPRE = 6 kΩ Checker-board pattern VODSEL=L *(Figure 1)*	f = 35 MHz		120		mA
	Serializer (Tx) Total Supply Current (includes load current)	R_L = 100Ω R_{PRE} = OFF Random pattern VODSEL=L	f = 35 MHz		65		mA
		R_L = 100Ω R_{PRE} = 6 kΩ Random pattern VODSEL=L	f = 35 MHz		80		mA
I_{CCTZ}	Serializer (Tx) Supply Current Power-down	TPWRDNB = 0.8V			200	500	µA
I_{CCR}	Deserializer (Rx) Total Supply Current (includes load current)	C_L = 8 pF Checker-board pattern LVTTL Output *(Figure 2)*	f = 35 MHz		180		mA
	Deserializer (Rx) Total Supply Current (includes load current)	C_L = 8 pF Random pattern LVTTL Output	f = 35 MHz		110		mA
I_{CCRZ}	Deserializer (Rx) Supply Current Power-down	RPWRDND = 0.8V			500	750	µA

Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period		28.6	T	200	ns
t_{TCIH}	Transmit Clock High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	TCLK Input Transition Time			3	6	ns
t_{JIT}	TCLK Input Jitter	(Note 9)			±200	ns

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	LVDS Low-to-High Transition Time	R_L = 100Ω, C_L = 10 pF to GND VODSEL = L *(Figure 3)*		0.6		ns
t_{LHLT}	LVDS High-to-Low Transition Time			0.6		ns
t_{DIS}	DIN (0:23) Setup to TCLK	R_L = 100Ω, C_L = 10 pF to GND (Note 8)	5			ns
t_{DIH}	DIN (0:23) Hold from TCLK		5			ns
t_{HZD}	DOUT ± HIGH to TRI-STATE Delay	R_L = 100Ω, C_L = 10 pF to GND (Note 4) *(Figure 7)*		5		ns
t_{LZD}	DOUT ± LOW to TRI-STATE Delay			5		ns
t_{ZHD}	DOUT ± TRI-STATE to HIGH Delay			5		ns
t_{ZLD}	DOUT ± TRI-STATE to LOW Delay			5		ns
t_{PLD}	Serializer PLL Lock Time *(Figure 8)*	R_L = 100Ω		10		ms
t_{SD}	Serializer Delay *(Figure 9)*	R_L = 100Ω VODSEL = L, TRFB = H		3.5T + 2.85		ns
		R_L = 100Ω VODSEL = L, TRFB = L		3.5T + 2.85		ns

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	**R**eceiver out **C**lock **P**eriod (Note 8)	$t_{RCP} = t_{TCP}$	RCLK	28.6		200	ns
t_{RDC}	**R**CLK **D**uty **C**ycle		RCLK	45	50	55	%
t_{CLH}	**C**MOS/TTL **L**ow-to-**H**igh Transition Time	C_L = 8 pF (lumped load) *(Figure 4)*	ROUT [0:23], LOCK, RCLK		2.5	3.5	ns
t_{CHL}	**C**MOS/TTL **H**igh-to-**L**ow Transition Time				2.5	3.5	ns
t_{ROS}	**RO**UT (0:7) **S**etup Data to RCLK (Group 1) *(Figure 11)*		ROUT [0:7]		$(29/56)*t_{RCP}$	$(2/5)*t_{RCP}$	ns
t_{ROH}	**RO**UT (0:7) **H**old Data to RCLK (Group 1) *(Figure 11)*				$(27/56)*t_{RCP}$	$(2/5)*t_{RCP}$	ns
t_{ROS}	**RO**UT (8:15) **S**etup Data to RCLK (Group 2) *(Figure 11)*		ROUT [8:15], LOCK		$0.5*t_{RCP}$	$(2/5)*t_{RCP}$	ns
t_{ROH}	**RO**UT (9:15) **H**old Data to RCLK (Group 2) *(Figure 11)*				$0.5*t_{RCP}$	$(2/5)*t_{RCP}$	ns
t_{ROS}	**RO**UT (16:23) **S**etup Data to RCLK (Group 3) *(Figure 11)*		ROUT [16:23]		$(27/56)*t_{RCP}$	$(2/5)*t_{RCP}$	ns
t_{ROH}	**RO**UT (16:23) **H**old Data to RCLK (Group 3) *(Figure 11)*				$(29/56)*t_{RCP}$	$(2/5)*t_{RCP}$	ns
t_{HZR}	**H**IGH to TRI-STATE Delay	*(Figure 12)*	ROUT [0:23], RCLK, LOCK		3	10	ns
t_{LZR}	**L**OW to TRI-STATE Delay				3	10	ns
t_{ZHR}	TRI-STATE to **H**IGH Delay				3	10	ns
t_{ZLR}	TRI-STATE to **L**OW Delay				3	10	ns

Deserializer Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DD}	**D**eserializer **D**elay *(Figure 10)*		RCLK		[4+(3/56)]T+ 5.9		ns
			5 MHz		817	825	ns
			35 MHz		122	125	ns
t_{DRDL}	Deserializer PLL Lock Time from Powerdown	(Notes 7, 8)	5 MHz		5	12	ms
			35 MHz		5	10	ms
RxIN_TOL_L	**R**eceiver **IN**put **TOL**erance **L**eft, *(Figure 15)*	(Notes 6, 10)	5 MHz–35 MHz			0.25	UI
RxIN_TOL_R	**R**eceiver **IN**put **TOL**erance **R**ight, *(Figure 15)*	(Notes 6, 10)	5 MHz–35 MHz			0.25	UI

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: When the Serializer output is tri-stated, the Deserializer will lose PLL lock. Resynchronization MUST occur before data transfer.

Note 5: t_{DRDL} is the time required by the deserializer to obtain lock when exiting powerdown mode. t_{DRDL} is specified with an external synchronization pattern.

Note 6: RxIN_TOL is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. It is a measurement in reference with the ideal bit position, please see National's AN-1217 for detail.

Note 7: The Deserializer PLL lock time may vary depending on input data patterns and the number of transitions within the pattern.

Note 8: Guaranteed by Design (GBD) using statistical analysis.

Note 9: Total Interconnect Jitter Budget (t_{JI}) specifies the allowable jitter added by the interconnect assuming both transmitter and receiver are Auto SerDes circuits.

Note 10: UI – Unit Interval, equivalent to one ideal serialized data bit width. The UI scales with frequency.

Note 11: *Figures 1, 2, 9, 10, 13* show a falling edge data strobe (TCLK IN/RCLK OUT).

Note 12: *Figures 6, 11* show a rising edge data strobe (TCLK IN/RCLK OUT).

AC Timing Diagrams and Test Circuits

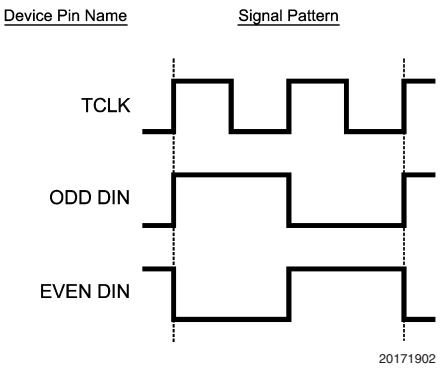


FIGURE 1. Serializer Input Checker-board Pattern

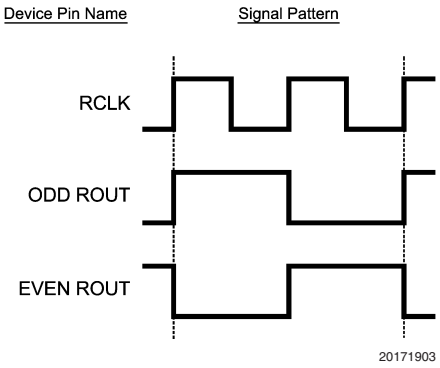


FIGURE 2. Deserializer Output Checker-board Pattern

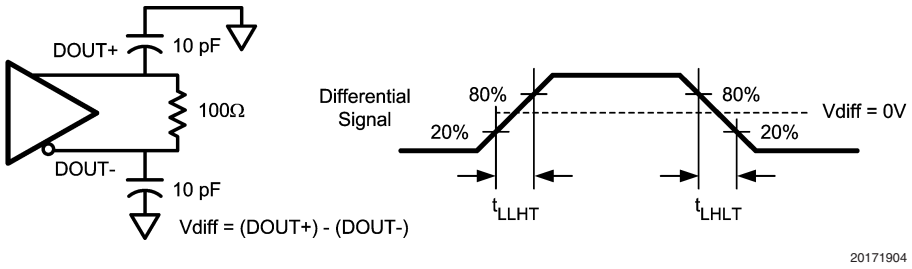


FIGURE 3. Serializer LVDS Output Load and Transition Times

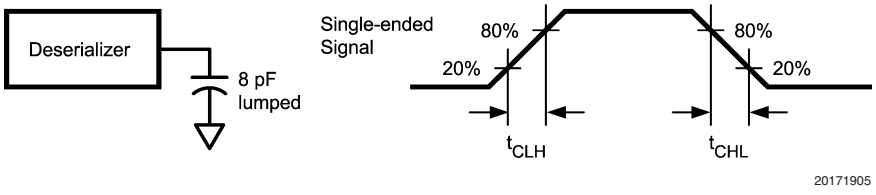


FIGURE 4. Deserializer LVCMOS/LVTTL Output Load and Transition Times

AC Timing Diagrams and Test Circuits (Continued)

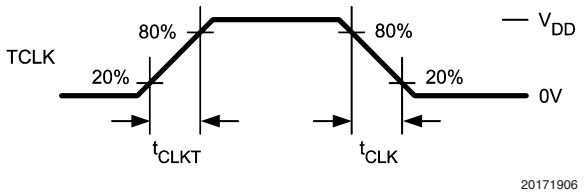


FIGURE 5. Serializer Input Clock Transition Times

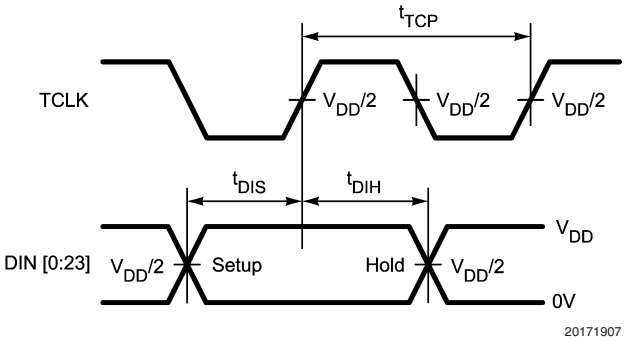


FIGURE 6. Serializer Setup/Hold Times

AC Timing Diagrams and Test Circuits (Continued)

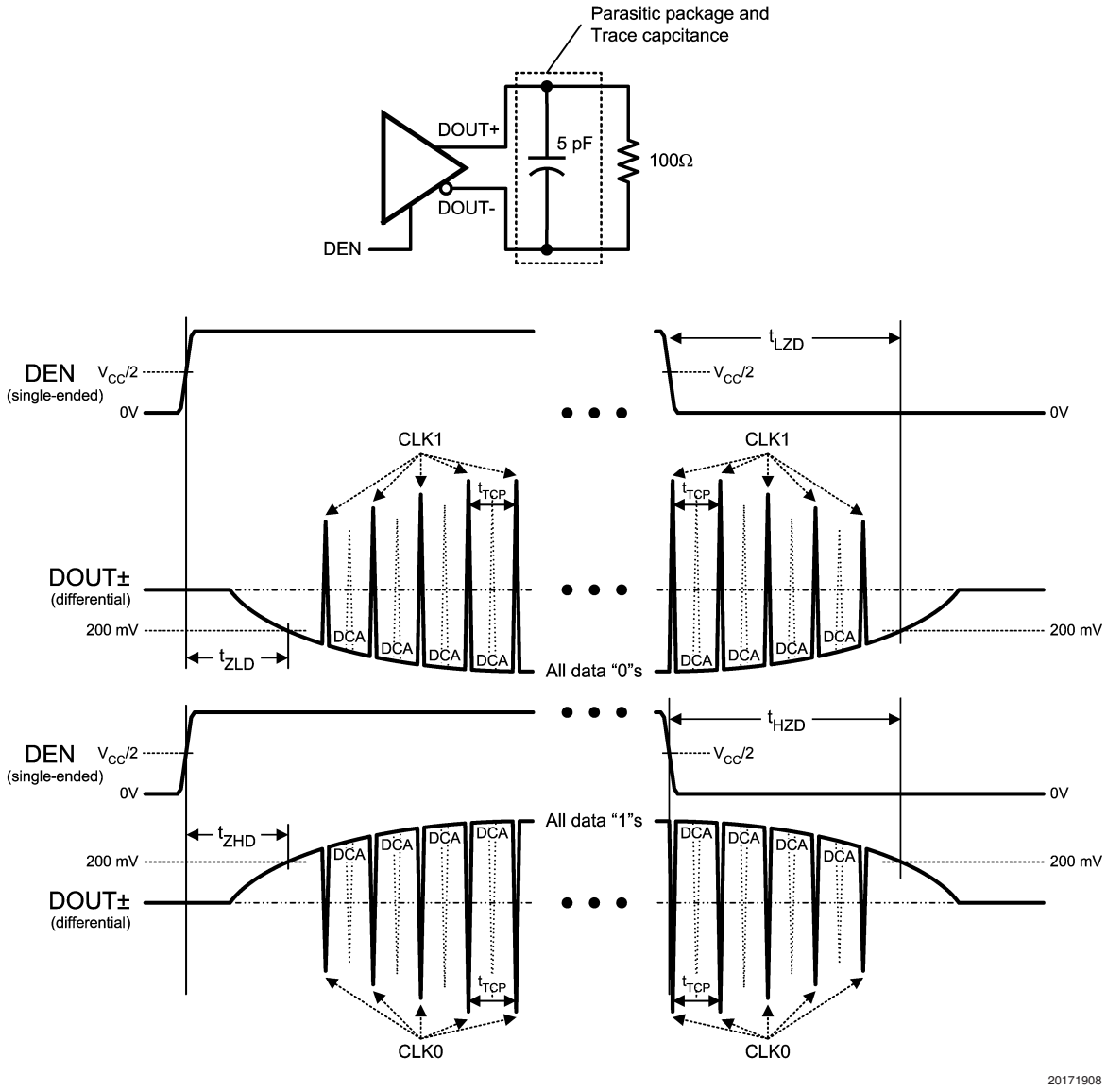


FIGURE 7. Serializer TRI-STATE Test Circuit and Delay

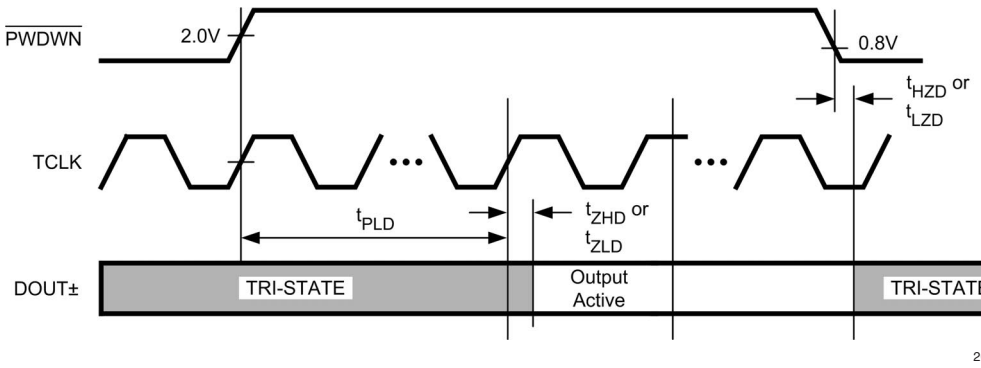


FIGURE 8. Serializer PLL Lock Time, and TPWDNB TRI-STATE Delays

AC Timing Diagrams and Test Circuits (Continued)

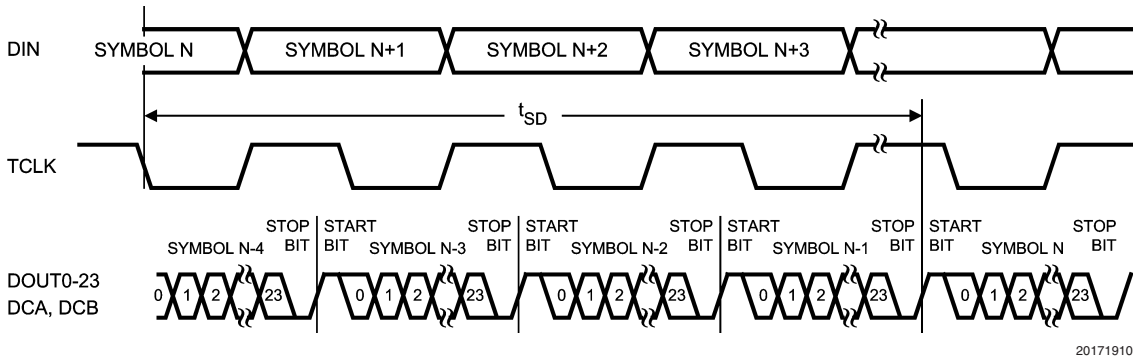


FIGURE 9. Serializer Delay

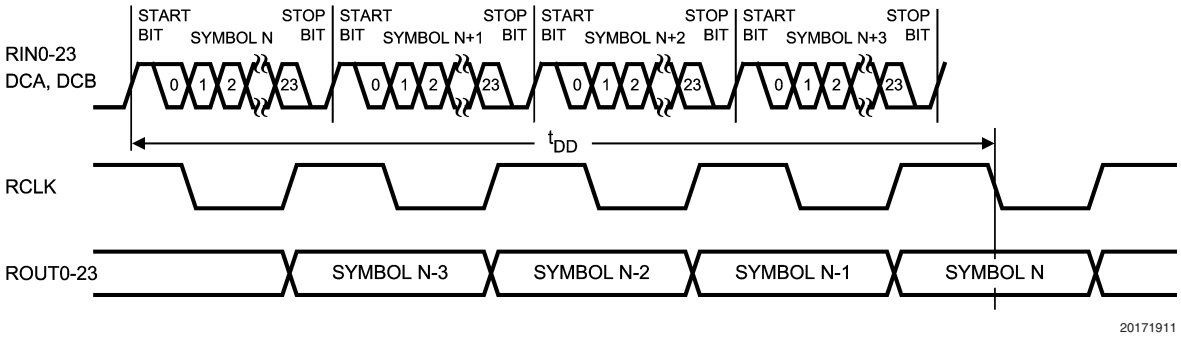


FIGURE 10. Deserializer Delay

AC Timing Diagrams and Test Circuits (Continued)

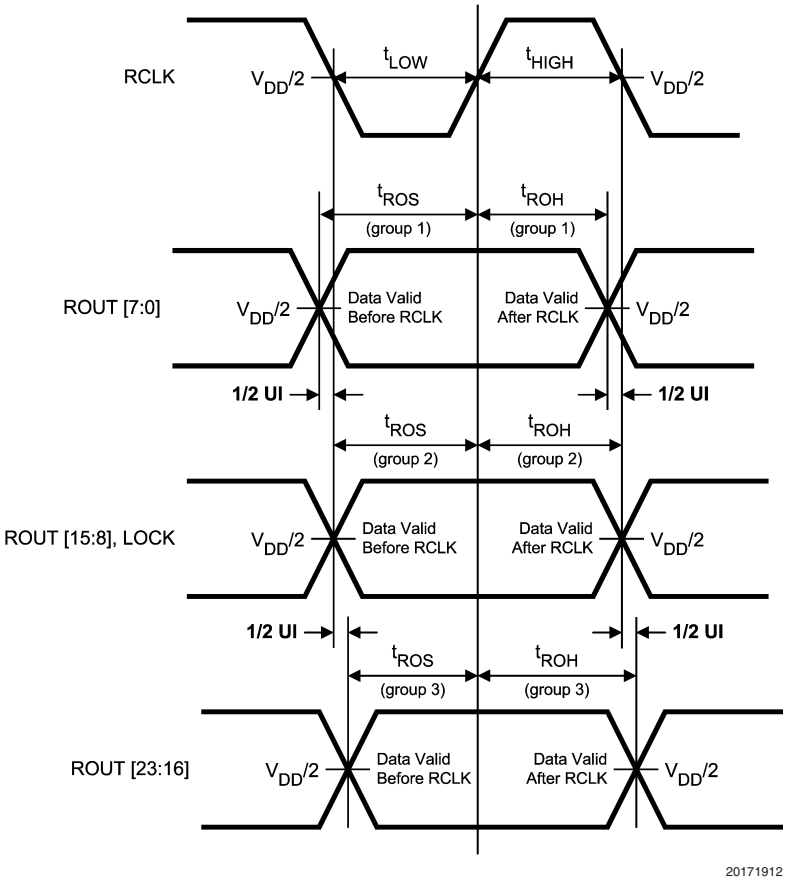
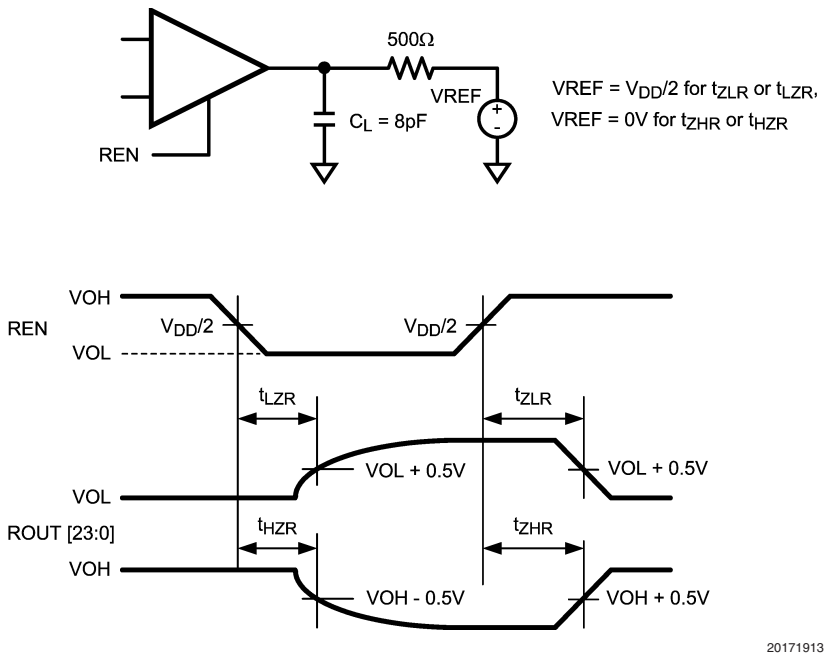


FIGURE 11. Deserializer Setup and Hold Times



Note: C_L includes instrumentation and fixture capacitance within 6 cm of ROUT[23:0]

FIGURE 12. Deserializer TRI-STATE Test Circuit and Timing

AC Timing Diagrams and Test Circuits (Continued)

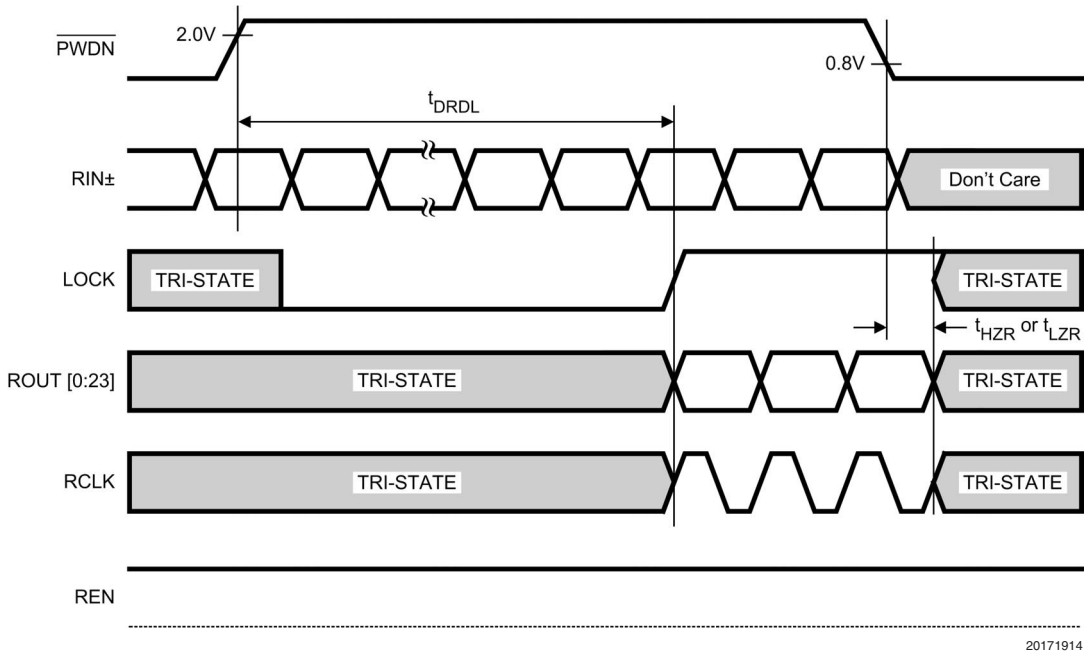


FIGURE 13. Deserializer PLL Lock Times and RPWDNB TRI-STATE Delay

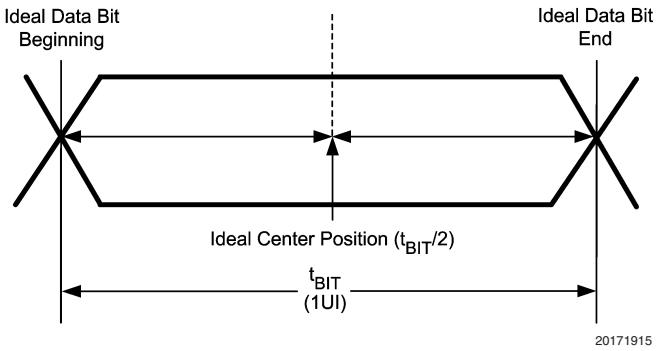


FIGURE 14. Transmitter Output Eye Opening

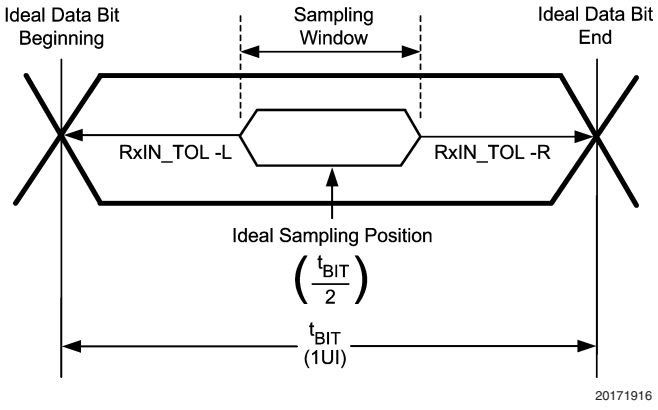
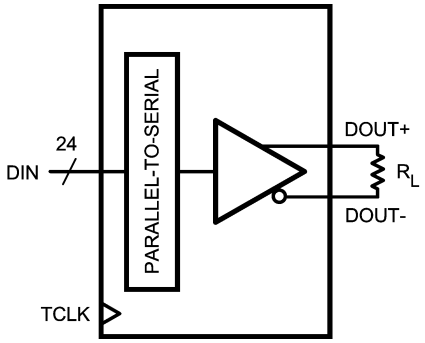


FIGURE 15. Receiver Input Tolerance (RxIN_TOL) and Sampling Window

AC Timing Diagrams and Test Circuits (Continued)



VOD = (D_{OUT+}) − $(D_{OUT\ -})$
Differential output signal is shown as (D_{OUT+}) − $(D_{OUT\ -})$, device in Data Transfer mode.

FIGURE 16. Serializer VOD Diagram

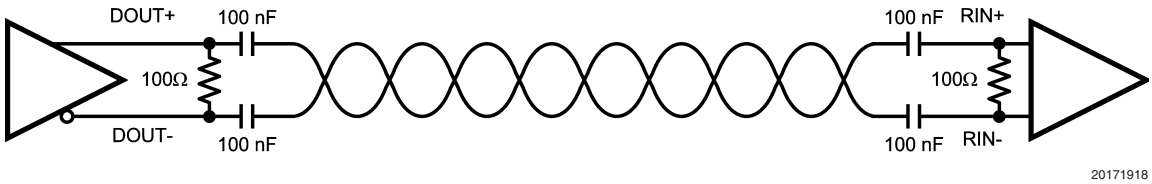


FIGURE 17. AC Coupled Application

Pin Descriptions

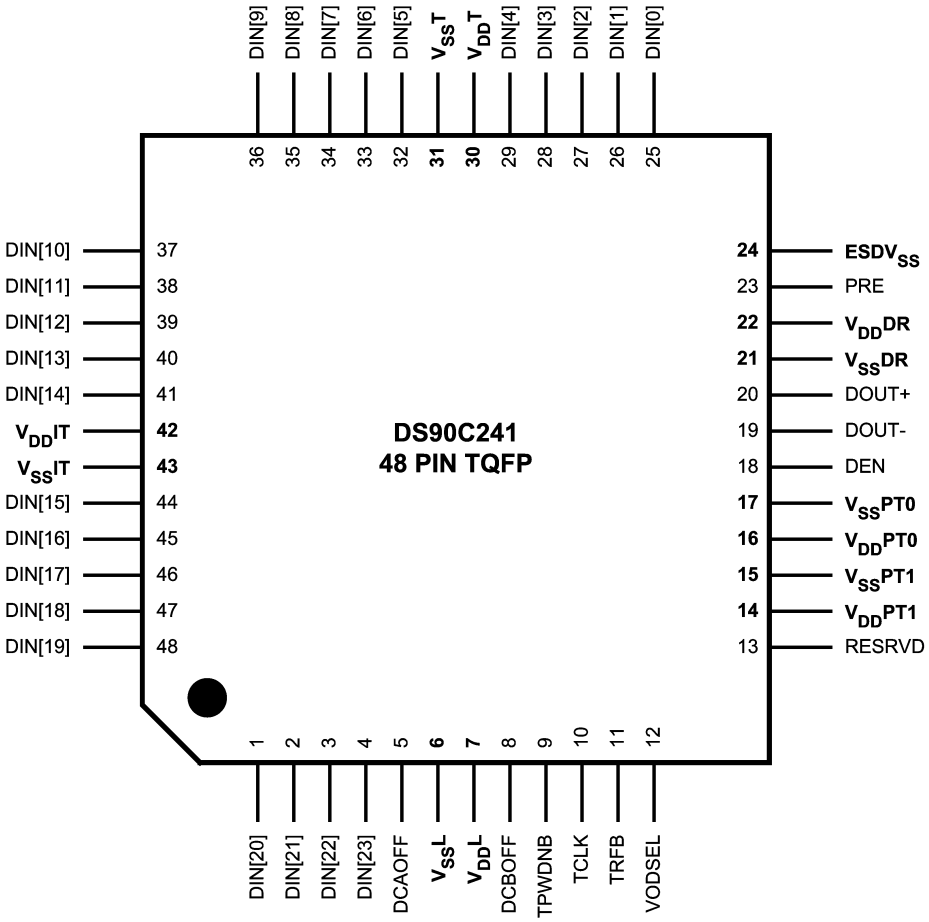
Pin #	Pin Name	I/O	Description
DS90C241 SERIALIZER PIN DESCRIPTIONS			
22	VDDDR	VDD	Analog **V**oltage Supply, LVDS O/P Power
21	VSSDR	GND	Analog Ground, LVDS O/P **G**round
16	VDDPT0	VDD	Analog **V**oltage supply, VCO Power
17	VSSPT0	GND	Analog ground, VCO **G**round
14	VDDPT1	VDD	Analog **V**oltage supply, **P**LL Power
15	VSSPT1	GND	Analog Ground, **P**LL **G**round
30	VDDT	VDD	Digital **V**oltage supply, **T**x serializer Power
31	VSST	GND	Digital Ground, **T**x serializer **G**round
7	VDDL	VDD	Digital **V**oltage supply, **T**x **L**ogic Power
6	VSSL	GND	Digital Ground, Tx Logic **G**round
42	VDDIT	VDD	Digital **V**oltage supply, **T**x **I**nput Power
43	VSSIT	GND	Digital Ground, Tx Input **G**round
24	VSSESD	GND	**ESD** Ground
4-1, 48-44, 41-32, 29-25	DIN[23:0]	CMOS_I	Transmitter **D**ata **IN**puts
10	TCLK	CMOS_I	**T**ransmitter reference **CL**oc**K**. Used to strobe data at the DIN inputs and to drive the transmitter PLL
9	TPWDNB	CMOS_I	**T**ransmitter **P**o**W**er **D**ow**N** **B**ar (ACTIVE L). TPWDNB = L; Disabled, DOUT (+/-) are TRI-STATED stand-by mode, PLL is shutdown TPWDNB = H; **E**nabled
18	DEN	CMOS_I	**D**ata **EN**able (ACTIVE H) DEN = L; Disabled, DOUT (+/-) are TRI-STATED, PLL still operational DEN = H; **E**nabled
13	RESRVD	CMOS_I	**RES**E**RV**E**D** - tie Low
23	PRE	CMOS_I	**PRE**-emphasis select pin. PRE = ($R_{PRE} \geq 3$ kΩ); I_{max} = (1.2/R*20), R_{min} = 3 kΩ PRE = H or floating; pre-emphasis off
11	TRFB	CMOS_I	**T**ransmitter **R**ising/**F**alling **B**ar Clock Edge Select (H = rising edge L = falling edge)
12	VODSEL	CMOS_I	**VOD** level **SEL**ect VODSEL = L; IOD ≈ 3.5 mA, (default). e.g. 3.5 mA*100Ω≈350 mV VODSEL = H; IOD ≈ 7.0 mA, VOD doubles approximately. e.g. 7 mA*100Ω ≈ 700 mV
5	DCAOFF	CMOS_I	RESERVED — tie Low
8	DCBOFF	CMOS_I	RESERVED — tie Low
20	DOUT+	LVDS_O	Transmitter LVDS true **(+) OUT**put
19	DOUT–	LVDS_O	Transmitter LVDS inverted **(-) OUT**put
DS90C124 DESERIALIZER PIN DESCRIPTIONS			
39	VDDIR	VDD	Analog LVDS **V**oltage supply, Power
40	VSSIR	GND	Analog LVDS **G**round
47	VDDPR0	VDD	Analog **V**oltage supply, **P**LL Power
46	VSSPR0	GND	Analog Ground, **P**LL **G**round
45	VDDPR1	VDD	Analog **V**oltage supply, **P**LL VCO Power
44	VSSPR1	GND	Analog Ground, **P**LL VCO **G**round
37	VDDR1	VDD	Digital **V**oltage supply, Logic Power
38	VSSR1	GND	Digital Ground, Logic **G**round
36	VDDR0	VDD	Digital **V**oltage supply, Logic Power
35	VSSR0	GND	Digital Ground, Logic **G**round
30	VDDOR1	VDD	Digital **V**oltage supply, LVTTL O/P Power

Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Description
DS90C124 DESERIALIZER PIN DESCRIPTIONS			
29	VSSOR1	GND	Digital Ground, LVTTL O/P **G**round
20	VDDOR2	VDD	Digital **V**oltage supply, LVTTL O/P Power
19	VSSOR2	GND	Digital Ground, LVTTL O/P **G**round
7	VDDOR3	VDD	Digital **V**oltage supply, LVTTL O/P Power
8	VSSOR3	GND	Digital Ground, LVTTL O/P **G**round
41	RIN+	LVDS_I	**R**eceiver **LVDS** true (+) **IN**put
42	RIN–	LVDS_I	**R**eceiver **LVDS** inverted **(–) IN**put
2	RESRVD	CMOS_I	**RES**E**RV**E**D** - tie Low
43	RRFB	CMOS_I	**R**eceiver **R**ising **F**alling **B**ar clock Edge Select RRFB = H; ROUT LVTTL O/P clocked on **R**ising CLK RRFB = L; ROUT LVTTL O/P clocked on **F**alling CLK
48	REN	CMOS_I	**R**eceiver **EN**able, (ACTIVE H) REN = L; Disabled, ROUT[23-0] and RCLK TRI-STATED, PLL still operational REN = H; **E**nabled
1	RPWDNB	CMOS_I	**R**eceiver **P**o**W**er **D**ow**N** **B**ar (ACTIVE L) RPWDNB = L; Disabled, ROUT[23-0], RCLK, and LOCK are TRI-STATED in stand-by mode, PLL is shutdown RPWDNB = H; **E**nabled
17	LOCK	CMOS_O	**LOCK** indicates the status of the receiver PLL LOCK = L; receiver PLL is unlocked, ROUT[23-0] and RCLK are TRI-STATED LOCK = H; receiver PLL is locked
25-28, 31-34	ROUT[7:0]	CMOS_O	**R**eceiver **O**utputs – Group 1
13-16, 21-24	ROUT[15:8]	CMOS_O	**R**eceiver **O**utputs – Group 2
3-6, 9-12	ROUT[23:16]	CMOS_O	**R**eceiver **O**utputs – Group 3
18	RCLK	CMOS_O	**R**ecovered **CL**oc**K**. Parallel data rate clock recovered from the embedded clock.

Pin Diagrams

Serializer - DS90C241



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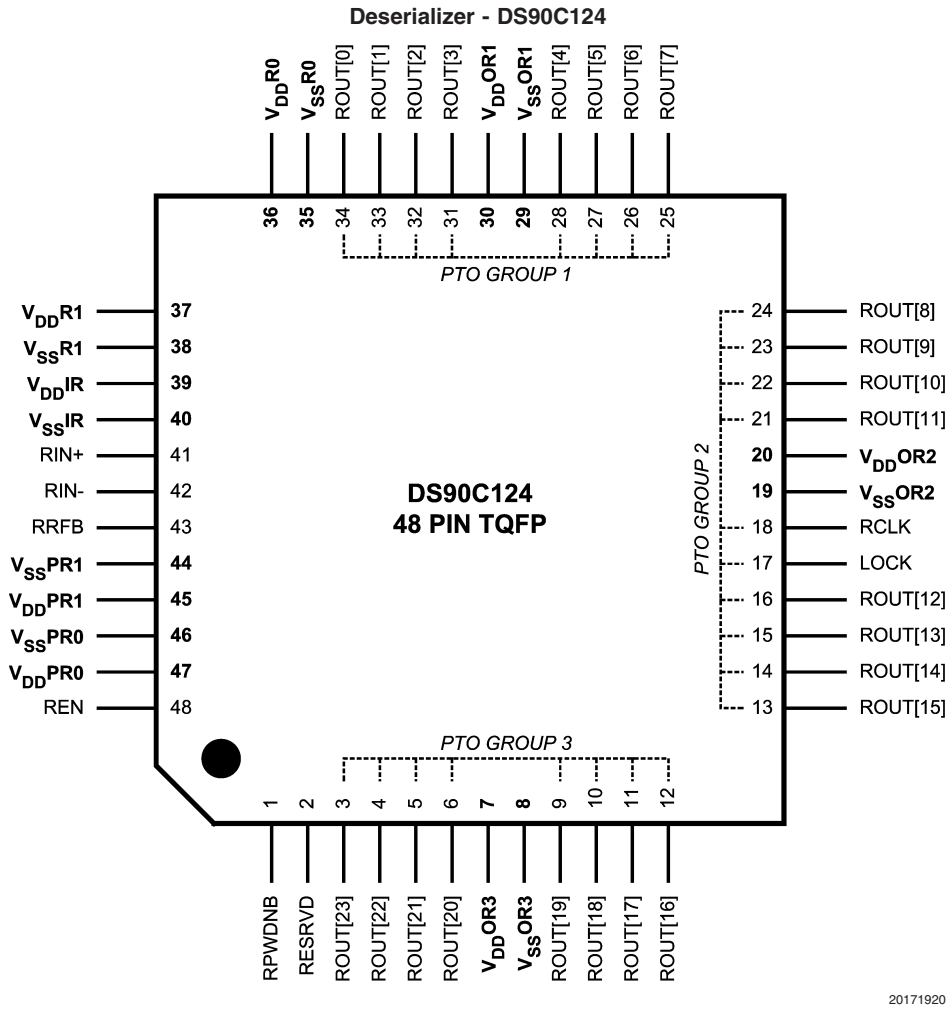
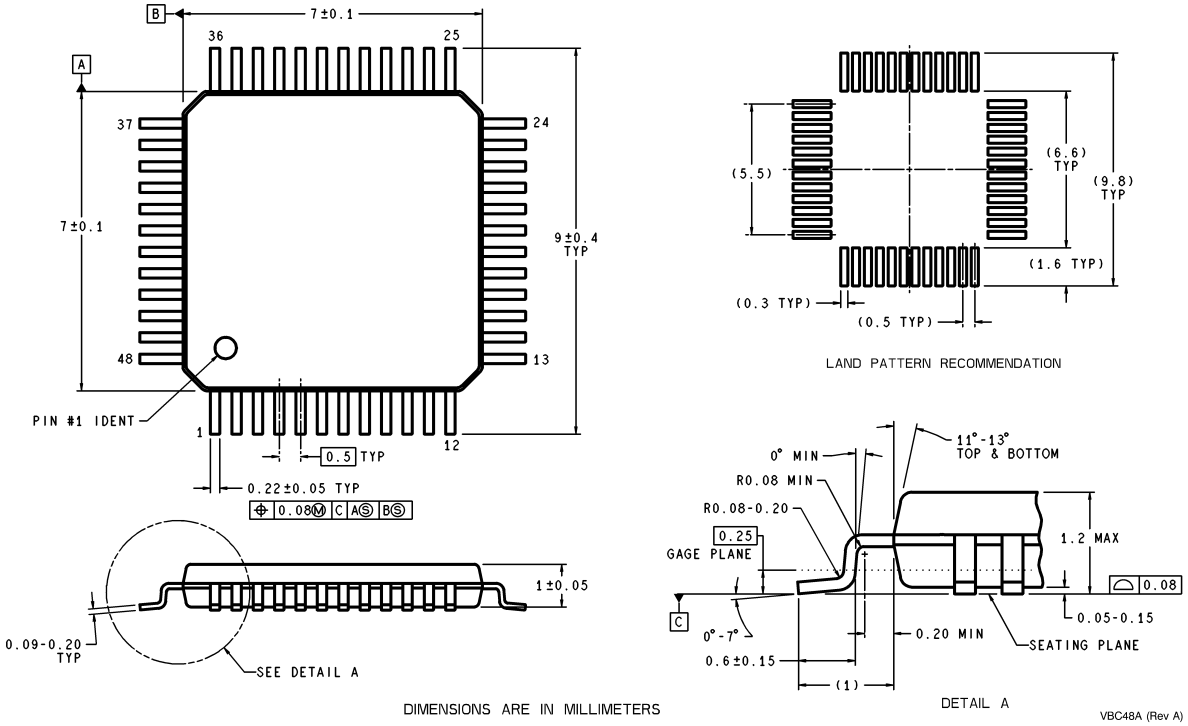
Pin Diagrams (Continued)



Physical Dimensions inches (millimeters) unless otherwise noted



Dimensions show in millimeters only
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NS Package Number IVS48

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