EB201/D

High Cell Density MOSFETs

Low On–Resistance Affords New Design Options

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ENGINEERING BULLETIN

Just a few years ago an affordable 60 V, 10 mΩ power transistor was a dream. After all, 10 mΩ is the resistance of about 20 cm of #22 gauge wire. Today a sub–10 mΩ power MOSFET is not only available, it is housed in a standard TO–220. Such are the advances that have occurred lately in "high cell density" power MOSFET technology. Furthermore, Motorola's high cell density technology, HDTMOS®, brings other advantages such as greatly improved body diode performance. The technological advances are sufficiently great that they are fundamentally changing low voltage power transistor technology.

Cutting the MOSFET's On–Resistance

A cross section of the power MOSFET is shown in Figure 1. The major contributors to the standard MOSFET's on–resistance are its spreading, channel, JFET, accumulation region, and substrate resistances. To achieve ultra–low $R_{DS(on)}$, device designers must decrease the resistance of all these components. Most of the resistive elements can be reduced by shrinking cell size and adding more cells per square centimeter of silicon. However, there is a limit to maximum packing density. As cell density becomes very high, on–resistance actually increases due to a higher JFET resistance. With today's processes and cell geometries, the optimum cell density is about five times that of standard power MOSFETs. Devices built with ON Semiconductor's high cell density process (HDTMOS) employ about 6 M cells/in^2, up from the 1.2 M cells/in^2 used in standard power MOSFETs. Figure 2 illustrates the marked difference in cell density.

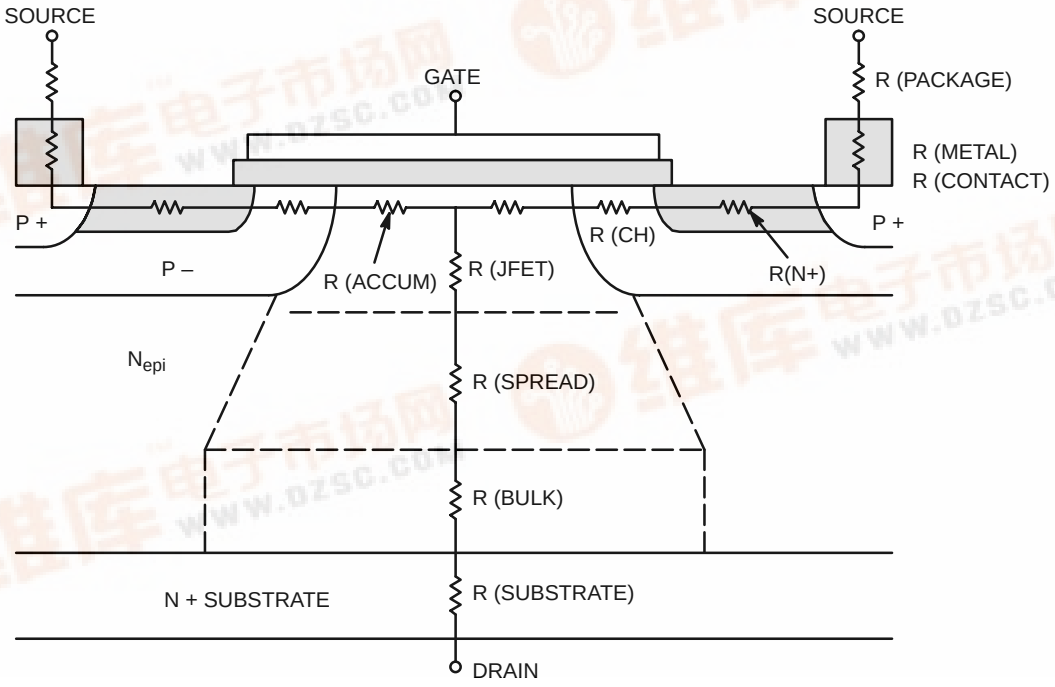

Figure 1. HDTMOS Cross Section

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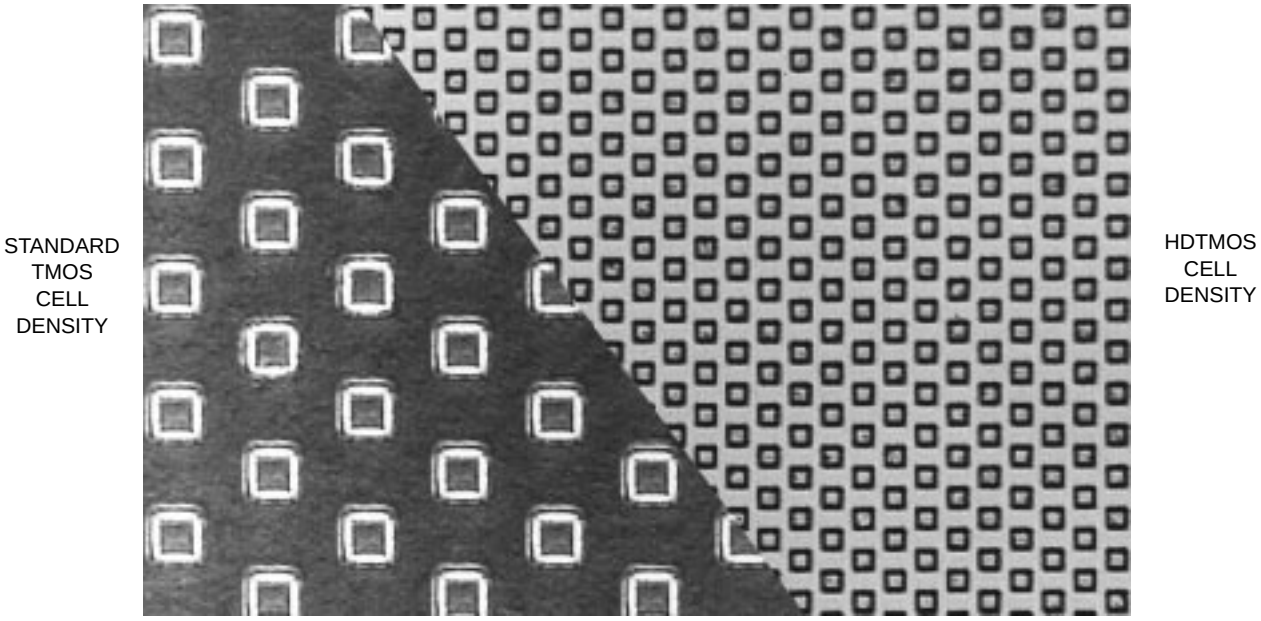

Figure 2. HDTMOS versus Standard TMOS™ Cell Densities

Also a key factor in lowering on–resistance is the use of low resistivity substrates. The substrate of the power MOSFET can be thought of as the mechanical base onto which the transistors are built. Although it comprises almost all of the wafer thickness, its only purpose is to strengthen the wafer for its trip through wafer processing, dicing, and final assembly. The resistance added by the substrate is entirely undesirable, and low resistivity substrates are a must for ultra–low on–resistance MOSFETs. Figure 3 compares the major on–resistance components of HDTMOS to those of standard cell MOSFETs.

The on–resistance area product is a good figure of merit for the power MOSFET, and lower is better for this parameter. The original 28 mΩ, 60 V MOSFET had an on–resistance area product of about 7.0 mΩ–cm^2 (based on the maximum on–resistance rating at 25°C). Die size reductions over the last several years have shaved the product to about 5.5 mΩ–cm^2. The newest device, the MTP75N05HD, is more than a refinement of typical power MOSFET technology. Its 2.4 mΩ–cm^2 product was attained by completely redesigning the device and developing an entirely new manufacturing process.

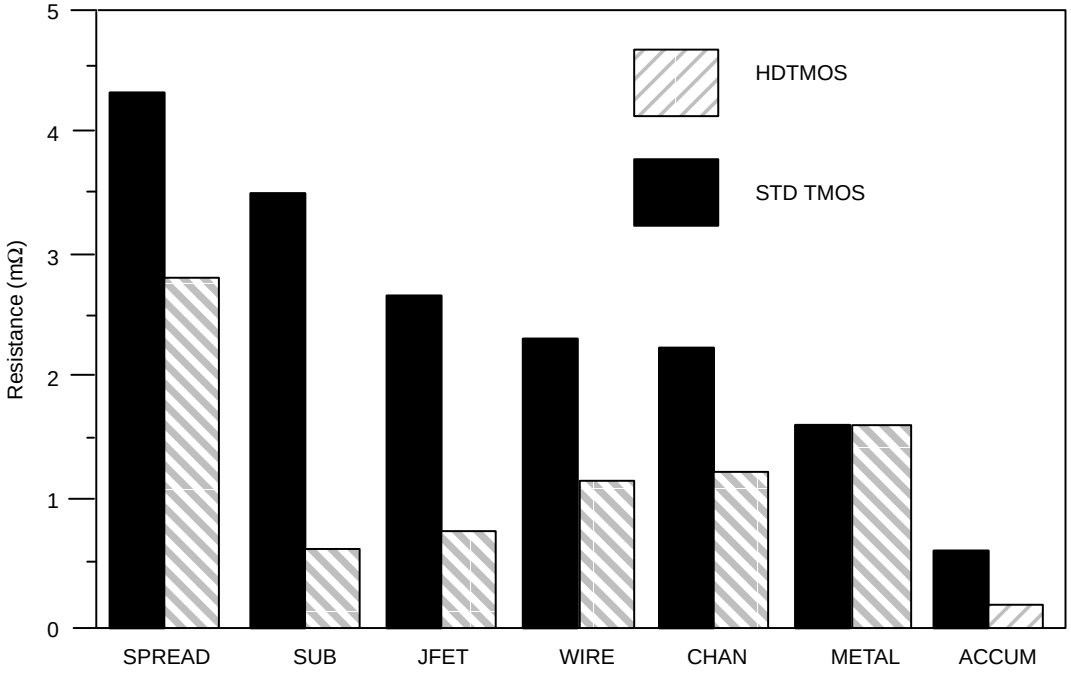

Figure 3. On–Resistance Components

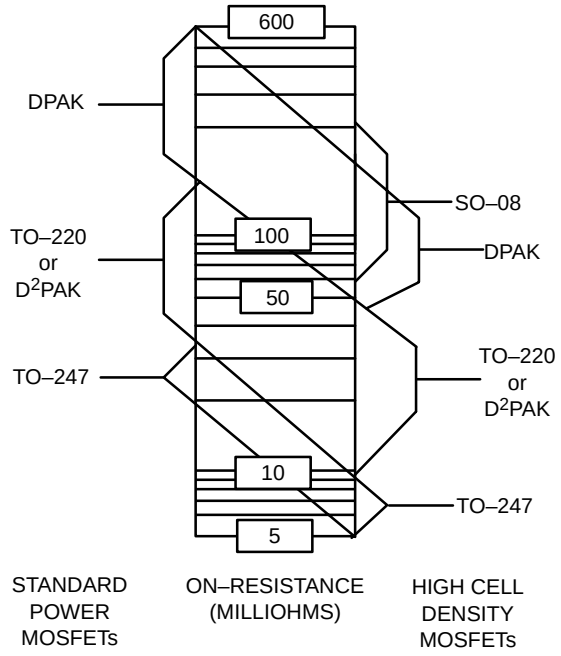

Figure 4. Packaging Options Given $R_{DS(on)}$

A note of caution regarding the use of on–resistance area products is worthwhile. Lateral DMOS devices have been shown to have a low on–resistance area product based on active area, that is, actual MOSFET cell area excluding gate feeds, bond pads, wirebonds, etc. However, because lateral DMOS processes have no thick metal capability and because both the drain and the source contacts must be routed on the surface of the chip, LDMOS structures pay a high penalty for bussing current on and off the chip. Based on total device on–resistance, present LDMOS devices have about three times the on–resistance–area product of the newest vertical devices such as the MTP75N05HD.

Manufacturing High Cell Density MOSFETs

Producing power MOSFETs with greater than 2 million cells per square inch requires an alternative manufacturing method. A process used for VLSI devices is employed to reduce cell size and create higher cell densities. The high resolution of this process is achieved by utilizing positive photoresist and 5X step–and–repeat projection aligners. In this process the mask is made 5 times larger to gain line width resolution. Then, when the image is projected onto the wafer, it is demagnified 5 times, leaving a crisp and highly resolvable image. The mask is then stepped along the wafer, and the process is repeated. Together with VLSI design rules and shallow junction depths, this self–aligned process is capable of producing cell densities greater than 5.5 million cells per square inch.

Using the On–Resistance Advantage of HDTMOS

There are several ways to utilize high cell density technology, but the most attractive is to extend the current capability of a given power transistor package. For example, as a TO–220 goes from a 28 mΩ to a 14 mΩ or 10 mΩ device, designers can use the lower on–resistance to reduce junction temperature and improve system efficiency, or to increase the current capacity of the system. Figure 4 shows how the on–resistance range of popular packages changes with the introduction of HDTMOS.

The on–resistance reductions and specifications suggests one clear use of the technology: applications may be able to move from larger to smaller packages, which cuts the cost of the package and decreases the required heatsink or circuit board area. A good example of this is the 14 mΩ TO–247. Until very recently, the only way to achieve such low on–resistance was to build a large die (on the order of 256 by 256 mils) and place it in the TO–247, which is quite a large and expensive package. Using HDTMOS, a 14 or even 10 mΩ die can fit into a TO–220. The smaller, more popular TO–220 package brings a strong cost advantage.

Similarly, designers may be able to remove a device from a heatsink and use a free standing device or one that can be surface mounted instead. An example of this is replacing a TO–220 with a DPAK (TO–252), or more likely, with a D^2PAK, which are both popular surface mount packages. As the on–resistance of the DPAK falls from around 120 to about 40 mΩ and the D^2PAK's $R_{DS(on)}$ collapses to 10 mΩ, some engineers will no doubt prefer the smaller, more easily mountable packages. The development of HDTMOS is timely since it coincides with the steady improvements in surface mount substrates (such as metal core boards) which allow much higher power dissipation. Taken together, the mechanical and electrical advances can significantly boost current handling capability of a surface mount module.

Estimates of the current capability of several packages are shown in Table 1. Calculations are based on the largest die that a package will house, and the on–resistance of some of the SO–8s and the DPAKs are projected. On–resistance–area products of the smallest die sizes are slightly larger than those of large die sizes due to a disproportionate penalty for edge terminations, wirebond pads, and routing of gate feeds. The analysis is based on a maximum junction temperature appropriate for the mounting substrate, i.e., devices on heat sinks were allowed to reach a junction temperature of 150 or 175°C, whereas surface mount devices were limited to 125°C. Junction to ambient thermal resistance which was used is typical of the particular mounting method. The first column of figures shows the maximum rated on–resistance at 25°C. The second column shows an estimate of the maximum allowable current at a junction temperature of either 175 or 125°C, depending on the mounting method. The calculations show that HDTMOS gives about a 50% increase in maximum allowable current.

Another way to compare standard MOSFET technology and HDTMOS is to note the junction temperature of each device at a given load current and ambient temperature. Column 2 of Table 1 shows that HDTMOS will run about 30 to 60°C cooler than a standard power MOSFET of equivalent die area. Load current is assumed to be the amount of current needed to push the HDTMOS device to 125 or 150°C, depending on mounting method.

Table 1. Current Handling Capability and Junction Temperature Comparison

Devices	Max $R_{DS(on)}$ @ 25°C (mΩ)	Max Current (Amps)	Junction Temperature (°C)
HDTMOS TO–220	10	21(1)	150(2)
STD TO–220	21	15(1)	180(2)
HD DPAK on FR4	45	3.6(3)	125(4)
STD DPAK on FR4	100	2.2(3)	185(4)
HD D^2PAK on FR4	10	7.1(5)	125(6)
STD D^2PAK on FR4	21	5.0(5)	185(6)
HD D^2PAK on Thermal Clad®	10	15.3(7)	125(8)
STD D^2PAK on Thermal Clad	21	10.7(7)	185(8)
HD 8–Pin SOIC (1 of 2 Die)	64	2.2(9)	125(10)
STD 8–Pin SOIC (1 of 2 Die)	132	1.6(9)	185(10)

1. Largest die available in a TO–220, $R_{\Theta JC}$ = 1.0°C/W, $R_{\Theta CA}$ = 5.0°C/W, T_{amb} = 125°C, T_{max} = 175°C.
2. Largest die available in a TO–220, $R_{\Theta JC}$ = 1.0°C/W, $R_{\Theta CA}$ = 5.0°C/W, T_{amb} = 125°C, I_d = 15.5 A.
3. Largest die available in a DPAK, $R_{\Theta JC}$ = 3.12°C/W, $R_{\Theta CA}$ = 50°C/W, T_{amb} = 85°C, T_{board} = 125°C max.
4. Largest die available in a DPAK, $R_{\Theta JC}$ = 3.12°C/W, $R_{\Theta CA}$ = 50°C/W, T_{amb} = 85°C, I_d = 3.6 A.
5. Largest die available in a D^2PAK, $R_{\Theta JC}$ = 1.0°C/W, $R_{\Theta CA}$ = 50°C/W, T_{amb} = 85°C, T_{board} = 125°C max.
6. Largest die available in a D^2PAK, $R_{\Theta JC}$ = 1.0°C/W, $R_{\Theta CA}$ = 50°C/W, T_{amb} = 85°C, I_d = 7.1 A.
7. Largest die available in a D^2PAK, $R_{\Theta JC}$ = 1.0°C/W, $R_{\Theta CA}$ = 10°C/W, T_{amb} = 85°C, T_{board} = 125°C max.
8. Largest die available in a D^2PAK, $R_{\Theta JC}$ = 1.0°C/W, $R_{\Theta CA}$ = 10°C/W, T_{amb} = 85°C, I_d = 15.3A.
9. Largest die available in an 8–pin SOIC, $R_{\Theta JC}$ = 5.0°C/W, $R_{\Theta CA}$ = 75°C/W, T_{amb} = 85°C, T_{board} = 125°C max.
10. Largest die available in an 8–pin SOIC, $R_{\Theta JC}$ = 5.0°C/W, $R_{\Theta CA}$ = 75°C/W, T_{amb} = 85°C, I_d = 2.2 A.

Behavior of Intrinsic Diode

The switching characteristics of the MOSFET's body diode are very important in systems such as PWM (pulse width modulated) motor controllers that use it as a freewheeling, or commutating diode. Of particular interest are the diode's reverse recovery characteristics, which play a major role in determining radiated and conducted noise as well as switching losses.

As a minority carrier device, the body diode takes a finite time, t_{rr}, to switch from forward conducting to reverse blocking due to the storage of minority carrier charge, Q_{rr}. A typical waveform showing Q_{rr}, t_{rr}, t_a, and t_b is shown in Figure 5. Q_{rr}, t_{rr}, t_a, and t_b are a function of the forward current and the rate at which the diode is switched, or applied di/dt. The abruptness or snappiness of diode recovery is best described by the ratio t_b/t_a. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy. Another key characteristic to note is that the diode will not support reverse voltage until the peak reverse recovery current is reached. It is these above mentioned characteristics that determine commutation losses and noise.

Because the diode will not support voltage until the peak reverse recovery current is reached, the transistor that is turning on and diverting current from the diode (usually the transistor in the opposite leg of a 1/2 bridge) takes the brunt of the commutation losses. The diode incurs little power dissipation until the relatively brief t_b time. Obviously, repeatedly forcing the diode through reverse recovery increases transistor power dissipation. Therefore, in PWM applications one would like a diode with short t_{rr} and low Q_{rr} to minimize these losses.

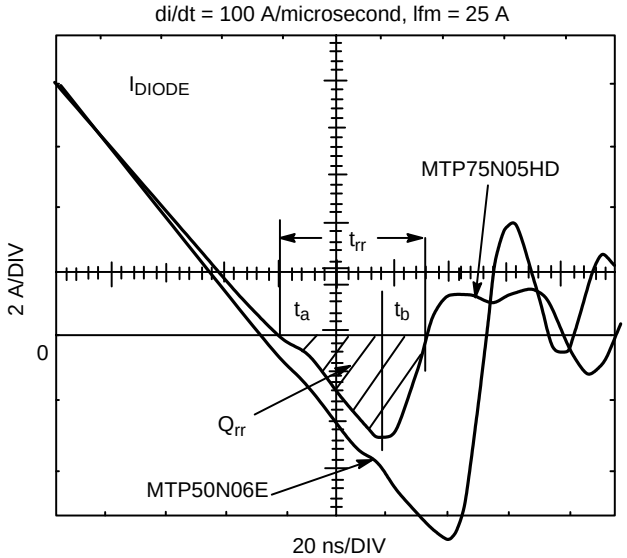

Figure 5. Diode Reverse Recovery Comparison

Cutting switching losses is easily accomplished by boosting switching speeds; however, the repercussions of this strategy must be carefully considered. Sharpening the switching edges generates more electrical noise. The mechanisms at work are finite irremovable parasitic inductances and capacitances acted upon by high di/dt's and dv/dt's. The diode's negative di/dt during t_a is directly controlled by the transistor clearing the stored charge. However, the positive di/dt during t_b is more dependent on the diode itself, the maximum reverse recovery current, and parasitic circuit elements. The abrupt edges during t_b induce

ringing in the parasitic components. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise. So, although the diode recovery time is only a fraction of the total commutation time, the noise generated by the diode's abruptness limits commutation speeds and determines system switching losses.

Compared to the diodes of standard cell density MOSFETs, ON Semiconductor's high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge, and have a softer reverse recovery (Figure 5). Figure 6 shows that some high cell density devices are just as noisy as their predecessors. The softness advantage of HDTMOS diodes means they can be forced through reverse recovery at a higher di/dt than that of a standard cell MOSFET diode without increasing the current ringing or generating more noise. Generalizing about how much faster the new diodes can be commutated is difficult since the t_b time is in part a function of circuit layout. However, a maximum reduction of about 50% seems feasible.

One precaution required when using the body diode of a high cell density device is that its forward voltage, v_f, is approximately 1 V at elevated current, which is typical of a p–n junction. Compared to the MOSFET's $V_{ds(on)}$, v_f is likely to be high. So if the diode's duty cycle is high, the on–state losses of the diode must be considered. The diode's high forward voltage can be decreased by turning on the MOSFET when its diode is to conduct. With the gate on, current flows through the channel (source–to–drain), and the voltage drop is equal to that of the MOSFET in its conventional direction.

Switching Speed and Ruggedness

Except for on–resistance and body diode performance, high cell density devices are very similar to existing MOSFET technology. For example, the output characteristics and gate charge curves of high cell density devices have the same general characteristics as those of standard devices. For a given die size, HDTMOS devices require more gate charge than their standard counterparts. However, for a given on–resistance, HDTMOS devices have lower gate charge and they switch faster. Standard and high cell density gate charge waveforms, those of the MTP50N05E (28 mΩ, 163 mils by 200 mils) and the MTP75N05HD (9.5 mΩ, 170 mils by 220 mils), are shown in Figure 7.

Figures 8 and 9 show the switching behavior of the MTP50N05E and the MTP75N05HD. The HDTMOS device is slower due to its higher per unit area input capacitance and larger die area. Had the comparison been based on the same on–resistance, it would have favored the HDTMOS device.

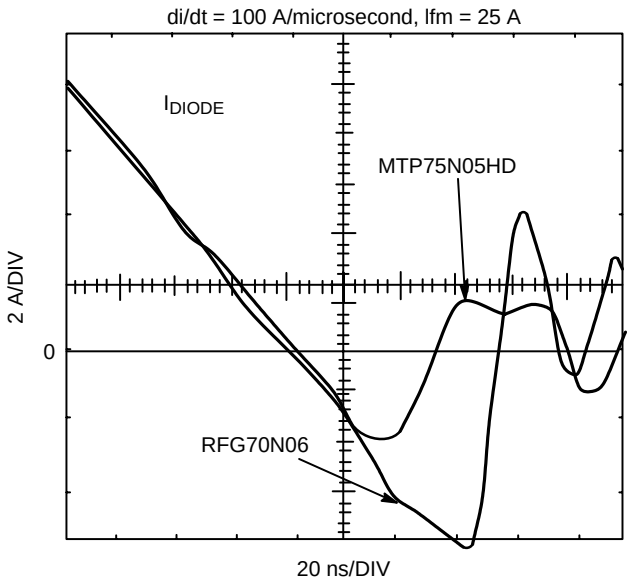

Figure 6. Diode Reverse Recovery Compared to Competition

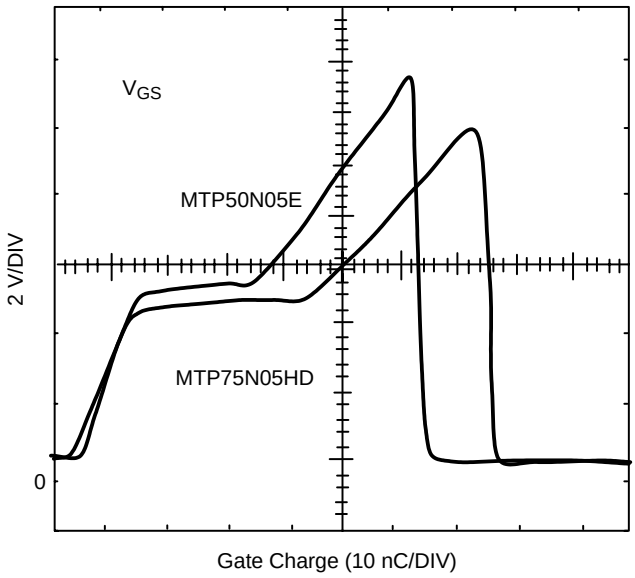

Figure 7. Gate Charge Comparison Between Standard TMOS and HDTMOS

Today's reliability requirements mandate that all new high current MOSFETs be rugged with respect to overvoltage transients that might appear across the drain–source of the MOSFET. They must be able to handle avalanche currents of at least their continuous current rating. HDTMOS devices are no exception to this rule. The ruggedness of both standard and HDTMOS are limited by maximum junction temperature, so for a given die area, they have roughly the same unclamped inductive switching capability.

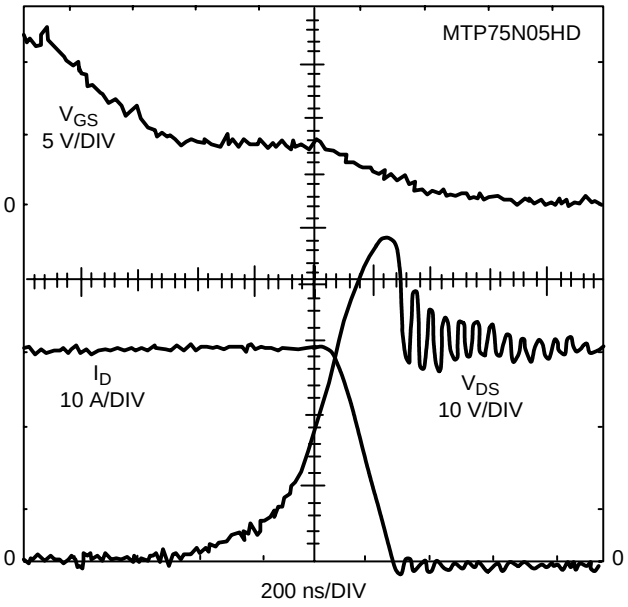

Figure 8. MTP75N05HD Clamped Inductive Turn–Off

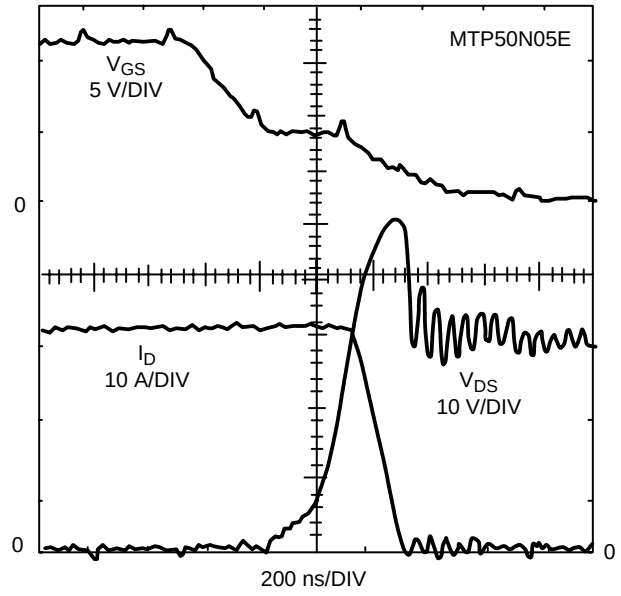

Figure 9. MTP50N05E Clamped Inductive Turn–Off

On–Resistance/Die Size Tradeoffs

When replacing an existing MOSFET with a high cell density device with the same on–resistance, designers must consider the implications of using a smaller die size. Since the die size is cut by a factor of 40 to 50%, pulsed energy capability will be affected. The ability to handle energy transients such as overvoltage transients or fault currents is to the first order proportional to die area. Therefore, for a given on–resistance standard devices are inherently more robust.

The smaller die size of HDTMOS may affect the system's thermal performance, but that depends on the system's thermal profile. Compared to a standard cell MOSFET, a high cell density MOSFET will have around twice the junction–to–case thermal resistance. That difference is in the range of 0.5 to 1.5°C/W. If the system's total junction to ambient thermal resistance ($R_{\Theta JA}$) is very good, less than 5°C/W for example, then the added thermal resistance will alter the junction temperature significantly. If the junction to ambient thermal resistance is very high, 50°C/W for example, as it might be in a surface mount application, then the added junction–to–case thermal resistance is not a problem. These thermal issues reinforce the perception that the best use of high cell density MOSFETs is in new, higher current devices and in surface mount applications where the objective is to avoid generating heat.

Best Uses of High Cell Density MOSFETs

Designers are considering using high cell density technology in many applications. The need for an improved power transistor usually centers around a new and difficult design goal such as reducing module size while maintaining or increasing functionality. The need for lower voltage drop (to ensure that maximum voltage appears at the load) or higher efficiency are other common reasons cited for using very low on–resistance MOSFETs. Cutting costs is another reason for using HDTMOS. Costs can be cut if the power transistor can be housed in a simpler package or if the module's packaging or assembly can be simplified. For example, HDTMOS may allow using all surface mount components, or a heatsink may be able to be downsized or removed.

Specific applications for HDTMOS include motor control, solid state relays, battery operated equipment such as laptop computers or cordless tools, synchronous rectifiers for power conversion, and replacement of ORing diodes in computer systems.

Cost

The advent of a new technology does not bring widespread use unless it is cost effective, so high cell density devices must be competitive with standard power MOSFETs. Compared on a cost per ampere basis, high cell density devices fair well. Since there are no major cost savings in replacing standard MOSFETs that already have a small die size, and due to the problems associated with switching from a standard to a high cell density device, the HDTMOS product family will focus on lower on–resistances that are currently not available in standard technology. Next, HDTMOS will be used to replace standard devices which require large die area such as the MTP50N06E. Current plans are to offer HDTMOS replacements for on–resistances up to 40 mΩ.

Table 2. Relative Size of On–Resistance Components

On–Resistance Component	1000 V Standard MOSFET	250 V Standard MOSFET	50 V Standard MOSFET	50 V, High Cell Density MOSFET
Channel	0.4%	5.1%	40.5%	20.3%
Accumulation	0.1%	1.6%	12.6%	5.5%
JFET	8.3%	19.1%	12.7%	16.3%
EPI	91.1%	72.5%	20.1%	34.2%
Substrate	0.1%	1.7%	14.1%	23.7%

SMARTDISCRETES™ Features on HDTMOS Devices

The HDTMOS process is compatible with ON Semiconductor's SMARTDISCRETES process. The features available in the SMARTDISCRETES process include SENSEFET™s, gate–source Zener protection, gate–drain Zener clamps for self clamping of drain–to–source transients, and over current limits. Also, there is the potential for fault flags and overtemperature shutdown. Of these features gate–source protection Zeners are the most likely option to be used in HDTMOS. Adding the Zeners has little impact on die size and processing complexity. Series gate resistors can be added to enhance the gate's ESD capability and to limit the maximum switching speeds so that RFI and EMI are bounded.

The wisdom of adding other SMARTDISCRETES features is questionable. SENSEFETs are not likely since it is difficult to generate measurable and accurate sense voltages with a very low on–resistance device. Adding an overcurrent limit is unlikely since the feature requires a resistor placed in series with the source, which runs contrary to all the reasons for selecting high cell density in the first place. Overtemperature shutdown and self clamping of voltage transients at the drain are envisioned as features for specialized devices and not for the entire product line.

Voltage Ratings

High cell density MOSFETs are limited in the range of voltages that they serve. There are few high current applications requiring voltages below 12 V, so that defines one end of the HDTMOS voltage spectrum. Presently, the other end of the voltage range is at best 100 V and possibly only 60 V. As the MOSFET's breakdown voltage increases, more of the on–resistance appears in the epitaxial region, whose resistivity and thickness increase with voltage (Table 2). Consequently, improving the on–resistance of the cells on the surface of the chip has a diminishing effect as voltage increases. Sixty volt devices will serve the automotive and industrial markets, while 30 V devices will be used in the computer and portable tools industries.

P–Channels

P–channel devices benefit from high cell densities, too. The performance of P–channel MOSFETs have always trailed that of their N–channel counterparts since they inherently have about three times the on–resistance. But cutting on–resistance area product by a factor of two broadens the range of applications serviceable by P–channels too. Of special interest are 20 V devices in the SO–8 package, where a single logic level P–channel has an on–resistance rating of 70 mΩ, and a dual would be rated at 140 mΩ each. Current plans are to introduce a 30 V P–channel in the DPAK, which would have an on–resistance rating in the range of 100 mΩ. The new P–channels hold great promise for use in laptop computers and in computer peripherals. Their gate drives are especially efficient since they do not require the charge pump that the N–channel devices need.

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