



EMIF03-SIM01F2

3-line IPAD™, EMI filter including ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space occupation:
1.42 mm x 1.42 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards

- IEC 61000-4-2 level 4 on input pins
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL SRD 883E - Method 3015-6 Class 3

Applications

EMI filtering and ESD protection for:

- SIM interface (subscriber identity module)
- UIM interface (universal identity module)

Description

The EMIF03-SIM01F2 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The EMIF03 Flip Chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

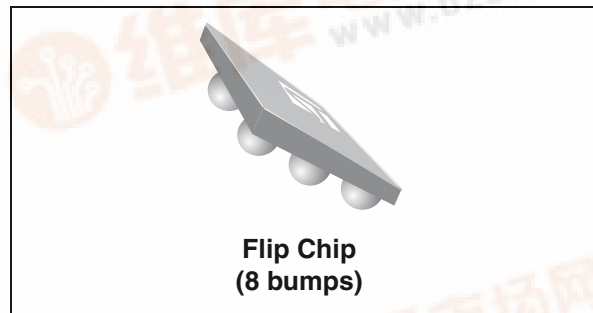


Figure 1. Pin layout (bump side)

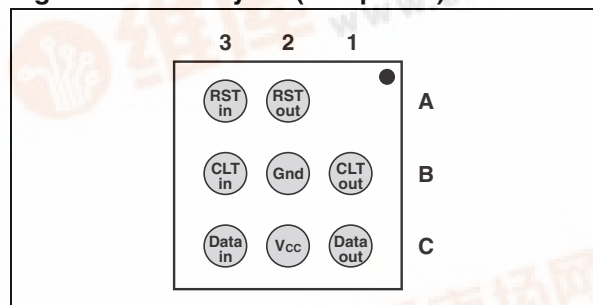
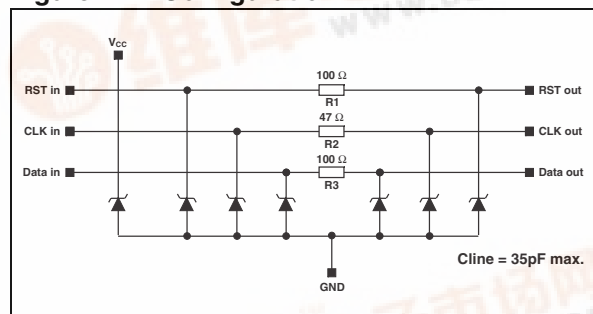


Figure 2. Configuration



TM: IPAD is a trademark of STMicroelectronics.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

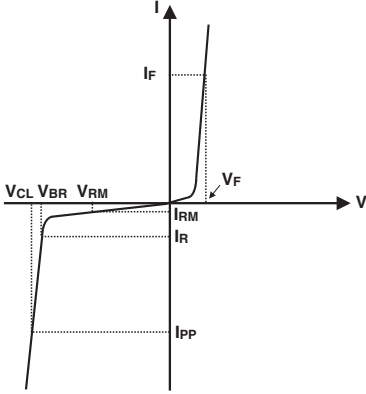
Symbol	Parameters				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
V_{CL}	Clamping voltage				
R_d	Dynamic impedance				
I_{PP}	Peak pulse current				
$R_{I/O}$	Series resistance between input and output				
C_{line}	Input capacitance per line				
Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{ mA}$	6			V
I_{RM}	$V_{RM} = 3\text{ V per line}$			1	μA
R_d			1.5		Ω
R_1		95	100	105	Ω
R_2		44.65	47	49.35	Ω
R_3		95	100	105	Ω
C_{line}	@ 0 V			35	pF

Figure 3. S21 (dB) attenuation measurement Figure 4. Analog crosstalk measurement

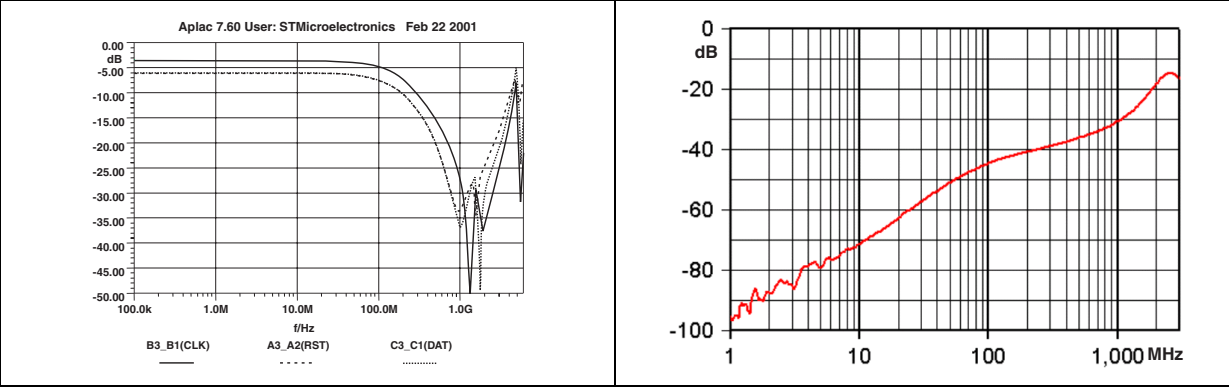


Figure 5. Digital crosstalk measurement Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (Vin) and on one output (Vout)

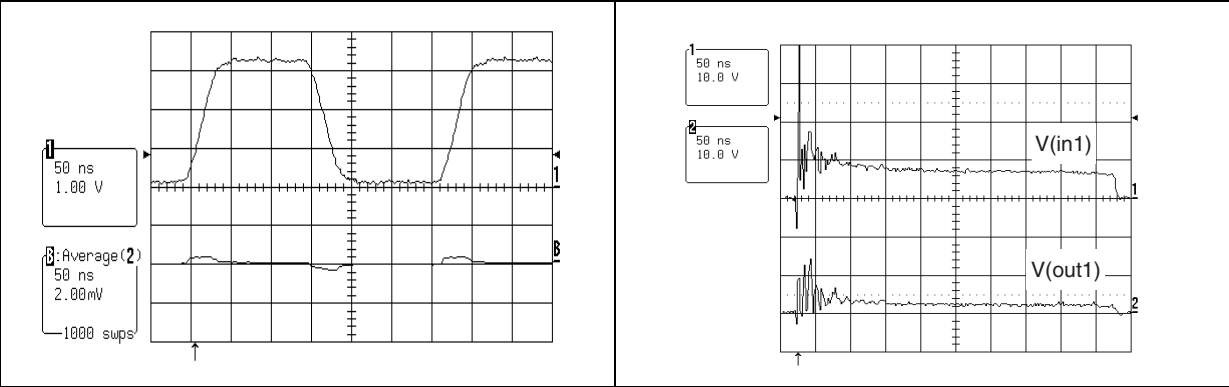
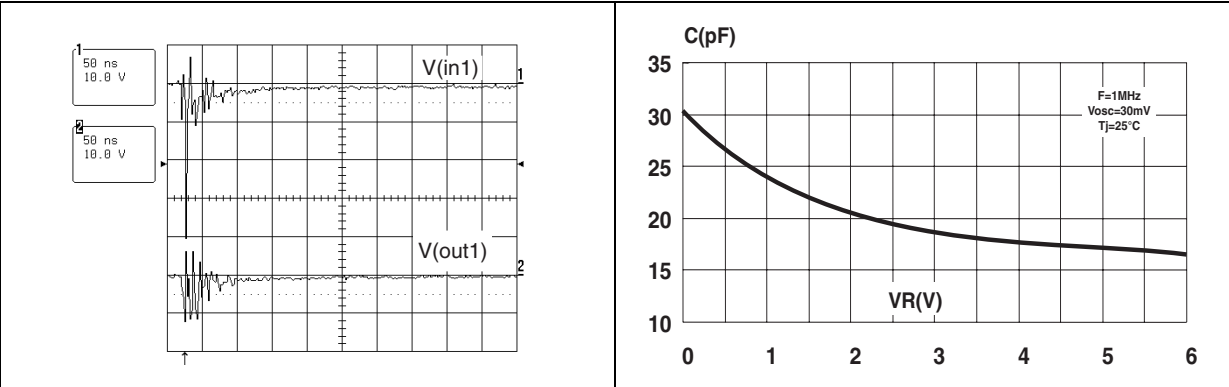
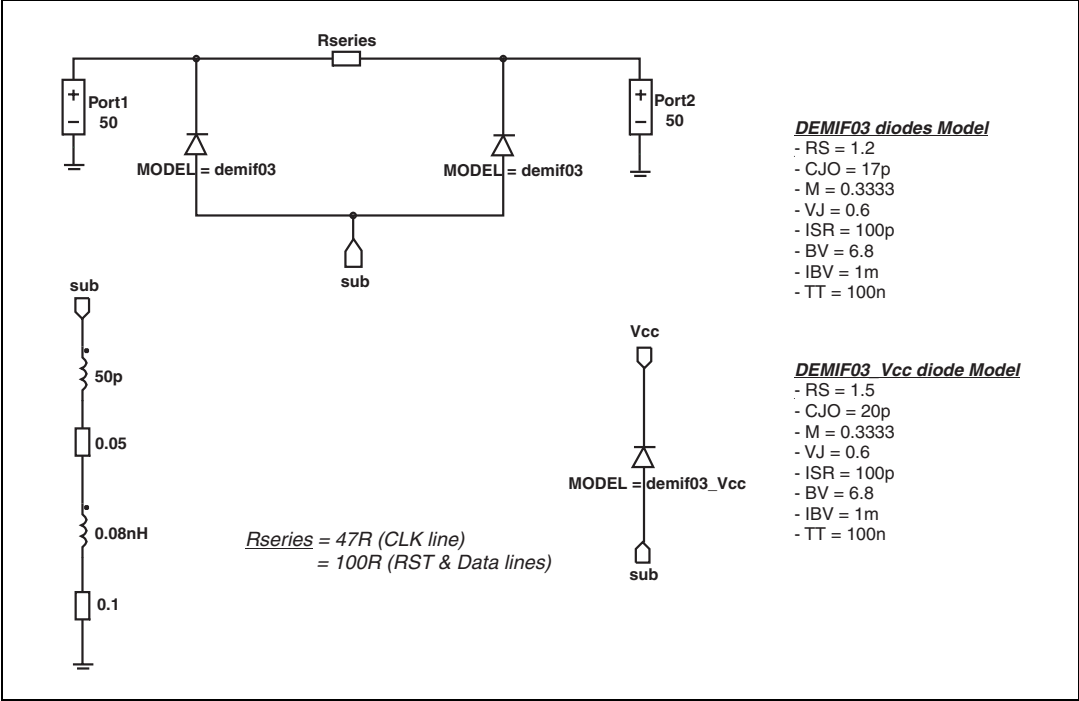


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (Vin) and on one output (Vout) Figure 8. Line capacitance versus applied voltage (typical)



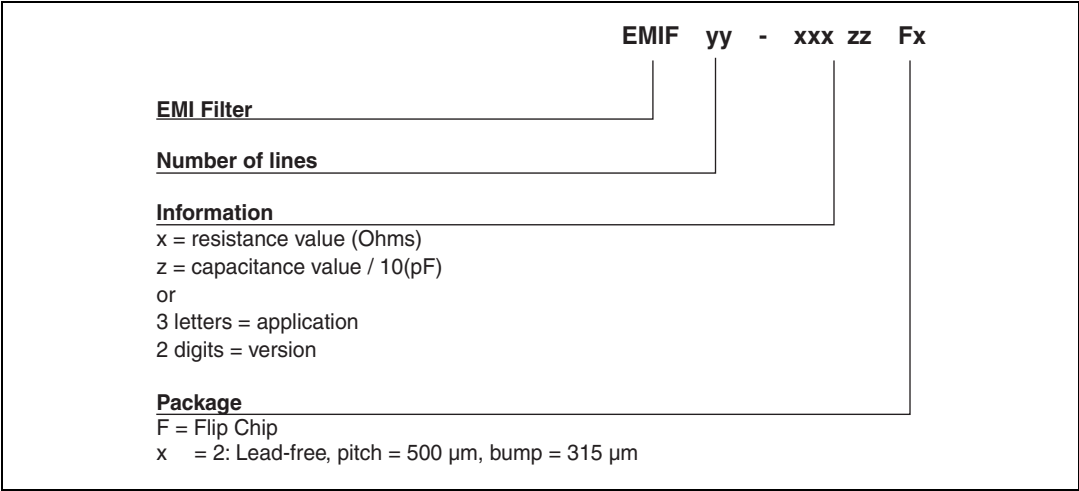
2 Application information

Figure 9. Aplac model



3 Ordering information scheme

Figure 10. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 11. Package dimensions

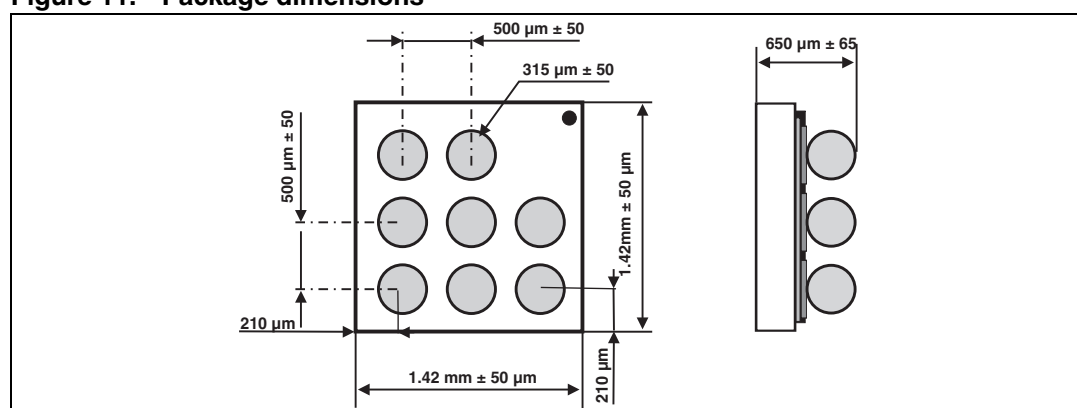


Figure 12. Footprint

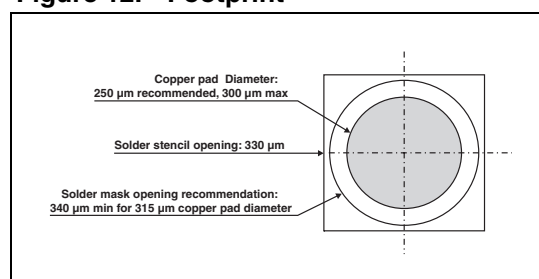


Figure 13. Marking

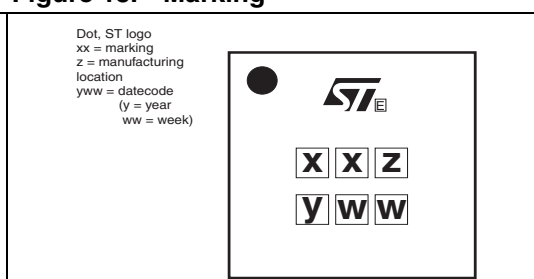
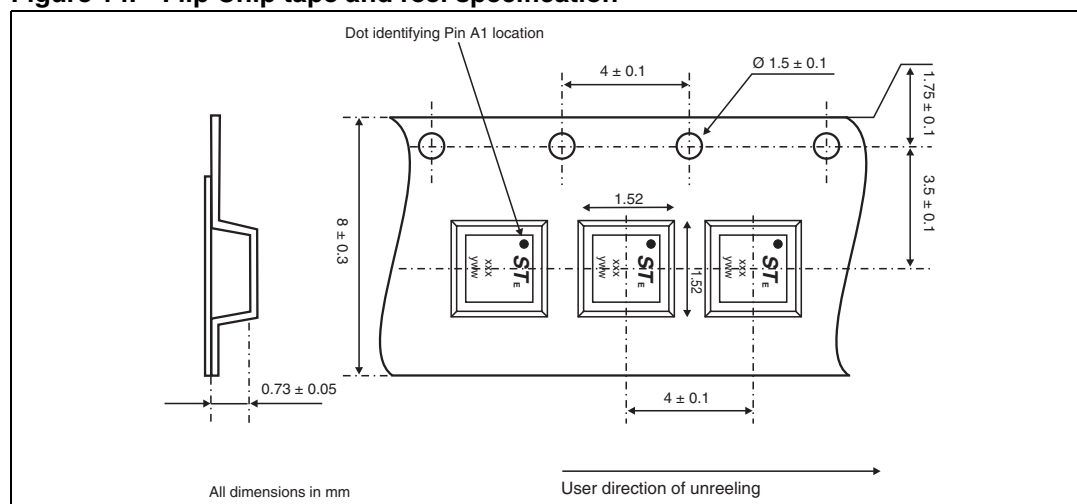


Figure 14. Flip Chip tape and reel specification



5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM01F2	FC	Flip Chip	2.9 mg	5000	Tape and reel 7"

Note:

More information is available in the application notes:

AN1235: "Flip Chip: Package description and recommendations for use"

AN1751: "EMI filters: Recommendations and measurements"

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
08-Oct-2004	1	Initial release.
13-Dec-2004	2	Table 3 . on page 6: Flip Chip weight corrected from 3.3 mg to 2.9 mg.
28-Apr-2008	3	Updated ECOPACK statement. Updated Figure 10 , Figure 11 and Figure 14 . Reformatted to current standards.

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