

Transistor

2.5V Drive Nch+Nch MOS FET

EM6K1

● Structure

Silicon N-channel MOS FET

● Features

- 1) Two 2SK3019 transistors in a single EMT package.
- 2) The MOS FET elements are independent, eliminating mutual interference.
- 3) Mounting cost and area can be cut in half.
- 4) Low on-resistance.
- 5) Low voltage drive (2.5V) makes this device ideal for portable equipment.

● Applications

Interfacing, switching (30V, 100mA)

●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6K1		○

- **Absolute maximum ratings (Ta=25°C)**

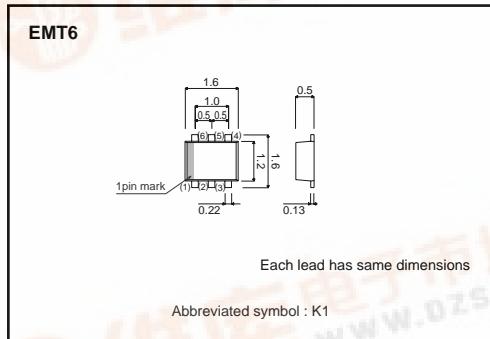
<It is the same ratings for Tr1 and Tr2. >

Parameter	Symbol	Limits	Unit
Drain-source voltage	V _{DSS}	30	V
Gate-source voltage	V _{GSS}	±20	V
Drain current	Continuous	I _D	mA
	Pulsed	I _{DP} ^{*1}	mA
Total power dissipation	P _D ^{*2}	150	mW / TOTAL
		120	mW / ELEMENT
Channel temperature	T _{CH}	150	°C
Storage temperature	T _{STG}	-55 to +150	°C

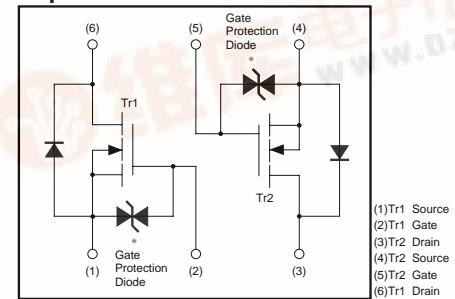
*1 $P_w \leq 10\mu\text{s}$, Duty cycle $\leq 1\%$

*2 With each pin mounted on the recommended lands.

● **External dimensions (Unit : mm)**



● Equivalent circuit



- * A protection diode has been built in between the gate and the source to protect against static electricity when the product is in use. Use the protection circuit when rated voltages are exceeded.

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●Electrical characteristics ($T_a=25^\circ\text{C}$)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 1	μA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D=10\mu\text{A}$, $V_{GS}=0\text{V}$
Zero gate voltage drain current	I_{DSS}	—	—	1.0	μA	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$
Gate threshold voltage	$V_{GS(\text{th})}$	0.8	—	1.5	V	$V_{DS}=3\text{V}$, $I_D=100\mu\text{A}$
Static drain-source on-state resistance	$R_{DS(\text{on})}$	—	5	8	Ω	$I_D=10\text{mA}$, $V_{GS}=4\text{V}$
	$R_{DS(\text{on})}$	—	7	13	Ω	$I_D=1\text{mA}$, $V_{GS}=2.5\text{V}$
Forward transfer admittance	$ Y_{fs} $	20	—	—	mS	$V_{DS}=3\text{V}$, $I_D=10\text{mA}$
Input capacitance	C_{iss}	—	13	—	pF	$V_{DS}=5\text{V}$
Output capacitance	C_{oss}	—	9	—	pF	$V_{GS}=0\text{V}$
Reverse transfer capacitance	C_{rss}	—	4	—	pF	$f=1\text{MHz}$
Turn-on delay time	$t_{d(\text{on})}$	—	15	—	ns	$I_D=10\text{mA}$, $V_{DD}=5\text{V}$
Rise time	t_r	—	35	—	ns	$V_{GS}=5\text{V}$
Turn-off delay time	$t_{d(\text{off})}$	—	80	—	ns	$R_L=500\Omega$
Fall time	t_f	—	80	—	ns	$R_G=10\Omega$

●Electrical characteristic curves

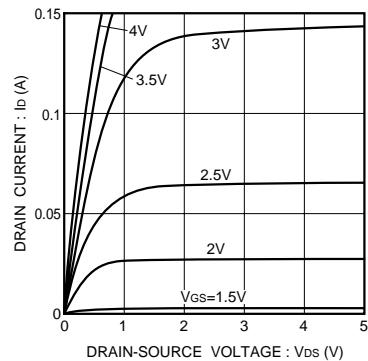


Fig.1 Typical Output Characteristics

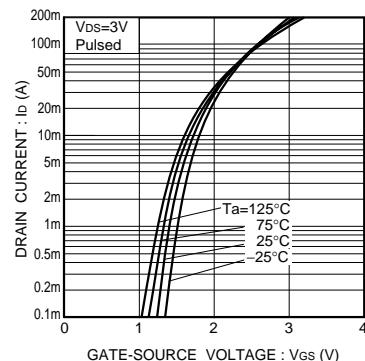


Fig.2 Typical Transfer Characteristics

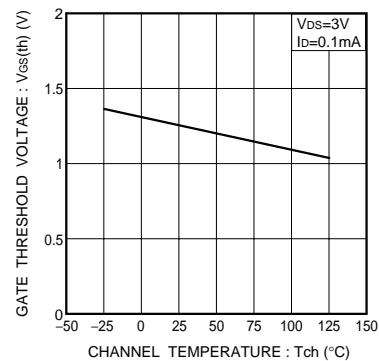


Fig.3 Gate Threshold Voltage vs. Channel Temperature

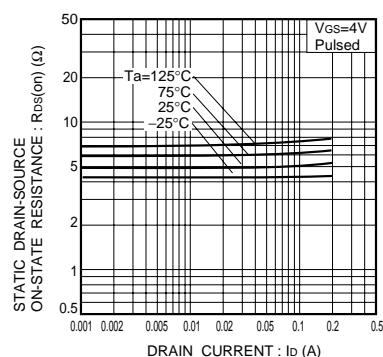


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

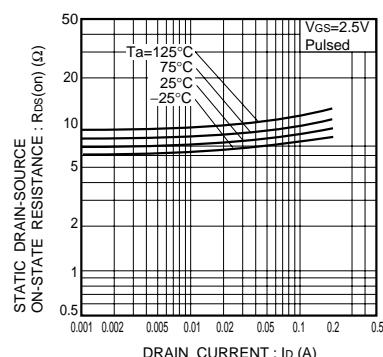


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

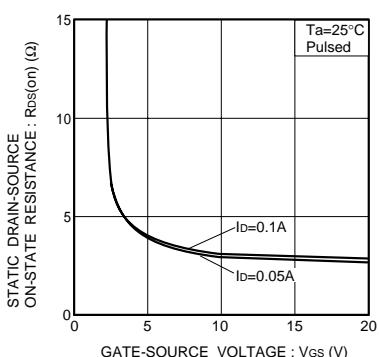


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

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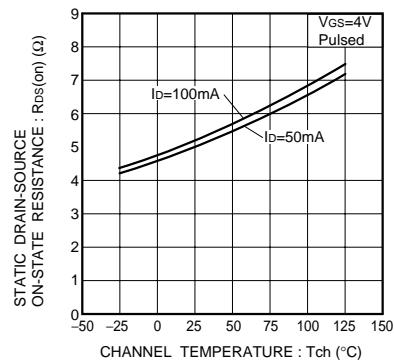


Fig.7 Static Drain-Source On-State Resistance vs. Channel Temperature

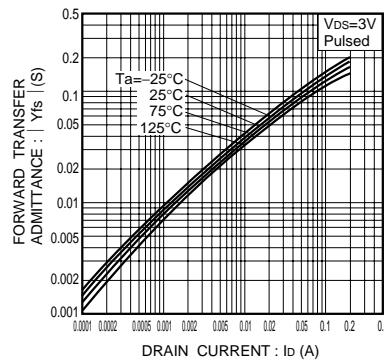


Fig.8 Forward Transfer Admittance vs. Drain Current

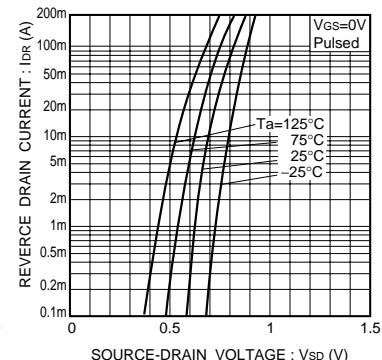


Fig.9 Reverse Drain Current vs. Source-Drain Voltage (I)

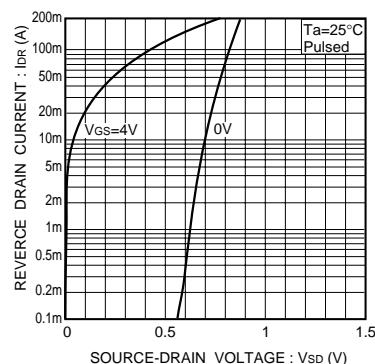


Fig.10 Reverse Drain Current vs. Source-Drain Voltage (II)

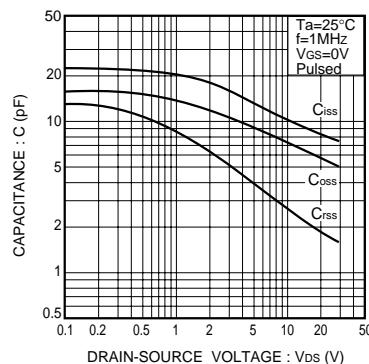


Fig.11 Typical Capacitance vs. Drain-Source Voltage

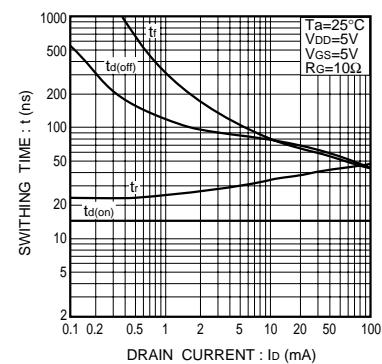


Fig.12 Switching Characteristics

●Switching characteristics measurement circuits

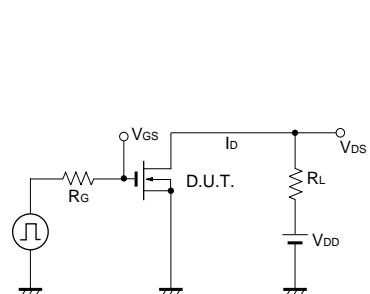


Fig.13 Switching Time Test Circuit

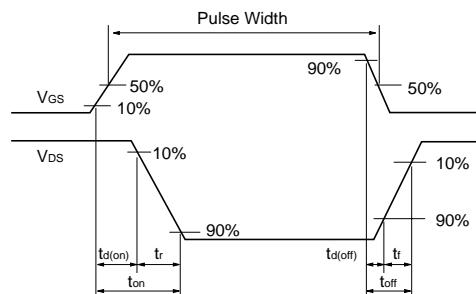


Fig.14 Switching Time Waveforms

Appendix

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