

EM65101

128COM/160SEG
16 Gray Scale Level
LCD Driver

Product Specification

Doc. VERSION 0.4


ELAN MICROELECTRONICS CORP.

August 2005

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Specification Revision History

| Doc. Version | Revision Description | Date |
|--------------|--|-------------------|
| 0.1 | Initial version | January 10, 2005 |
| 0.2 | <ol style="list-style-type: none"> 1. Add pin related information 2. Modify reset time 3. Modify write timing 4. Add V0 specification 5. Modify application circuit on CK and VBA pins 6. Remove Nline reverse figure | February 22, 2005 |
| 0.3 | <ol style="list-style-type: none"> 1. Modify Extending command 2. Modify read EEPROM sequence | March 08, 2005 |
| 0.4 | <ol style="list-style-type: none"> 1. Modify Nline settingvalue 2. Modify the EEPROM programming voltage 3. Modify AXI, AIM function description 4. Remove the CF and VTC description 5. Modify the write timing on 68-family and SPI mode 6. The V4 voltage limit when setting bias=1/4 and 1/5 7. Modify the read address on RF register 8. Modify the DC spec with dynamic current and Fosc 9. Modify the contrast value setting 10. Modify the SC description 11. Add tray information 12. Modify application circuit and description on VREF and VBA pins | August 15, 2005 |



1 General Description

The EM65101 is an LCD controller for 16-level gray scale graphic dot-matrix liquid crystal display system. It is a (160 x 128) for segment and common driver circuit. It has a built-in display RAM, a power supply circuit for LCD driver. It also supports EEPROM function for programming information to tune the V_{LCD} offset voltage to get the best contrast which helps in compacting system design. Its "partial display"¹ function realizes results in low power consumption.

2 Feature

- 16-level gray scale display with the PWM method
- LCD output circuit:
160 segment / 128 common outputs
- Display RAM capacity: $128 \times 160 \times 4 = 81920$ bits
- Built-in display RAM and power supply circuit:
Booster: 2 to 6 times
On-chip electronic contrast function (65 steps)
Voltage follower (LCD bias: 1/4 to 1/13)
- Partial display function
- Microprocessor interface:
8-bit parallel bi-direction interface with the 6800-series or 8080-series
4-line Serial Peripheral Interface (4-line SPI)
3-line Serial Peripheral Interface (3-line SPI)
- Operating voltage range:
Logical power supply voltage: 2.2 to 3.3 V
Analog power supply voltage: 2.4 to 3.3 V
- Screen scrolling function
- EEPROM function to change the tuning LCD operating voltage V_{op}
- Write cycle time: 200 ns
- Package:

| Part Number | Package |
|-------------|---|
| EM65101AH* | Bare chip (aluminum pad without bump, see Figure 4-1 below) |
| EM65101AGH* | Gold bumped chip |
| EM65101AF* | COF chip |
| EM65101AT* | TAB (TCP) chip |

* EM65101=ELAN base P/N; A=package type version; H/GH/FT=packaging category

¹ A function that utilizes only part of the screen, thus reducing power consumption.

3 Applications

- Mobile phone
- Small PDA

4 Pin Configurations

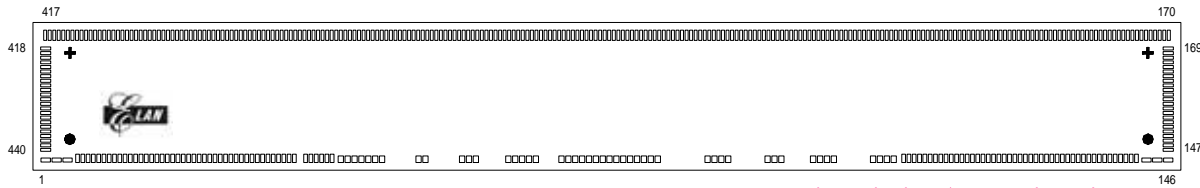


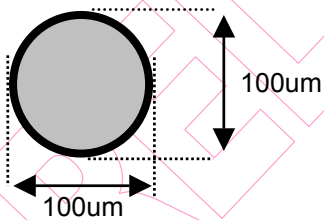
Figure 4-1 EM65101AH Pin Configuration (Sample)

NOTE
The ELAN logo is at the left side end and Pin1 is at the bottom-left corner.

4.1 Alignment Key

| Mark | Coordinates (X,Y) | Mark | Coordinates (X,Y) |
|--------|-------------------|---------|-------------------|
| U-Left | -5019.95, 273.5 | U-Right | 5020.75, 273.5 |
| D-Left | -5019.95, -321.65 | D-Right | 5020.75, -321.65 |

D-Left and D-Right:



U-Left and U-Right:

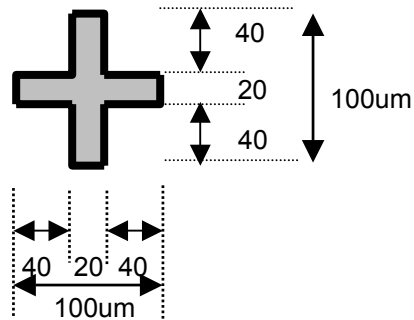


Figure 4-2 Pin Alignment Key



4.2 Pin Dimensions

| Item | Pad No. | Bump Size | | Unit |
|------------------------------------|--------------------------|-----------|------|------|
| | | X | Y | |
| Chip size | - | 10850 | 1380 | μm |
| Bump Size | 1 ~ 3 ; 144 ~ 146 | 88 | 38 | |
| | 4 ~ 51 ; 99 ~ 143 | 35 | 78 | |
| | 52 ~ 98 | 50 | 61 | |
| | 147 ~ 169 ; 418 ~ 440 | 96 | 28 | |
| | 170 ~ 417 | 28 | 96 | |
| Pad Pitch | 1 ~ 3 ; 144 ~ 146 | 103 | | |
| | 4 ~ 51 ; 99 ~ 143 | 50 | | |
| | 52 ~ 98 | 65 | | |
| | 147 ~ 169 ; 418 ~ 440 | 43 | | |
| | 170 ~ 417 | 43 | | |
| | Min pitch | 43 | | |
| Die thickness (excluding bumps) | 20 ± 1 mil (500 ± 25 um) | | | |
| Bump Height | 17 ± 3 um | | | |
| Minimum Bump Gap | 15 um | | | |
| Coordinate Origin | Chip center | | | |

4.3 Recommended COG ITO Traces Resistor

| Interface | ITO Traces Resistances |
|---|------------------------|
| V0~V4 CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3- CAP4+, CAP5+, VOUT, V2X VDD, VEE, VSS | Max=50Ω |
| WRB, RDB, CSB, ..., D0~D7 | Max=3KΩ |
| RESB | Max=5~10KΩ |



4.3 PAD Coordinates Table

| Pin No. | Pad Name | Coordinate (X,Y) | Pin No. | Pad Name | Coordinate (X,Y) |
|---------|----------|------------------|---------|----------|------------------|
| 1 | DUMMY | -5305.0, -595.0 | 51 | VSS | -2598.2, -579.0 |
| 2 | DUMMY | -5202.0, -595.0 | 52 | VOUT | -2515.6, -587.5 |
| 3 | DUMMY | -5099.0, -595.0 | 53 | VOUT | -2450.6, -587.5 |
| 4 | DUMMY | -5004.6, -579.0 | 54 | VOUT | -2385.6, -587.5 |
| 5 | VSS | -4954.6, -579.0 | 55 | VOUT | -2320.6, -587.5 |
| 6 | TEST | -4904.6, -579.0 | 56 | VOUT | -2255.6, -587.5 |
| 7 | P/S | -4854.6, -579.0 | 57 | VOUT | -2190.6, -587.5 |
| 8 | VDD | -4804.6, -579.0 | 58 | CAP5+ | -2125.6, -587.5 |
| 9 | M86 | -4754.6, -579.0 | 59 | CAP5+ | -1780.1, -587.5 |
| 10 | VSS | -4704.6, -579.0 | 60 | CAP3+ | -1715.1, -587.5 |
| 11 | CSB | -4654.6, -579.0 | 61 | CAP3+ | -1369.3, -587.5 |
| 12 | CSB | -4604.6, -579.0 | 62 | CAP3- | -1304.3, -587.5 |
| 13 | RESB | -4554.6, -579.0 | 63 | CAP3- | -1239.3, -587.5 |
| 14 | RS | -4504.6, -579.0 | 64 | CAP3- | -932.3, -587.5 |
| 15 | RS | -4454.6, -579.0 | 65 | CAP3- | -867.3, -587.5 |
| 16 | CK | -4404.6, -579.0 | 66 | CAP2- | -802.3, -587.5 |
| 17 | CK | -4354.6, -579.0 | 67 | CAP2- | -737.3, -587.5 |
| 18 | WRB | -4304.6, -579.0 | 68 | CAP2- | -672.3, -587.5 |
| 19 | WRB | -4254.6, -579.0 | 69 | CAP2- | -430.3, -587.5 |
| 20 | RDB | -4204.6, -579.0 | 70 | CAP2- | -365.3, -587.5 |
| 21 | RDB | -4154.6, -579.0 | 71 | CAP2+ | -300.3, -587.5 |
| 22 | D0 | -4104.6, -579.0 | 72 | CAP2+ | -235.3, -587.5 |
| 23 | D0 | -4054.6, -579.0 | 73 | CAP2+ | -170.3, -587.5 |
| 24 | D1 | -4004.6, -579.0 | 74 | CAP2+ | -105.3, -587.5 |
| 25 | D1 | -3954.6, -579.0 | 75 | CAP2+ | -40.3, -587.5 |
| 26 | D2 | -3904.6, -579.0 | 76 | CAP2+ | 24.7, -587.5 |
| 27 | D2 | -3854.6, -579.0 | 77 | CAP4+ | 89.7, -587.5 |
| 28 | D3 | -3804.6, -579.0 | 78 | CAP4+ | 154.7, -587.5 |
| 29 | D3 | -3754.6, -579.0 | 79 | CAP4+ | 219.7, -587.5 |
| 30 | D4 | -3704.6, -579.0 | 80 | CAP4+ | 284.7, -587.5 |
| 31 | D4 | -3654.6, -579.0 | 81 | CAP4+ | 349.7, -587.5 |
| 32 | D5 | -3604.6, -579.0 | 82 | CAP4+ | 414.7, -587.5 |
| 33 | D5 | -3554.6, -579.0 | 83 | VEE | 479.7, -587.5 |
| 34 | D6 | -3504.6, -579.0 | 84 | VEE | 951.7, -587.5 |
| 35 | D6 | -3454.6, -579.0 | 85 | VEE | 1016.7, -587.5 |
| 36 | D7 | -3404.6, -579.0 | 86 | CAP1- | 1081.7, -587.5 |
| 37 | D7 | -3354.6, -579.0 | 87 | CAP1- | 1146.7, -587.5 |
| 38 | VSS | -3304.6, -579.0 | 88 | CAP1- | 1518.7, -587.5 |
| 39 | CKS | -3254.6, -579.0 | 89 | CAP1+ | 1583.7, -587.5 |
| 40 | VDD | -3204.6, -579.0 | 90 | CAP1+ | 1648.7, -587.5 |
| 41 | VDD | -3154.6, -579.0 | 91 | CAP1+ | 1948.7, -587.5 |
| 42 | VDD | -3104.6, -579.0 | 92 | CAP1+ | 2013.7, -587.5 |
| 43 | VDD | -3054.6, -579.0 | 93 | V2X | 2078.7, -587.5 |
| 44 | VBA | -3004.6, -579.0 | 94 | V2X | 2143.7, -587.5 |
| 45 | VREF | -2954.6, -579.0 | 95 | V2X | 2515.7, -587.5 |
| 46 | VPP | -2848.2, -579.0 | 96 | VSS | 2580.7, -587.5 |
| 47 | VPP | -2798.2, -579.0 | 97 | VSS | 2645.7, -587.5 |
| 48 | VPP | -2748.2, -579.0 | 98 | VSS | 2710.7, -587.5 |
| 49 | VSS | -2698.2, -579.0 | 99 | VSS | 2804.6, -579.0 |
| 50 | VSS | -2648.2, -579.0 | 100 | VSS | 2854.6, -579.0 |



| Pin No. | Pad Name | Coordinate (X,Y) | Pin No. | Pad Name | Coordinate (X,Y) |
|---------|----------|------------------|---------|----------|------------------|
| 101 | VSS | 2904.6, -579.0 | 151 | COM60 | 5305.0, -328.0 |
| 102 | VSS | 2954.6, -579.0 | 152 | COM59 | 5305.0, -285.0 |
| 103 | VSS | 3004.6, -579.0 | 153 | COM58 | 5305.0, -242.0 |
| 104 | VSS | 3054.6, -579.0 | 154 | COM57 | 5305.0, -199.0 |
| 105 | V4 | 3104.6, -579.0 | 155 | COM56 | 5305.0, -156.0 |
| 106 | V4 | 3154.6, -579.0 | 156 | COM55 | 5305.0, -113.0 |
| 107 | V4 | 3204.6, -579.0 | 157 | COM54 | 5305.0, -70.0 |
| 108 | V4 | 3254.6, -579.0 | 158 | COM53 | 5305.0, -27.0 |
| 109 | V4 | 3304.6, -579.0 | 159 | COM52 | 5305.0, 16.0 |
| 110 | V4 | 3354.6, -579.0 | 160 | COM51 | 5305.0, 59.0 |
| 111 | V4 | 3404.6, -579.0 | 161 | COM50 | 5305.0, 102.0 |
| 112 | V3 | 3454.6, -579.0 | 162 | COM49 | 5305.0, 145.0 |
| 113 | V3 | 3504.6, -579.0 | 163 | COM48 | 5305.0, 188.0 |
| 114 | V3 | 3554.6, -579.0 | 164 | COM47 | 5305.0, 231.0 |
| 115 | V3 | 3604.6, -579.0 | 165 | COM46 | 5305.0, 274.0 |
| 116 | V3 | 3654.6, -579.0 | 166 | COM45 | 5305.0, 317.0 |
| 117 | V3 | 3704.6, -579.0 | 167 | COM44 | 5305.0, 360.0 |
| 118 | V3 | 3754.6, -579.0 | 168 | COM43 | 5305.0, 403.0 |
| 119 | V2 | 3804.6, -579.0 | 169 | DUMMY | 5305.0, 446.0 |
| 120 | V2 | 3854.6, -579.0 | 170 | DUMMY | 5310.5, 570.0 |
| 121 | V2 | 3904.6, -579.0 | 171 | COM42 | 5267.5, 570.0 |
| 122 | V2 | 3954.6, -579.0 | 172 | COM41 | 5224.5, 570.0 |
| 123 | V2 | 4004.6, -579.0 | 173 | COM40 | 5181.5, 570.0 |
| 124 | V2 | 4054.6, -579.0 | 174 | COM39 | 5138.5, 570.0 |
| 125 | V2 | 4104.6, -579.0 | 175 | COM38 | 5095.5, 570.0 |
| 126 | V1 | 4154.6, -579.0 | 176 | COM37 | 5052.5, 570.0 |
| 127 | V1 | 4204.6, -579.0 | 177 | COM36 | 5009.5, 570.0 |
| 128 | V1 | 4254.6, -579.0 | 178 | COM35 | 4966.5, 570.0 |
| 129 | V1 | 4304.6, -579.0 | 179 | COM34 | 4923.5, 570.0 |
| 130 | V1 | 4354.6, -579.0 | 180 | COM33 | 4880.5, 570.0 |
| 131 | V1 | 4404.6, -579.0 | 181 | COM32 | 4837.5, 570.0 |
| 132 | V1 | 4454.6, -579.0 | 182 | COM31 | 4794.5, 570.0 |
| 133 | V1 | 4504.6, -579.0 | 183 | COM30 | 4751.5, 570.0 |
| 134 | V0 | 4554.6, -579.0 | 184 | COM29 | 4708.5, 570.0 |
| 135 | V0 | 4604.6, -579.0 | 185 | COM28 | 4665.5, 570.0 |
| 136 | V0 | 4654.6, -579.0 | 186 | COM27 | 4622.5, 570.0 |
| 137 | V0 | 4704.6, -579.0 | 187 | COM26 | 4579.5, 570.0 |
| 138 | V0 | 4754.6, -579.0 | 188 | COM25 | 4536.5, 570.0 |
| 139 | V0 | 4804.6, -579.0 | 189 | COM24 | 4493.5, 570.0 |
| 140 | V0 | 4854.6, -579.0 | 190 | COM23 | 4450.5, 570.0 |
| 141 | V0 | 4904.6, -579.0 | 191 | COM22 | 4407.5, 570.0 |
| 142 | V0 | 4954.6, -579.0 | 192 | COM21 | 4364.5, 570.0 |
| 143 | DUMMY | 5004.6, -579.0 | 193 | COM20 | 4321.5, 570.0 |
| 144 | DUMMY | 5099.0, -595.0 | 194 | COM19 | 4278.5, 570.0 |
| 145 | DUMMY | 5202.0, -595.0 | 195 | COM18 | 4235.5, 570.0 |
| 146 | DUMMY | 5305.0, -595.0 | 196 | COM17 | 4192.5, 570.0 |
| 147 | DUMMY | 5305.0, -500.0 | 197 | COM16 | 4149.5, 570.0 |
| 148 | COM63 | 5305.0, -457.0 | 198 | COM15 | 4106.5, 570.0 |
| 149 | COM62 | 5305.0, -414.0 | 199 | COM14 | 4063.5, 570.0 |
| 150 | COM61 | 5305.0, -371.0 | 200 | COM13 | 4020.5, 570.0 |



| Pin No. | Pad Name | Coordinate (X,Y) | Pin No. | Pad Name | Coordinate (X,Y) |
|---------|----------|------------------|---------|----------|------------------|
| 201 | COM12 | 3977.5, 570.0 | 251 | SEG37 | 1827.5, 570.0 |
| 202 | COM11 | 3934.5, 570.0 | 252 | SEG38 | 1784.5, 570.0 |
| 203 | COM10 | 3891.5, 570.0 | 253 | SEG39 | 1741.5, 570.0 |
| 204 | COM9 | 3848.5, 570.0 | 254 | SEG40 | 1698.5, 570.0 |
| 205 | COM8 | 3805.5, 570.0 | 255 | SEG41 | 1655.5, 570.0 |
| 206 | COM7 | 3762.5, 570.0 | 256 | SEG42 | 1612.5, 570.0 |
| 207 | COM6 | 3719.5, 570.0 | 257 | SEG43 | 1569.5, 570.0 |
| 208 | COM5 | 3676.5, 570.0 | 258 | SEG44 | 1526.5, 570.0 |
| 209 | COM4 | 3633.5, 570.0 | 259 | SEG45 | 1483.5, 570.0 |
| 210 | COM3 | 3590.5, 570.0 | 260 | SEG46 | 1440.5, 570.0 |
| 211 | COM2 | 3547.5, 570.0 | 261 | SEG47 | 1397.5, 570.0 |
| 212 | COM1 | 3504.5, 570.0 | 262 | SEG48 | 1354.5, 570.0 |
| 213 | COM0 | 3461.5, 570.0 | 263 | SEG49 | 1311.5, 570.0 |
| 214 | SEG0 | 3418.5, 570.0 | 264 | SEG50 | 1268.5, 570.0 |
| 215 | SEG1 | 3375.5, 570.0 | 265 | SEG51 | 1225.5, 570.0 |
| 216 | SEG2 | 3332.5, 570.0 | 266 | SEG52 | 1182.5, 570.0 |
| 217 | SEG3 | 3289.5, 570.0 | 267 | SEG53 | 1139.5, 570.0 |
| 218 | SEG4 | 3246.5, 570.0 | 268 | SEG54 | 1096.5, 570.0 |
| 219 | SEG5 | 3203.5, 570.0 | 269 | SEG55 | 1053.5, 570.0 |
| 220 | SEG6 | 3160.5, 570.0 | 270 | SEG56 | 1010.5, 570.0 |
| 221 | SEG7 | 3117.5, 570.0 | 271 | SEG57 | 967.5, 570.0 |
| 222 | SEG8 | 3074.5, 570.0 | 272 | SEG58 | 924.5, 570.0 |
| 223 | SEG9 | 3031.5, 570.0 | 273 | SEG59 | 881.5, 570.0 |
| 224 | SEG10 | 2988.5, 570.0 | 274 | SEG60 | 838.5, 570.0 |
| 225 | SEG11 | 2945.5, 570.0 | 275 | SEG61 | 795.5, 570.0 |
| 226 | SEG12 | 2902.5, 570.0 | 276 | SEG62 | 752.5, 570.0 |
| 227 | SEG13 | 2859.5, 570.0 | 277 | SEG63 | 709.5, 570.0 |
| 228 | SEG14 | 2816.5, 570.0 | 278 | SEG64 | 666.5, 570.0 |
| 229 | SEG15 | 2773.5, 570.0 | 279 | SEG65 | 623.5, 570.0 |
| 230 | SEG16 | 2730.5, 570.0 | 280 | SEG66 | 580.5, 570.0 |
| 231 | SEG17 | 2687.5, 570.0 | 281 | SEG67 | 537.5, 570.0 |
| 232 | SEG18 | 2644.5, 570.0 | 282 | SEG68 | 494.5, 570.0 |
| 233 | SEG19 | 2601.5, 570.0 | 283 | SEG69 | 451.5, 570.0 |
| 234 | SEG20 | 2558.5, 570.0 | 284 | SEG70 | 408.5, 570.0 |
| 235 | SEG21 | 2515.5, 570.0 | 285 | SEG71 | 365.5, 570.0 |
| 236 | SEG22 | 2472.5, 570.0 | 286 | SEG72 | 322.5, 570.0 |
| 237 | SEG23 | 2429.5, 570.0 | 287 | SEG73 | 279.5, 570.0 |
| 238 | SEG24 | 2386.5, 570.0 | 288 | SEG74 | 236.5, 570.0 |
| 239 | SEG25 | 2343.5, 570.0 | 289 | SEG75 | 193.5, 570.0 |
| 240 | SEG26 | 2300.5, 570.0 | 290 | SEG76 | 150.5, 570.0 |
| 241 | SEG27 | 2257.5, 570.0 | 291 | SEG77 | 107.5, 570.0 |
| 242 | SEG28 | 2214.5, 570.0 | 292 | SEG78 | 64.5, 570.0 |
| 243 | SEG29 | 2171.5, 570.0 | 293 | SEG79 | 21.5, 570.0 |
| 244 | SEG30 | 2128.5, 570.0 | 294 | SEG80 | -21.5, 570.0 |
| 245 | SEG31 | 2085.5, 570.0 | 295 | SEG81 | -64.5, 570.0 |
| 246 | SEG32 | 2042.5, 570.0 | 296 | SEG82 | -107.5, 570.0 |
| 247 | SEG33 | 1999.5, 570.0 | 297 | SEG83 | -150.5, 570.0 |
| 248 | SEG34 | 1956.5, 570.0 | 298 | SEG84 | -193.5, 570.0 |
| 249 | SEG35 | 1913.5, 570.0 | 299 | SEG85 | -236.5, 570.0 |
| 250 | SEG36 | 1870.5, 570.0 | 300 | SEG86 | -279.5, 570.0 |



| Pin No. | Pad Name | Coordinate (X,Y) | Pin No. | Pad Name | Coordinate (X,Y) |
|---------|----------|------------------|---------|----------|------------------|
| 301 | SEG87 | -322.5, 570.0 | 351 | SEG137 | -2472.5, 570.0 |
| 302 | SEG88 | -365.5, 570.0 | 352 | SEG138 | -2515.5, 570.0 |
| 303 | SEG89 | -408.5, 570.0 | 353 | SEG139 | -2558.5, 570.0 |
| 304 | SEG90 | -451.5, 570.0 | 354 | SEG140 | -2601.5, 570.0 |
| 305 | SEG91 | -494.5, 570.0 | 355 | SEG141 | -2644.5, 570.0 |
| 306 | SEG92 | -537.5, 570.0 | 356 | SEG142 | -2687.5, 570.0 |
| 307 | SEG93 | -580.5, 570.0 | 357 | SEG143 | -2730.5, 570.0 |
| 308 | SEG94 | -623.5, 570.0 | 358 | SEG144 | -2773.5, 570.0 |
| 309 | SEG95 | -666.5, 570.0 | 359 | SEG145 | -2816.5, 570.0 |
| 310 | SEG96 | -709.5, 570.0 | 360 | SEG146 | -2859.5, 570.0 |
| 311 | SEG97 | -752.5, 570.0 | 361 | SEG147 | -2902.5, 570.0 |
| 312 | SEG98 | -795.5, 570.0 | 362 | SEG148 | -2945.5, 570.0 |
| 313 | SEG99 | -838.5, 570.0 | 363 | SEG149 | -2988.5, 570.0 |
| 314 | SEG100 | -881.5, 570.0 | 364 | SEG150 | -3031.5, 570.0 |
| 315 | SEG101 | -924.5, 570.0 | 365 | SEG151 | -3074.5, 570.0 |
| 316 | SEG102 | -967.5, 570.0 | 366 | SEG152 | -3117.5, 570.0 |
| 317 | SEG103 | -1010.5, 570.0 | 367 | SEG153 | -3160.5, 570.0 |
| 318 | SEG104 | -1053.5, 570.0 | 368 | SEG154 | -3203.5, 570.0 |
| 319 | SEG105 | -1096.5, 570.0 | 369 | SEG155 | -3246.5, 570.0 |
| 320 | SEG106 | -1139.5, 570.0 | 370 | SEG156 | -3289.5, 570.0 |
| 321 | SEG107 | -1182.5, 570.0 | 371 | SEG157 | -3332.5, 570.0 |
| 322 | SEG108 | -1225.5, 570.0 | 372 | SEG158 | -3375.5, 570.0 |
| 323 | SEG109 | -1268.5, 570.0 | 373 | SEG159 | -3418.5, 570.0 |
| 324 | SEG110 | -1311.5, 570.0 | 374 | COM64 | -3461.5, 570.0 |
| 325 | SEG111 | -1354.5, 570.0 | 375 | COM65 | -3504.5, 570.0 |
| 326 | SEG112 | -1397.5, 570.0 | 376 | COM66 | -3547.5, 570.0 |
| 327 | SEG113 | -1440.5, 570.0 | 377 | COM67 | -3590.5, 570.0 |
| 328 | SEG114 | -1483.5, 570.0 | 378 | COM68 | -3633.5, 570.0 |
| 329 | SEG115 | -1526.5, 570.0 | 379 | COM69 | -3676.5, 570.0 |
| 330 | SEG116 | -1569.5, 570.0 | 380 | COM70 | -3719.5, 570.0 |
| 331 | SEG117 | -1612.5, 570.0 | 381 | COM71 | -3762.5, 570.0 |
| 332 | SEG118 | -1655.5, 570.0 | 382 | COM72 | -3805.5, 570.0 |
| 333 | SEG119 | -1698.5, 570.0 | 383 | COM73 | -3848.5, 570.0 |
| 334 | SEG120 | -1741.5, 570.0 | 384 | COM74 | -3891.5, 570.0 |
| 335 | SEG121 | -1784.5, 570.0 | 385 | COM75 | -3934.5, 570.0 |
| 336 | SEG122 | -1827.5, 570.0 | 386 | COM76 | -3977.5, 570.0 |
| 337 | SEG123 | -1870.5, 570.0 | 387 | COM77 | -4020.5, 570.0 |
| 338 | SEG124 | -1913.5, 570.0 | 388 | COM78 | -4063.5, 570.0 |
| 339 | SEG125 | -1956.5, 570.0 | 389 | COM79 | -4106.5, 570.0 |
| 340 | SEG126 | -1999.5, 570.0 | 390 | COM80 | -4149.5, 570.0 |
| 341 | SEG127 | -2042.5, 570.0 | 391 | COM81 | -4192.5, 570.0 |
| 342 | SEG128 | -2085.5, 570.0 | 392 | COM82 | -4235.5, 570.0 |
| 343 | SEG129 | -2128.5, 570.0 | 393 | COM83 | -4278.5, 570.0 |
| 344 | SEG130 | -2171.5, 570.0 | 394 | COM84 | -4321.5, 570.0 |
| 345 | SEG131 | -2214.5, 570.0 | 395 | COM85 | -4364.5, 570.0 |
| 346 | SEG132 | -2257.5, 570.0 | 396 | COM86 | -4407.5, 570.0 |
| 347 | SEG133 | -2300.5, 570.0 | 397 | COM87 | -4450.5, 570.0 |
| 348 | SEG134 | -2343.5, 570.0 | 398 | COM88 | -4493.5, 570.0 |
| 349 | SEG135 | -2386.5, 570.0 | 399 | COM89 | -4536.5, 570.0 |
| 350 | SEG136 | -2429.5, 570.0 | 400 | COM90 | -4579.5, 570.0 |

5 Functional Block Diagram

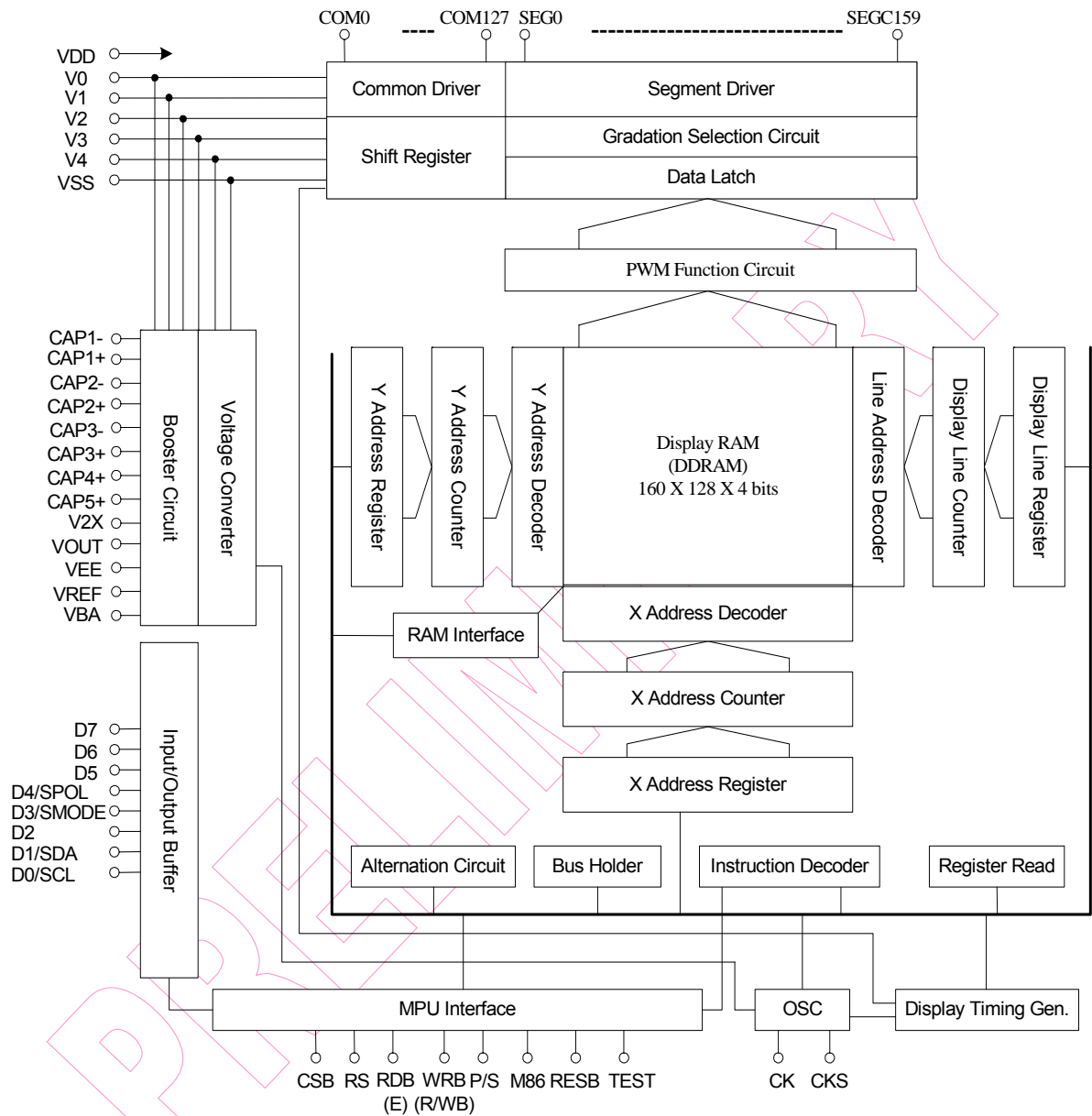


Figure 5-1 System Block Diagram

6 Pin Description

6.1 Power Supply Pins

| Symbol | I/O | Description |
|----------------------------|--------------|---|
| VDD | Power Supply | Power supply pin for logic circuit to +2.2 to 3.3V |
| VSS | Power Supply | Ground pin, connect to 0V |
| V0 V1 V2 V3 V4 | Power Supply | Bias power supply pin for LCD drive voltage When using an external power supply, convert the impedance by using the resistance-division of the LCD drive power supply or operation amplifier before adding the voltage to the pins. These voltages should have the following relationship: $VSS < V4 < V3 < V2 < V1 < V0$ When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. Then, you must connect each capacitor to VSS. |

6.2 LCD Power Supply Circuit Pins

| Symbol | I/O | Description |
|--------|--------------|---|
| CAP1+ | O | Connecting pin for the built-in booster's capacitor + side. The capacitor is connected between CAP1- and CAP1+. |
| CAP1- | O | Connecting pin for the built-in booster's capacitor - side. The capacitor is connected between CAP1- and CAP1+. |
| CAP2+ | O | Connecting pin for the built-in booster's capacitor + side. The capacitor is connected between CAP2- and CAP2+. |
| CAP2- | O | Connecting pin for the built-in booster's capacitor - side. The capacitor is connected between CAP2- and CAP2+. |
| CAP3+ | O | Connecting pin for the built-in booster's capacitor + side. The capacitor is connected between CAP3- and CAP3+. |
| CAP3- | O | Connecting pin for the built-in booster's capacitor - side. The capacitor is connected between CAP3- and CAP3+. |
| CAP4+ | O | Connecting pin for the built-in booster's capacitor + side. The capacitor is connected between CAP2- and CAP4+. |
| CAP5+ | O | Connecting pin for the built-in booster's capacitor + side. The capacitor is connected between CAP3- and CAP5+. |
| VEE | Power Supply | Voltage supply pin for the booster circuit. Usually this has the same voltage level as VDD. |
| VOUT | O | Output pin of the boosted voltage in the built-in booster. The capacitor must be connected between this pin and VSS. |
| V2X | O | Output pin which is equal to $2 \times VEE$. The capacitor must be connected between this pin and VSS. |
| VBA | O | Output pin for the regulator voltage of VBA AMP. |
| VREF | O | Output pin for temperature compensation output voltage The capacitor must be connected between this pin and VSS. |



6.3 System Bus Pins

| Symbol | I/O | Description | | | | | | | | | | | | | | | | | | |
|--|-------------|---|-------|-------------|---------------------|------|------------|--------------|---|-----|----|-------|----------|---|---|-----|----|-----|------------|-----|
| RESB | I | Reset input pin. When RESB is "L," initialization is executed. | | | | | | | | | | | | | | | | | | |
| D0/SCL D1/SDA D2 D3/SMODE D4.SPOL D5-D7 | I/O | Data bus/ Signal interface related pins. When the parallel interface is selected (P/S = "H"), the D7-D0 are 8-bit bi-directional data bus connecting to the MPU data bus. When the serial interface is selected (P/S = "L"), D0 and D1 (SCL, SDA) are used as serial interface pins. SCL: Input pin for data transfer clock SDA: Serial data input pin SMODE: Serial transfer mode select pin SPOL: RS pole select pin when the 3-wire serial interface is selected. SDA data is latched at the rising edge of SCL. Internal serial/parallel conversion into 8-bit data occurs at the rising edge of the 8th clock of SCL. After data transfer is complete or when making no access, you must set SCL to "L." | | | | | | | | | | | | | | | | | | |
| CSB | I | Chip select input pin CSB = "L": accepts access from MPU CSB = "H": denies access from MPU | | | | | | | | | | | | | | | | | | |
| RS | I | RAM/Register select input pin RS = "0": D7-D0 to display RAM data RS = "1": D7-D0 to control register data | | | | | | | | | | | | | | | | | | |
| RDB (E) | I | Read/Write control pin Select 80-family MPU type (M86 = "L") The RDB is a data read signal. When RDB is "L", D7-D0 are in an output status. Select 68-family MPU type (M86 = "H") R/WB = "H": When E is "H," D7-D0 are in an output status. R/WB = "L": Data on D7-D0 are latched at the falling edge for the E signal. | | | | | | | | | | | | | | | | | | |
| WRB (R/WB) | I | Read/Write control pin Select 80-family MPU type (M86 = "L") The WRB is a data write signal. Data on D7-D0 are latched at the rising edge of the WRB signal. Select 68-family MPU type (M86 = "H") Read/Write control input pin. R/W = "H": Read R/W = "L": Write | | | | | | | | | | | | | | | | | | |
| M86 | I | MPU interface type select input pin. M86 = "H": 68-family interface M86 = "L": 80-family interface Fixed at either "H" or "L" | | | | | | | | | | | | | | | | | | |
| TEST | I | For testing. Fix to "L." | | | | | | | | | | | | | | | | | | |
| P/S | I | Parallel/Serial interface select pin <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>P/S</th> <th>Chip Select</th> <th>Data Identification</th> <th>Data</th> <th>Read/Write</th> <th>Serial Clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>CSB</td> <td>RS</td> <td>D0-D7</td> <td>RDB, WRB</td> <td>-</td> </tr> <tr> <td>L</td> <td>CSB</td> <td>RS</td> <td>SDA</td> <td>Write only</td> <td>SCL</td> </tr> </tbody> </table> <p>P/S = "H": For parallel interface P/S = "L": For serial interface. Fixed D15-D5 pins are Hi-Z, RDB and WRB pins to either "H" or "L."</p> | P/S | Chip Select | Data Identification | Data | Read/Write | Serial Clock | H | CSB | RS | D0-D7 | RDB, WRB | - | L | CSB | RS | SDA | Write only | SCL |
| P/S | Chip Select | Data Identification | Data | Read/Write | Serial Clock | | | | | | | | | | | | | | | |
| H | CSB | RS | D0-D7 | RDB, WRB | - | | | | | | | | | | | | | | | |
| L | CSB | RS | SDA | Write only | SCL | | | | | | | | | | | | | | | |



6.4 LCD Driver Circuit Signals

| Symbol | I/O | Description | | | | | | | | | | | | | | | |
|----------------------|-----|---|------|---|--------------|---|---|-----|---|---|----|---|---|----|---|---|----|
| SEG0 to SEG159 | O | <p>Segment output pins for LCD drives.</p> <p>According to the Display RAM data, not lighted at "0", lighted at "1" (Normal Mode). Not lighted at "1", lighted at "0" (Reverse Mode) and, by a combination of the M signal and display data, one signal level among V0,V2,V3 and VSS signal levels are selected.</p> <p>Normal Mode Reverse Mode</p> | | | | | | | | | | | | | | | |
| COM0 to COM127 | O | <p>Common output pins for the LCD drivers. By combining the scanned data and M signal, one signal level among V0, V1, V4 and VSS signal level is selected.</p> <table border="1"> <thead> <tr> <th>Data</th> <th>M</th> <th>Output Level</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>VSS</td> </tr> <tr> <td>L</td> <td>H</td> <td>V1</td> </tr> <tr> <td>H</td> <td>L</td> <td>V0</td> </tr> <tr> <td>L</td> <td>L</td> <td>V4</td> </tr> </tbody> </table> | Data | M | Output Level | H | H | VSS | L | H | V1 | H | L | V0 | L | L | V4 |
| Data | M | Output Level | | | | | | | | | | | | | | | |
| H | H | VSS | | | | | | | | | | | | | | | |
| L | H | V1 | | | | | | | | | | | | | | | |
| H | L | V0 | | | | | | | | | | | | | | | |
| L | L | V4 | | | | | | | | | | | | | | | |

6.5 Oscillating Circuit Pins

| Symbol | I/O | Description |
|--------|-----|--|
| CKS | I | <p>Display timing clock source select input pin.</p> <p>CKS = "H": Use external clock from CK pin.</p> <p>CKS = "L": Use internal oscillated clock.</p> <p>In the case of TCP, draw it as a separate terminal.</p> |
| CK | I/O | <p>External clock input pin for displaying the timing (CKS=1) or internal clock output pin for displaying the timing (CKS=0).</p> <p>When using the internal oscillated clock, CK must be floating.</p> |

6.6 EEPROM Power Pins

| Symbol | I/O | Description |
|--------|-----|---|
| VPP | I | External power-forcing pin for programming or erasing EEPROM, 17~18V. |

7 Functional Description

7.1 MPU Interface

7.1.1 Reset Pin Description (RESB)

Hold the RESB at low for at least 40us after which the EM65101 accepts this reset command.

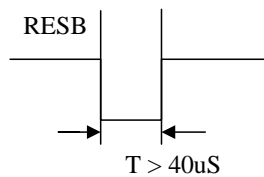


Figure 7-1 RESB Timing

7.1.2 Selection of Interface Type

The EM65101 transfers data through the 8-bit parallel I/O (D7-D0) or serial data input (SDA, SCL). You can use the P/S pin to select the parallel or serial interface. When the serial interface is selected, you are allowed to write data but data reading is not allowed.

| P/S | I/F Type | CSB | RS | RDB | WRB | M86 | SDA | SCL | Data |
|-----|----------|-----|----|-----|-----|-----|-----|-----|-------|
| H | Parallel | CSB | RS | RDB | WRB | M86 | - | - | D7~D0 |
| L | Serial | CSB | RS | - | - | - | SDA | SCL | - |

7.1.3 Parallel Input

When the parallel interface is selected with the P/S pin, the EM65101 allows data to be transferred in parallel to an 8-bit MPU through the data bus. For the 8-bit MPU, you can use the M86 pin to select either the 80-family or the 68-family MPU interface.

| M86 | MPU Type | CSB | RS | RDB | WRB | Data |
|-----|---------------|-----|----|-----|------|-------|
| H | 68-family MPU | CSB | RS | E | R/WB | D7~D0 |
| L | 80-family MPU | CSB | RS | RDB | WRB | D7~D0 |

7.1.4 Read/Write Functions of the Register and Display RAM

The EM65101 have four read/write functions in parallel interface mode. Each read/write function is selected by combinations of RS, RDB, and WRB signals.

| RS | 68-family R/WB | 80-family | | Function |
|----|----------------|-----------|-----|-------------------------|
| | | RDB | WRB | |
| 1 | 1 | 0 | 1 | Read internal Register |
| 1 | 0 | 1 | 0 | Write internal Register |
| 0 | 1 | 0 | 1 | Read display data |
| 0 | 0 | 1 | 0 | Write display data |



7.1.5 Serial Interface

The EM65101 has two types of serial interfaces, i.e., 3-wire or 4-wire serial interface. Use the SMODE pin to select the serial interface type.

SMODE = "L": 4-wire serial interface

SMODE = "H": 3-wire serial interface

7.1.5.1 4-Wire Serial Interface

When chip select is active (CSB = "L"), 4-wires type serial interface works through the SDA and SCL input pins. When chip select is inactive (CSB = "H"), the internal shift register and counter are reset to the initial condition. Serial data SDA are input sequentially in the order of D7 to D0 at the rising edge of the serial clock (SCL). The RS pin determines whether serial data input (SDA) is used as display RAM data or as control register data.

RS = "L": display RAM data

RS = "H": register control data

After completing the 8-bit data transfer, or when making no access, be sure to set the serial clock input (SCL) to "L." Care should be taken during PCB layout to avoid external noise from contaminating the SDA and SCL signals. To prevent any transfer error due to external noise, release chip select (CSB = "H") after every complete 8-bit data transfer.

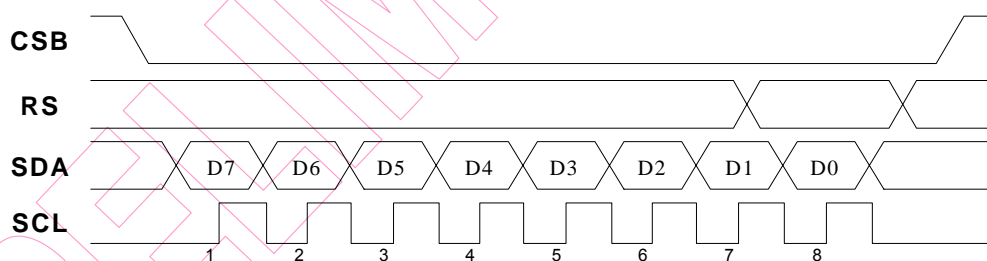


Figure 7-2 4-Wire Serial Interface

7.1.5.2 3-Wire Serial Interface

When chip select is active (CSB = "L"), 3-wire serial interface works through the SDA and SCL input pins. When chip select is inactive (CSB = "H"), the internal shift register and counter are reset to the initial condition. Serial data SDA are input sequentially in the order of RS, D7 to D0 at the rising edge of the serial clock (SCL). The first serial input data (RS) and the SPOL pin determine whether serial data input (SDA) is used as display RAM data or as control register data.

| SPOL = "0" | | SPOL = "1" | |
|------------|-----------------------|------------|-----------------------|
| RS | Display RAM/Register | RS | Display RAM/Register |
| 0 | Display RAM Data | 0 | Control Register Data |
| 1 | Control Register Data | 1 | Display RAM Data |

After completing the 9-bit data transfer, or when making no access, be sure to set the serial clock input (SCL) to "L." Care should be taken during PCB layout to avoid external noise from contaminating the SDA and SCL signals. To prevent any transfer error due to external noise, release chip select (CSB = "H") after every complete 9-bit data transfer.

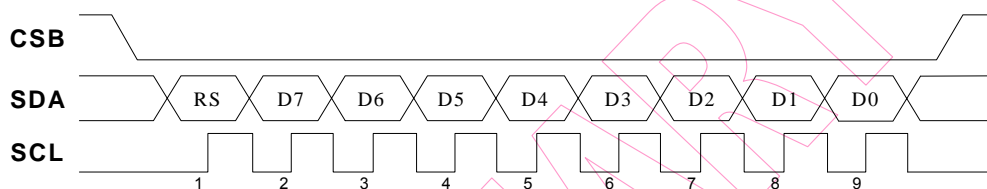


Figure 7-3 3-Wire Serial Interface

7.2 Writing Data to Display RAM and Control Register

The procedure to write data to the display RAM and Control Register is similar except for the RS selection to select the accessed object.

RS = "L": Display RAM data

RS = "H": Control register data

In the case of the 80-family MPU, data is written at the rising edge of WRB. In the case of the 68-family MPU, data is written at the falling edge of signal E.

7.2.1 Writing Data Operation

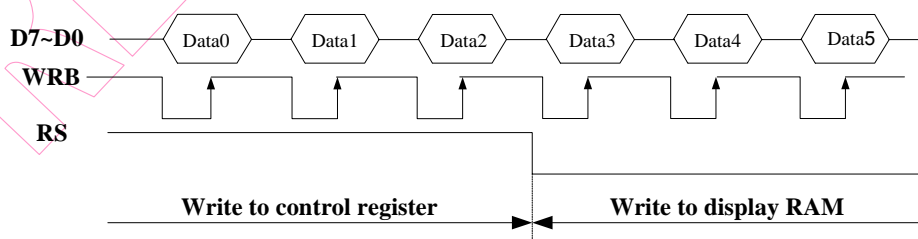


Figure 7-4 Writing Data Operation



7.2.2 Writing Data to Display RAM Data

The EM65101 is a 128-row by 160-column addressable array. Each pixel can be accessed when the X and Y addresses are specified. The 128 rows are divided into 16 Y addresses of 8 lines. Data is read from or written to the 8 lines of X address directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microcomputer can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM and displayed at the same time without causing any LCD flicker.

7.3 Y and X Address Circuits

7.3.1 Y Address Circuit

This circuit incorporates 4-bit Y address register which can only be changed by the "Y address" instruction. The Y address is set from 0 to 15.

7.3.2 X Address Circuit

This circuit assigns display RAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting the X address repeatedly, it is possible to scroll the screen and switch the Y address without changing the contents of the on-chip RAM. It incorporates the 7-bit Y address register which can only be changed by the initial display line instruction and the 7-bit counter circuit. At the beginning of each LCD frame, the contents of the register are copied to the X address counter which is incremented by the FLM signal. Thus generating the X address for transferring the 128-bit RAM data to the display latch circuit.

The REF select instruction makes it possible to invert the relationship between the X address and the segment outputs. It is necessary to rewrite the display data on the built-in RAM after issuing a REF select instruction. See and refer the following Figures 7-5 and 7-6.

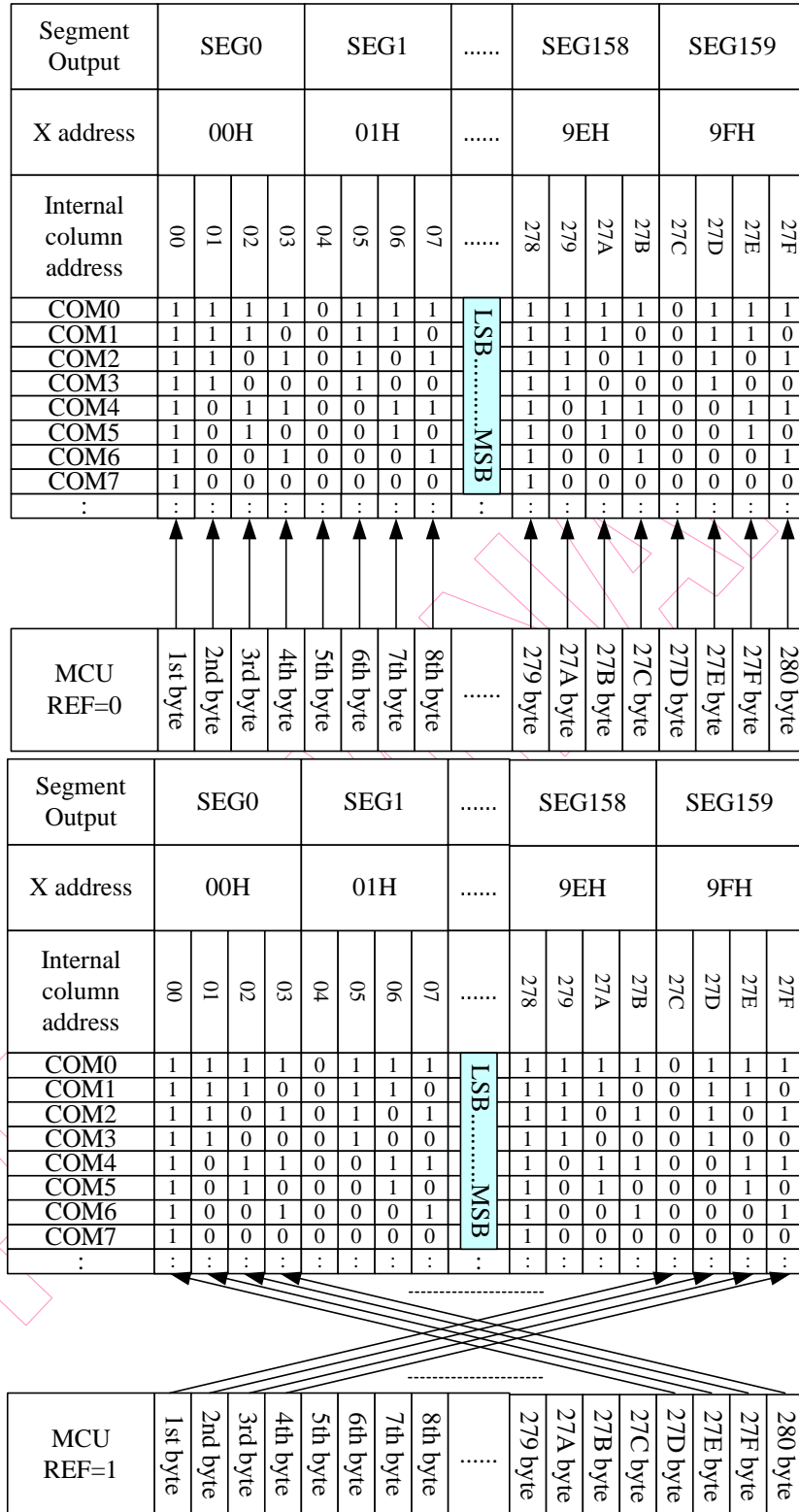


Figure 7-5 REF Control of the Relationship between the X Address and the Segment Outputs



7.3.3 EM65101 Display RAM Mapping

| | | | | | | | | | | | | | | | |
|-----------|----|----|----|-------|------|------|------|------|-------------|--|--------|--------|--------|--------|-----------|
| 0 | 0 | 0 | 0 | D0 | | | | | LSB.....MSB | | | | | 00H | COM0 |
| | | | | D1 | | | | | | | | 01H | COM1 | | |
| | | | | D2 | | | | | | | | 02H | COM2 | | |
| | | | | D3 | | | | | | | | 03H | COM3 | | |
| | | | | D4 | | | | | | | | 04H | COM4 | | |
| | | | | D5 | | | | | | | | 05H | COM5 | | |
| | | | | D6 | | | | | | | | 06H | COM6 | | |
| | | | | D7 | | | | | | | | 07H | COM7 | | |
| 0 | 0 | 0 | 1 | D0 | | | | | | | | | | 08H | COM8 |
| | | | | D1 | | | | | | | | | | 09H | COM9 |
| | | | | D2 | | | | | | | | | | 0AH | COM10 |
| | | | | D3 | | | | | | | | | | 0BH | COM11 |
| | | | | D4 | | | | | | | | | | 0CH | COM12 |
| | | | | D5 | | | | | | | | | | 0DH | COM13 |
| | | | | D6 | | | | | | | | | | 0EH | COM14 |
| | | | | D7 | | | | | | | | | | 0FH | COM15 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | | | | | | | | | | ⋮ | ⋮ |
| 1 | 1 | 1 | 0 | D0 | | | | | | | | | | 70H | COM112 |
| | | | | D1 | | | | | | | | | | 71H | COM113 |
| | | | | D2 | | | | | | | | | | 72H | COM114 |
| | | | | D3 | | | | | | | | | | 73H | COM115 |
| | | | | D4 | | | | | | | | | | 74H | COM116 |
| | | | | D5 | | | | | | | | | | 75H | COM117 |
| | | | | D6 | | | | | | | | | | 76H | COM118 |
| | | | | D7 | | | | | | | | | | 77H | COM119 |
| 1 | 1 | 1 | 1 | D0 | | | | | | | | | | 78H | COM120 |
| | | | | D1 | | | | | | | | | | 79H | COM121 |
| | | | | D2 | | | | | | | | | | 7AH | COM122 |
| | | | | D3 | | | | | | | | | | 7BH | COM123 |
| | | | | D4 | | | | | | | | | | 7CH | COM124 |
| | | | | D5 | | | | | | | | | | 7DH | COM125 |
| | | | | D6 | | | | | | | | | | 7EH | COM126 |
| | | | | D7 | | | | | | | | | | 7FH | COM127 |
| Y address | | | | REF=0 | 00 | 01 | 02 | 03 | | | 9C | 9D | 9E | 9F | X address |
| | | | | REF=1 | 9F | 9E | 9D | 9C | | | 03 | 02 | 01 | 00 | |
| D3 | D2 | D1 | D0 | | SEG0 | SEG1 | SEG2 | SEG3 | | | SEG156 | SEG157 | SEG158 | SEG159 | SEG |

Figure 7-6 Display RAM Mapping Diagram

7.4 Internal Register Read

When reading data from the display RAM, a dummy read is initially required. The designated address data is not output to the read operation immediately after the address is set to the AX or AY register. It is output when the second data is read. Dummy read is always initially required after address is set and the write cycle is started.

7.4.1 Read Display RAM Operation

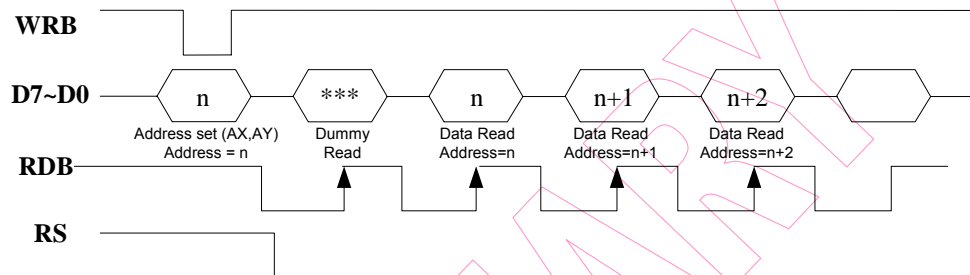


Figure 7-7 Read Display RAM Operation

The EM65101 can read the control registers. When issuing a control register read operation, the upper data bus nibble (D7-D4) is used for the register address (0 to FH). Up to 16 registers can be accessed directly. However, more than 16 registers are provided. To solve this over supply problem, the EM65101 uses the register bank control to access the RE register with a bank number. You can access the RE register through any bank. The following lists the steps to be taken when accessing the specific register using the bank access control.

1. Write 01H to the RE register for accessing the RA register.
2. Write the specific register address to the RA register.
3. Write the specific register bank to the RE register.
4. Read the specific register contents.

7.4.2 Register Read Operation

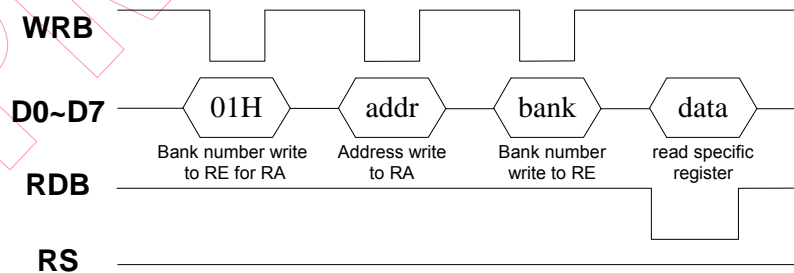


Figure 7-8 Register Read Operation

7.4 Display RAM Access Using Window Function

The EM65101 has a window area setting command for accessing a specified display RAM area. To use the window function, you need to set up the X & Y address positions. In addition, you also need to enable the auto-increment mode (AXI="1", AYI="1"). These two positions represent the window start position and window end position. Set the X address (AX) and Y address (AY) registers to specify the window start position of X and Y respectively. Set the Window X End address (EX) and Window Y End address (EY) to specify the window end positions of X and Y respectively. When accessing the window function, you can set AIM to "1" to modify write access. You should set the following registers before accessing RAM when you use the window function. Note that the Window Y End address setting can be set only as COM8, COM16..., COM127.

WIN = "1," AXI="1," AYI="1"

X address, Y address, Window X End address, Window Y End address

Moreover, these addresses should be kept in the following conditions:

- Window End X address(EX) Window Start X address (AX)
- Window End Y address(EY) Window Start Y address (AY)

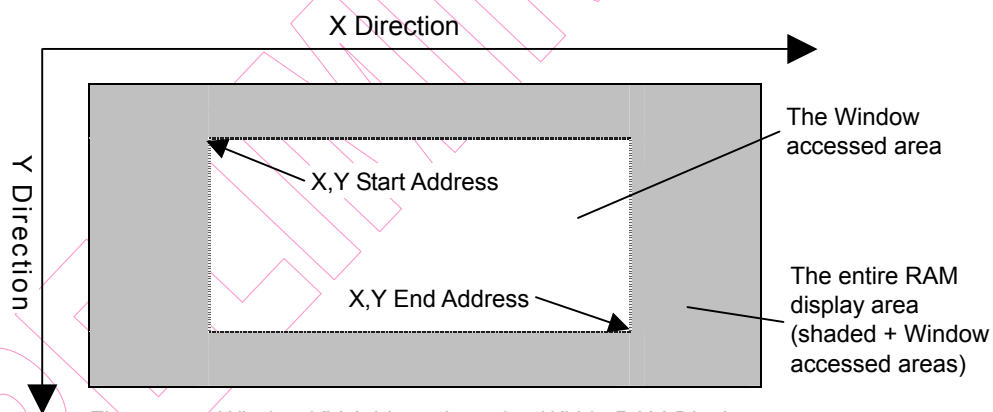


Figure 7-9 Window XY Address Location Within RAM Display

7.5 Display RAM Data and LCD

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by the REV register are set up as follows:

- Normal display (REV=0): RAM data = "0," not lit
RAM data = "1," lit
- Reverse display (REV=1): RAM data = "0," lit
RAM data = "1" not lit



7.6 Display Timing Circuit

The display timing circuit generates internal signals and timing pulses (internal LP, FLM, and M) by the clock.

| Symbol | Description |
|----------------|---|
| LP (internal) | The LP is a latch clock signal. At the raising edge, count the display line counter. At the falling edge, output the LCD drive signal. |
| FLM (internal) | The signal for the LCD display synchronous signals. When FLM is set to "H," the display start-line address is present. |
| M (internal) | The signal for alternate signals of LCD drive output |

7.6.1 Signal Generation for the Display Line Counter and the Display Data Latching Circuit

Clock frequencies are generated to the line counter and the display data latching circuit from the display clock (internal LP). Synchronized with the display clock (internal LP), the line addresses of Display RAM are generated and the 160-segment bits display data are latched to display data latching circuit to output to the LCD drive circuit (Segment outputs). Display data read out of to the LCD drive circuit is completely independent of MPU. Thus, MPU has no relationship to the read-out operation which accesses the display data.

7.6.2 Generation of the Alternate Signal M (Internal) and the Synchronous Signal FLM (Internal)

LCD alternate signal M (internal) and synchronous signal FLM (internal) are generated by the display clock LP (internal). FLM generates alternated drive waveform to the LCD drive circuit. Normally, FLM generates alternate drive waveform every frame (M-signal level is reversed every single frame). However, by setting up data in an n-line reverse register and n-line alternate control bit (NLIN), an n-line reverse waveform is generated at "1." These control bits are NLIN and EOR.

When NLIN = "H" :

EOR=0 M always reverses on the nth raster row regardless of whether the end of a frame is reached.

EOR=1 M reverses at the nth raster row and restarts the raster row count at the start of every frame.

7.6.3 Display Data Latching Circuit

Display data latching Circuit temporally latches display data that outputs display data to the LCD driver circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display all on functions are operated by controlling data in the display data latch. Therefore, no data within display RAM changes.

7.7 LCD Driver Output Timing

Display timing at Normal (not reverse mode), 1/128 Duty.

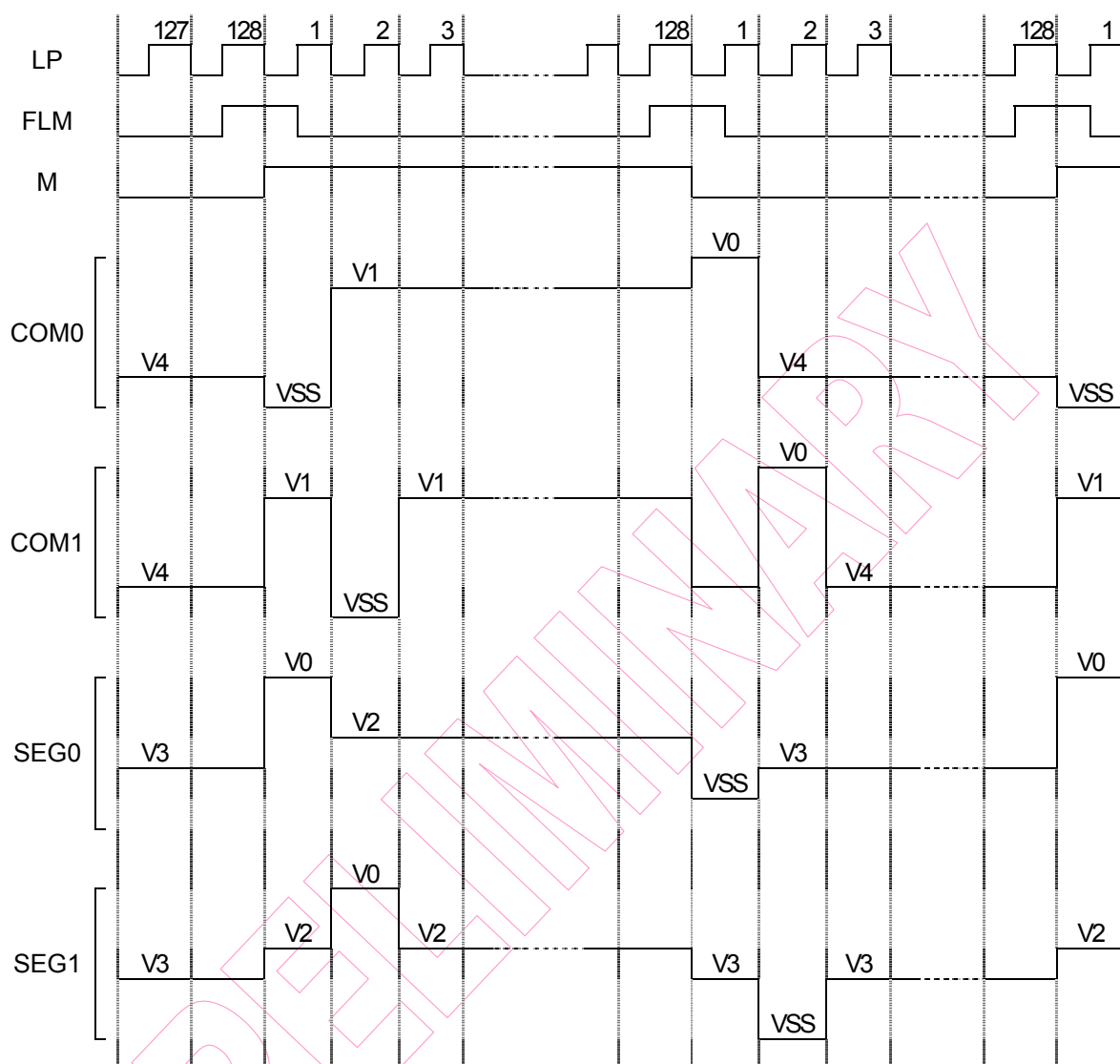


Figure 7-10 Normal Mode Display Timing Diagram

7.7.1 LCD Drive Circuit

This drive circuit generates four levels of LCD drive voltages. The circuit has 160-segment outputs and 128-common outputs and the outputs combine the display data and internal signal M. The common drive circuit that contains a shift register sequentially outputs common scan signals.

7.7.2 Oscillator Circuit

The EM65101 provides a CR oscillator. The output from this oscillator is used as the timing source for display signal and clock source for the clock booster.

When the external clock is used, the clock source is fed to the CK pin.

The duty cycle of the external clock must be 50%.

The ratio of the resistance at the CR oscillator is programmable. When you change this ratio, the frame frequency display is also changed.

7.8 Power Supply Circuit

This power circuit supplies the voltages necessary to drive an LCD. The circuit consists of a booster and a voltage converter.

Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3, and V4 that are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels.

Otherwise, the display quality will be degraded considerably. Instead, use an external power supply. When using external power supply, turn off the internal power supply (AMPON, DCON="00"), disconnect pins CAP1-, CAP1+, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP5+, V2X, VOUT, and VEE. Then, feed the external LCD drive voltages to Pins V0, V1, V2, V3, and V4. The power circuit can be controlled by power circuit related registers.

| DCON | AMPON | Booster Circuit | Voltage Conversion Circuit |
|------|-------|-----------------|----------------------------|
| 0 | 0 | Disable | Disable ¹ |
| 0 | 1 | Disable | Enable ² |
| 1 | 1 | Enable | Enable |

¹ Because the booster and the voltage converter are not operating, disconnect Pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP5+, V2X, VOUT and VEE.

Apply external LCD drive voltages to the corresponding pins.

² Because the booster is not operating, disconnect Pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP5+, and VEE.

Derive the voltage source to be supplied to the voltage converter from VOUT and the V2X pins.

7.9 Booster Circuit

Placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3-, across CAP4+ and CAP2-, across CAP5+ and CAP3-, and across VOUT/V2X and VSS, will boost the voltage coming from VEE and VSS n-times and output the boost up voltage to the VOUT pin. Voltages that are boost-up twice, three times, four times, and five times are output to the VOUT pin by the boost step register set. You can set the boost step registers.

- (1) In cases where the twice boost-up voltage is used, place C1 across CAP1+ and CAP1-, across V2X and VSS; and open CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP2-, CAP5+, and CAP3-.
- (2) In cases where the voltage that is boosted three times is used, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across V2X and VSS; and open CAP3+, CAP3-, CAP4+, CAP2-, CAP5+, and CAP3-

- (3) In cases where the four times boosted voltage is used, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3-, across V2X and VSS; and open CAP4+, CAP2-, CAP5+, and CAP3-
- (4) In cases where the voltage that is boosted five times is used, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3- across CAP4+ and CAP2-, across V2X and VSS; and open CAP5+ and CAP3-
- (5) In cases where the voltage that is boosted six times is used, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3-, across CAP4+ and CAP2-, across CAP5+ and CAP3-, and across V2X and VSS

When you use the built-in booster circuit, make sure the output voltage (VOUT) is less than the recommended operating voltage (18.0 Volt). If the output voltage (VOUT) is more than the recommended operating voltage, correct chip operation can NOT be guaranteed.

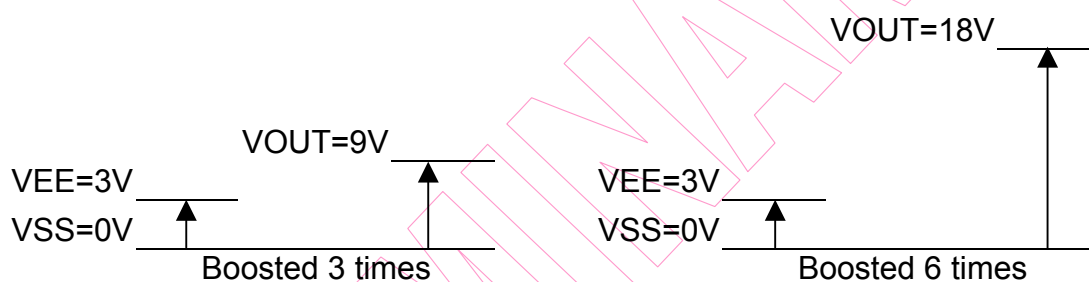


Figure 7-11 Correlation Between VEE and VOUT Boost-up Voltages

NOTE

The maximum voltage VOUT of 18V is automatically limited by hardware to avoid damage to the IC.

7.10 Electronic Volume

The voltage conversion circuit has a built-in electronic volume control, which allows VBA to be controlled by DV register settings. The DV registers are 7 bits providing 65 voltage values for the VBA. The relationship between VBA and DV is summarized in the following equation:

$$VBA = (1 + (M + \text{offset}) / 381) * VREF$$

$$V0 = VBA * N$$

Where:

M = DV register setting (offsets CV5 ~ CV0 setting on EEPROM)

N = RM register setting

VREF = Internal temperature compensation output voltage

7.11 Voltage Regulator

The EM65101 has a built-in reference voltage regulator, which regulates the amplified voltage from the internal temperature compensation output (VREF pin) to generate the LCD drive voltage (V0). Even if the boost-up voltage level fluctuates, V0 remains stable as long as VOUT is higher than V0. Stable power supply can be obtained by using this constant voltage, even if the load fluctuates. The EM65101 uses the generated LCD drive voltage (V0) level as the reference level for the electronic volume.

7.12 Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V0, that is; V1, V2, V3, and V4 are obtained by dividing V0 through a resistor network. The LCD drive voltage from EM65101 is biased at 1/4, 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12, & 1/13. When using the internal power supply, connect a stabilizing capacitor to each of Pins V0 to V4. The capacitor should be determined while selecting the LCD panel to be used. When using the external power supply, apply external LCD drive voltages to V0, V1, V2, V3, & V4. Disconnect Pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP5+, V2X, VOUT, & VEE. When using only the voltage conversion circuit, turn off the internal booster circuit, disconnect Pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP5+ and VEE. Get the voltage source to be supplied to the voltage converter from VOUT and V2X pins.

The following figure shows an application circuit on capacitor connections when using the internal power circuit (with the voltage boosted several times as shown).

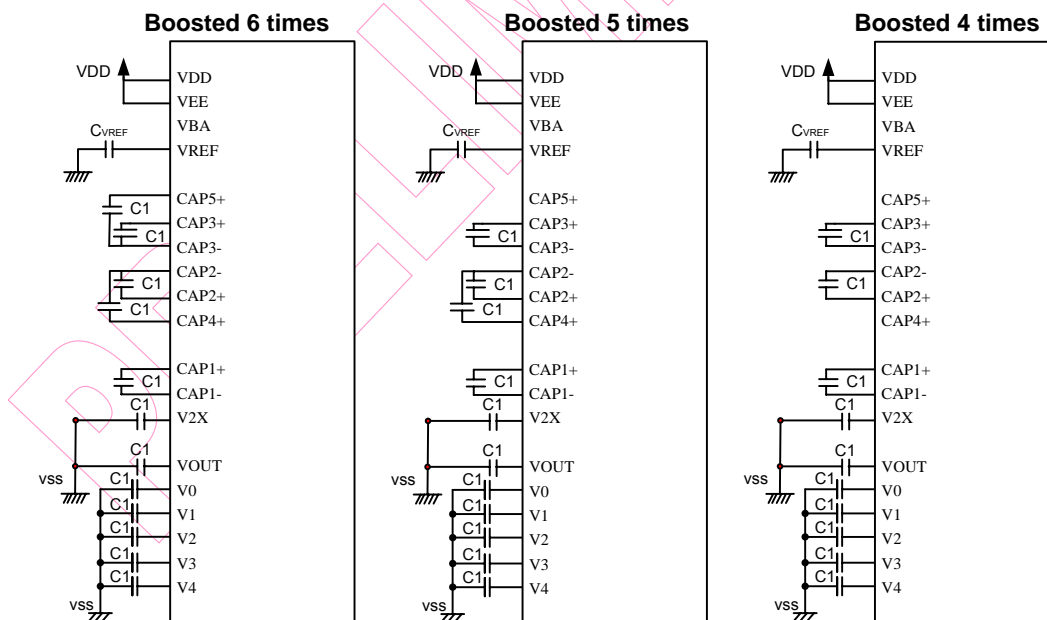


Figure 7-12a Internal Power Capacitor Connections Application Circuits
(Voltage Boosted 6, 5 and 4 Times)

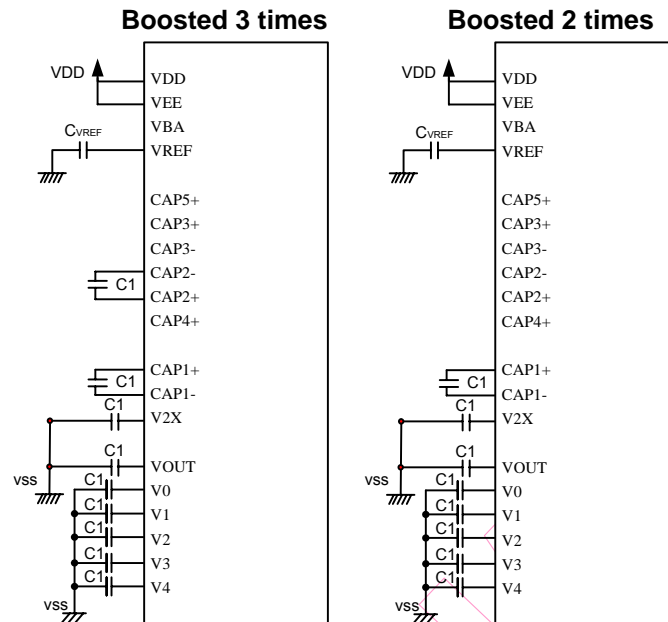


Figure 7-12b Internal Power Capacitor Connections Application Circuits
(Voltage Boosted 3 and 2 Times)

NOTE

1. Recommended values for C1 is 1uF, and for CVREF is 0.1uF.
2. To attain a stable voltage, it is recommended that you use VREF to connect a capacitor across CVREF and VSS.
4. Use of capacitor type X5R is recommended for C1 and CVREF.

7.13 EEPROM Function

The EM65101 supports EEPROM function that allows you to change the LCD operating voltage V_{op} . It can also select EEPROM operating mode and set to use internal or external power supply for EEPROM. In the EEPROM select register (Bank2 [0H]), then use (M1, M0) to select the operating mode for EEPROM:

| (M1, M0) | EEPROM Operating Mode | Delay Time |
|----------|-----------------------|--------------|
| 00 | Read | > 10 μ S |
| 01 | Program | > 4 mS |
| 10 | Erase | > 4 mS |
| 11 | Reserve | - |

NOTE

When using the EEPROM function, VDD must be larger than 2.8V ($V_{DD} > 2.8V$)

You can get the V_{op} calibration offset voltage by setting the V_{op} calibration offset register (Bank 2[1H & 2H]).

| CV5~CV0 | Calibration Offset |
|---------|--------------------|
| 011111 | +31 |
| 011110 | +30 |
| ... | ... |
| 000001 | +1 |
| 000000 | 0 |
| 100000 | -32 |
| 100001 | -31 |
| ... | ... |
| 111111 | -1 |

7.13.1 EEPROM Program, Read, and Erase Flow Charts

The following are the EEPROM Program, Read and Erase flow charts for achieving correct Vop offset voltage.

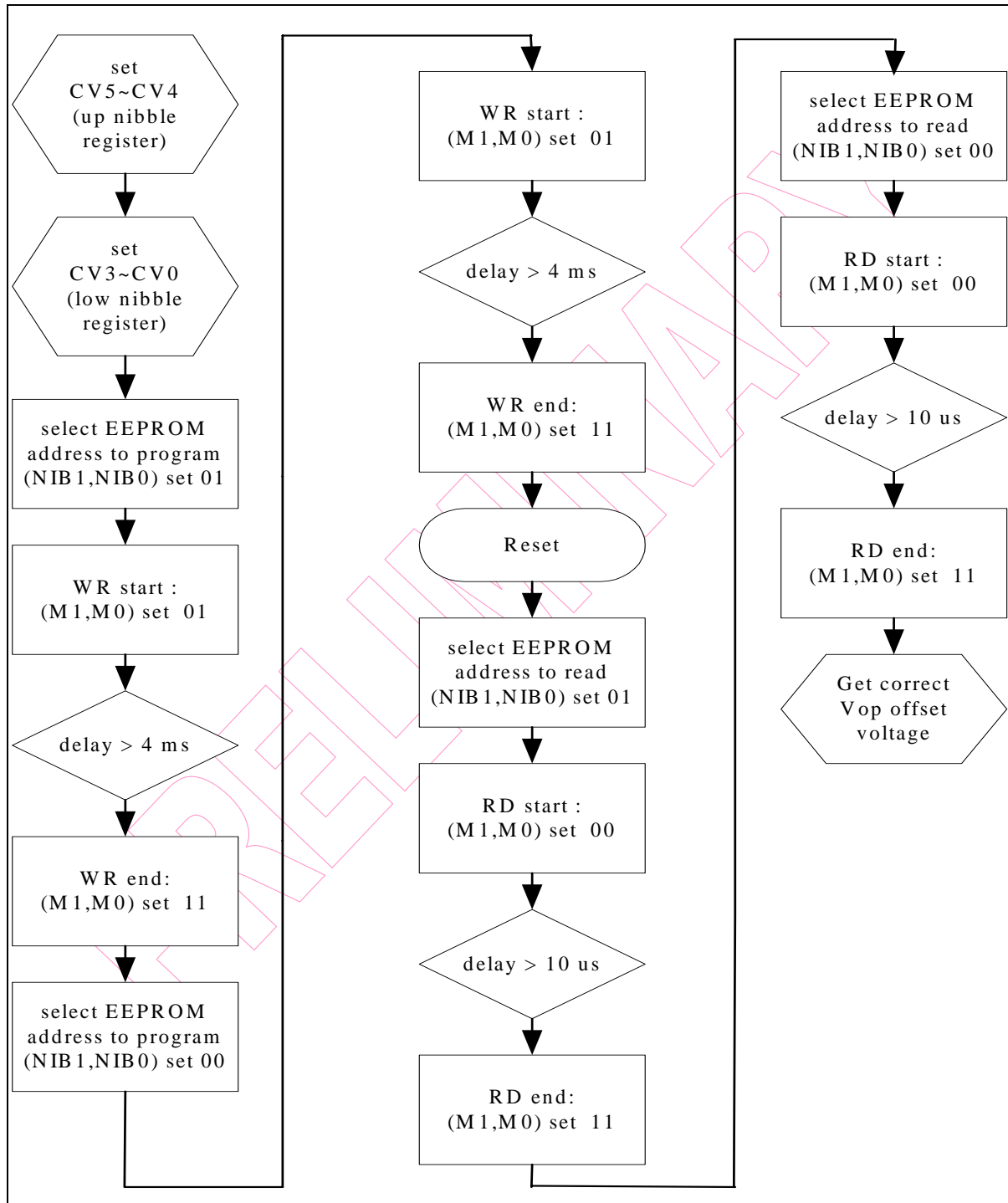


Figure 7-13 Program Flow Chart

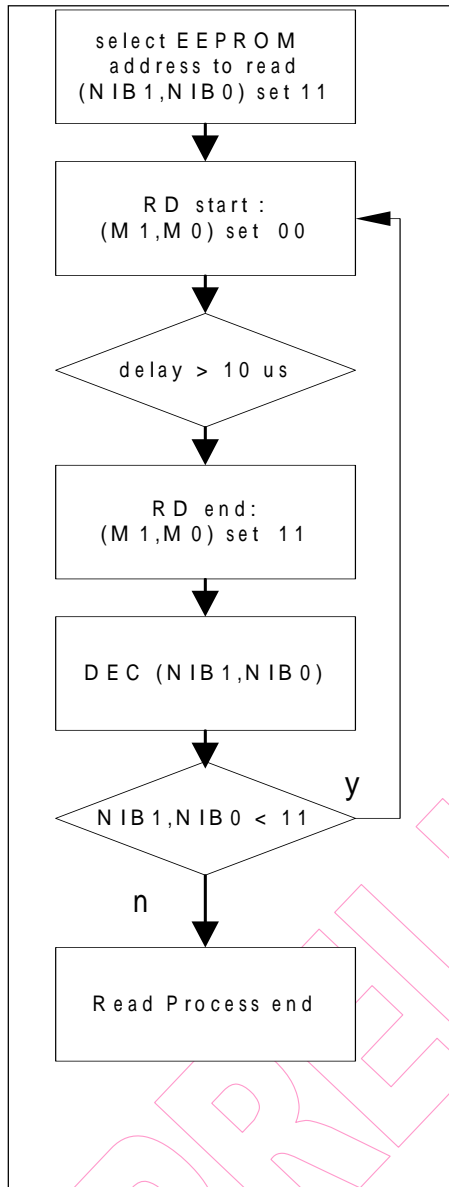


Figure 7-14 Read Flow Chart

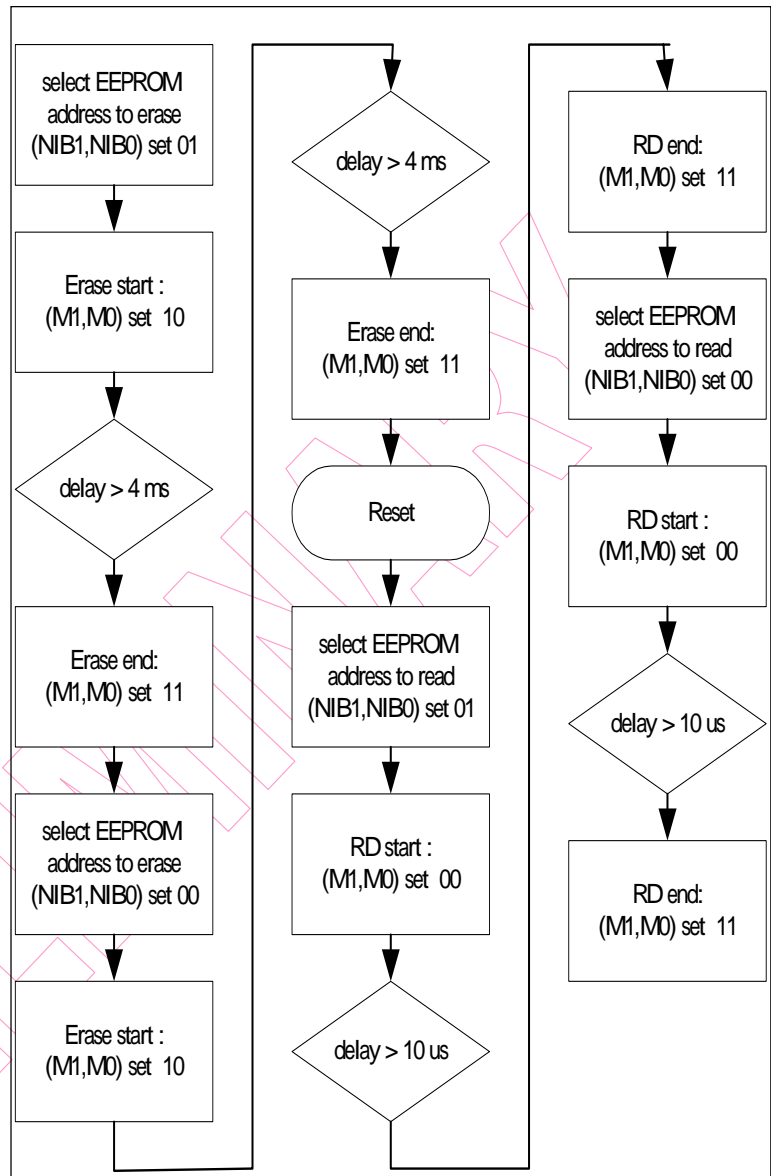


Figure 7-15 Erase Flow Chart



7.13.2 Vop Calibration Offset Examples

1) Program

Vop calibration offset is +30, CV5~CV0 is set to 011110

```
WRITE #F2H // set RE FLAG 010 → INSTRUCTION Bank 2
WRITE #11H // set CV5~CV4=01
WRITE #2EH // set CV3~CV0=1110
WRITE #51H // set NIB1~NIB0=01 → program CV5~CV4
WRITE #02H // set EEPROM operating mode →
           programming; EEPROM power is from internal V0
DELAY > 4 MS // wait > 4 ms to finish programming
WRITE #06H // set EEPROM mode → reserve (finish programming)
WRITE #50H // set NIB1~NIB0=00 → program CV3~CV0
WRITE #02H // set EEPROM operating mode →
           programming; EEPROM power is from internal V0
DELAY > 4 MS // wait > 4 ms to finish programming
WRITE #06H // set EEPROM mode → reserve (finish programming)
WRITE #F0H // set RE FLAG 000 → INSTRUCTION Bank 0
WRITE #81H // EM65101 reset
WRITE #F2H // set RE FLAG 010 → INSTRUCTION Bank 2
WRITE #51H // set NIB1~NIB0=01 → read CV5~CV4
WRITE #00H // set EEPROM operating mode → reading;
           read data from EEPROM to the CV5~CV4 registers
DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM to the CV5~CV4 registers)
WRITE #50H // set NIB1~NIB0=00 → read CV3~CV0
WRITE #00H // set EEPROM operating mode → reading; read data
           from EEPROM to the CV3~CV0 registers
DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM to the CV3~CV0 registers)
```

NOTE

- When setting CV5~CV0, you must set CV5~CV4 (upper nibble registers) first, then set CV3~CV0 (lower nibble registers), and then start to program.
- The programming sequence of CV5~CV4 and CV3~CV0 is not restricted.



2) Read

```
WRITE #F2H // set RE FLAG 010 → INSTRUCTION Bank 2
WRITE #53H // set NIB1~NIB0=11 → read Extension Command
WRITE #00H // set EEPROM operating mode → reading;
           read data from EEPROM

DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM

WRITE #52H // set NIB1~NIB0=10 → read Extension Command
WRITE #00H // set EEPROM operating mode → reading;
           read data from EEPROM

DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM

WRITE #51H //set NIB1~NIB0=01 → read CV5~CV4
WRITE #00H // set EEPROM operating mode → reading;
           read data from EEPROM to the CV5~CV4 registers

DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM to the CV5~CV4 registers)

WRITE #50H //set NIB1~NIB0=00 → read CV3~CV0
WRITE #00H // set EEPROM operating mode → reading; read data
           from EEPROM to the CV3~CV0 registers

DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM to the CV3~CV0 registers)
```

NOTE

When reading from CV5~CV0, you must read the EEPROM data to CV5~CV4 (upper nibble register) first, then read the EEPROM data to CV3~CV0 (lower nibble registers).



3) Erase

```
WRITE #F2H // set RE FLAG 010 → INSTRUCTION Bank 2
WRITE #51H // set NIB1~NIB0=01 → erase CV5~CV4
WRITE #04H // set EEPROM operating mode → erasing;
           EEPROM power is from internal V0

DELAY > 4 MS // wait > 4 ms to finish erasing
WRITE #06H // set EEPROM mode → reserve (finish erasing)
WRITE #50H // set NIB1~NIB0=00 → erase CV3~CV0
WRITE #04H // set EEPROM operating mode → erasing;
           EEPROM power is from internal V0

DELAY > 4 MS // wait > 4 ms to finish erasing
WRITE #06H // set EEPROM mode → reserve (finish erasing)
WRITE #F0H // set RE FLAG 000 → INSTRUCTION Bank 0
WRITE #81H // EM65101 reset
WRITE #F2H // set RE FLAG 010 → INSTRUCTION Bank 2
WRITE #51H // set NIB1~NIB0=01 → read CV5~CV4
WRITE #00H // set EEPROM operating mode → reading;
           read data from EEPROM to the CV5~CV4 registers

DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM to CV5~CV4 register)

WRITE #50H // set NIB1~NIB0=00 → read CV3~CV0
WRITE #00H // set EEPROM operating mode → reading; read data
           from EEPROM to the CV3~CV0 registers

DELAY >10 uS // wait >10 uS to finish reading
WRITE #06H // set EEPROM mode → reserve (finish reading data
           from EEPROM to CV3~CV0 register)
```

NOTE

CV5~CV0 should be equal to 1111 after erasing

7.14 Partial Display Function

The EM65101 has a partial display function, which can display a part of graphic display area. This function is used to set lower bias ratio, lower boost step, and lower LCD drive voltage. When setting the partial display function, the EM65101 consumes less power. The Partial display function is suitable for clock indication or calendar indication when portable equipment is on stand-by.

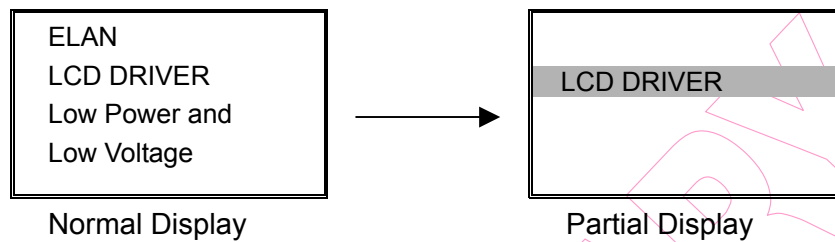


Figure 7-16 Partial Display Block Diagram

When using the partial display function, it is necessary to follow the sequence shown below.

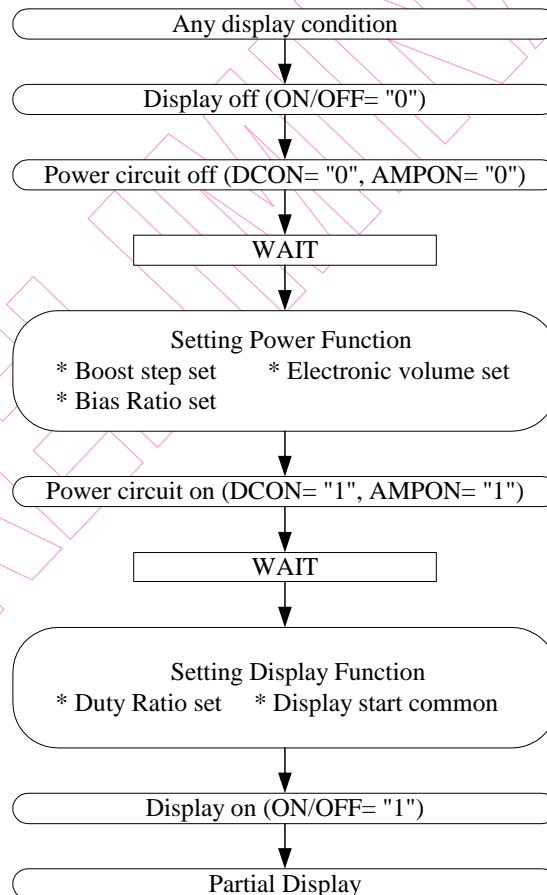


Figure 7-17 Partial Display Function Sequential Flow

Select a display duty ratio for the partial display from 1/8 to 1/128 using the DS (LCD duty ratio) register.

Set the most suitable values for LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and others according to the actual LCD panel and selected duty ratio in use.

7.15 Discharge Circuit

The EM65101 has a built-in the discharge circuit, which discharges electricity from the capacitors to provide stable power sources (V0~V4). The discharge circuit is valid when the DIS register is set to "1." When the built-in power supply is used, be sure to set DIS="1" after the power source is turned off (DCON, AMPON)=(0, 0).

CAUTION!!!

Do NOT turn on both the built-in power source and the external power source (V0~V4, VOUT) while DIS ="1."

7.16 Scroll Function

This function specifies a portion of screen for scrolling. It sets the scroll top address, scroll bottom address, scroll specified address, scroll mode of the scrolling area, and scroll start address. Note that the scroll top address should be smaller than the scroll bottom address, i.e.,

$0 \leq \text{scroll top address, scroll bottom address, scroll specified address} \leq 127$;

scroll top address \leq scroll start address \leq scroll bottom address.

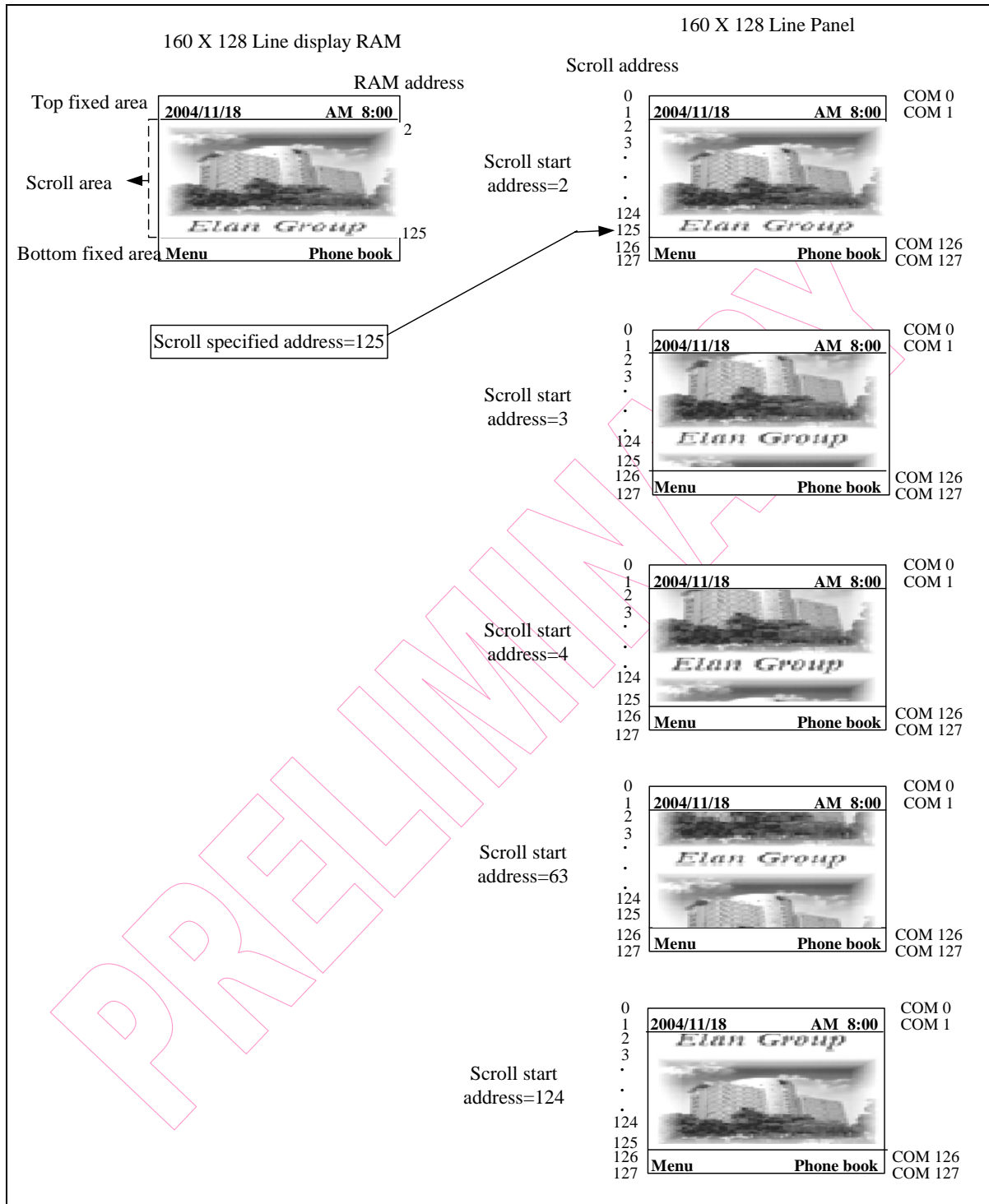


Figure 7-18 Example on Scroll Function Display vs. Address Values

Set the scroll top address and scroll bottom address to define the area of scrolling data in RAM

Example:

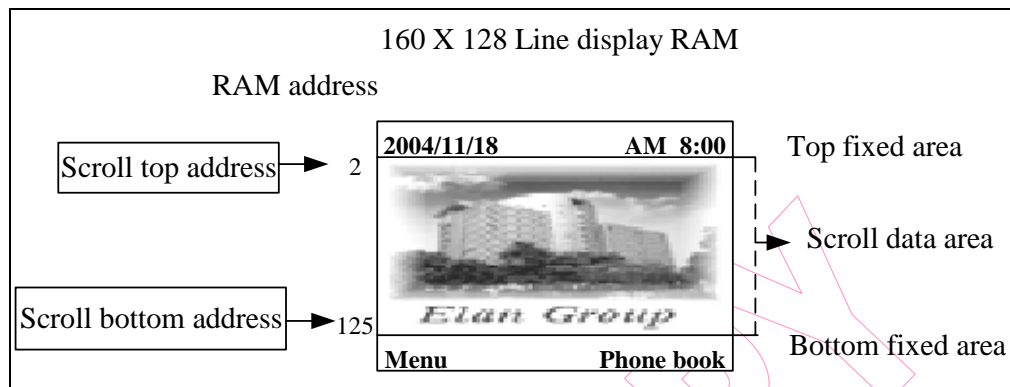


Figure 7-19 Setting the Scrolling Data Area in RAM

Set the scroll specified address according to the panel size and duty selection to specify the address to which to jump relative to the scroll bottom address. Then display the fixed bottom data area. Note that scroll specified address = scroll top address + panel scroll area – 1

Example: (160 x 128 Line panel; 1/32 duty, partial display)

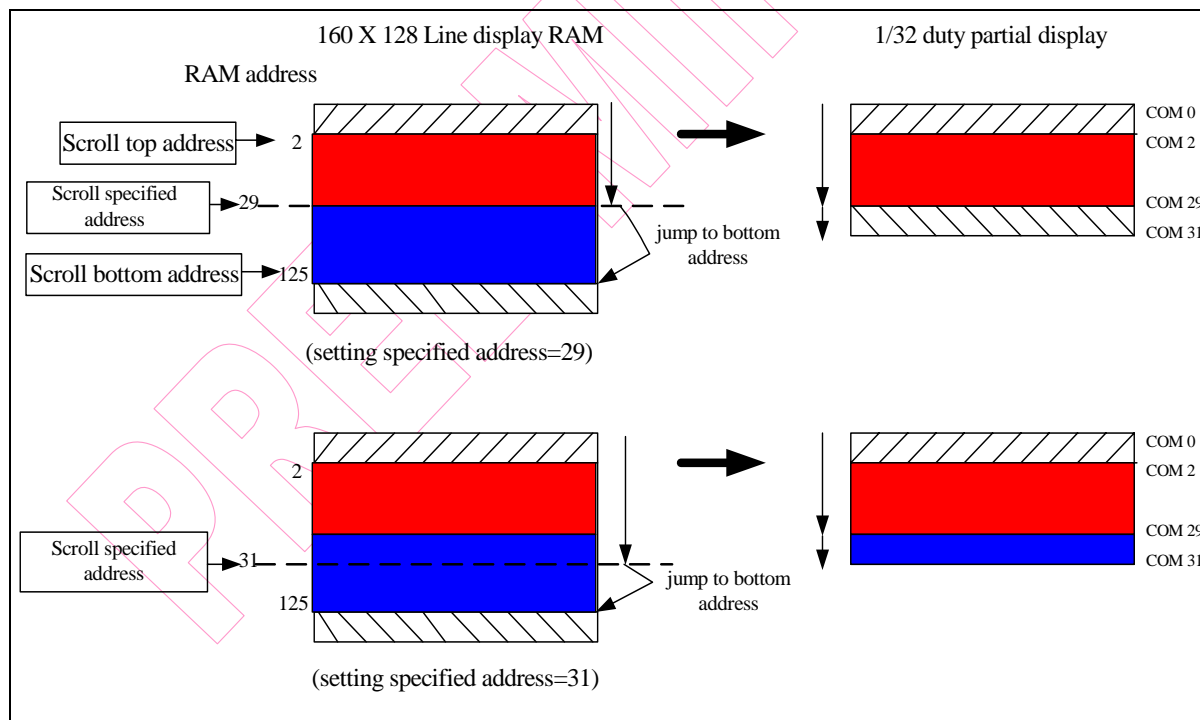


Figure 7-20 Setting the Scroll Bottom Address of a Scrolling Area

NOTE

You must set the scroll top address, the scroll bottom address, the scroll specified address, and the scroll start address carefully when using the scroll function. If there is any error, the scrolling result will be inaccurate. Follow the rules shown below:

Scroll top address <= Scroll bottom address

Scroll specified address = Scroll top address + panel scroll area - 1

Scroll top address <= Scroll start address <= Scroll bottom address

7.17 Initial Values

| ITEM | Initial Value |
|-------------------------------|-----------------------------|
| Display RAM | Not fixed |
| X Address | 00H set |
| Y Address | 00H set |
| Display starting common | Set at the first common(0H) |
| Display ON/OFF | Display OFF |
| Display Normal/Reverse | Normal |
| Display duty | 1/128 |
| n-line alternated | Every frame unit |
| (BF1,BF0) | (0,0) |
| Common shift direction | COM0 COM127 |
| Increment mode | Increment OFF |
| Register in electronic volume | (0,0,0,0,0,0,0) |
| Power Supply | OFF |
| Bias ratio | 1/12 bias |
| Booster | 6 times |
| Discharge Register | Disabled |
| RM value | 8.9 times |
| Windows function | Disabled |
| Scrolling function | Disabled |

7.18 Safety Measures when Switching Power ON and OFF

The high current that may occur when a voltage is supplied to the LCD driver power supply while the system power supply is floating, could permanently damage the LSI. Hence, the precautionary actions as detailed below should be taken into considerations seriously when switching power on and off.

7.18.1 When Using the External Power Supply

Power ON Proper Sequence:

- 1) Logic system (VDD) power ON, perform a reset operation
- 2) Supply the external LCD drive voltage to the corresponding pins (V0, V1, V2, V3 and V4)



Power OFF Proper Sequence:

- 1) Set the HALT register to "1" or perform a reset operation
- 2) Cut off external LCD drive voltage
- 3) Logic system (VDD) power OFF

NOTE

Connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V0 or VOUT (when using the internal voltage conversion circuit) of the system as a current limiter. In addition, set a suitable resistor value of the resistor depending on the quality of the LCD display.

7.18.2 When Using the Built-in Power Supply

Power ON Proper Sequence:

- 1) Logic system (VDD) power ON
- 2) Booster circuit system (VEE) power ON
- 3) Perform a reset operation and enable the booster and voltage conversion circuit.

NOTE

If the VDD and VEE voltages do NOT have the same potential, the logic system (VDD) is automatically powered on first.

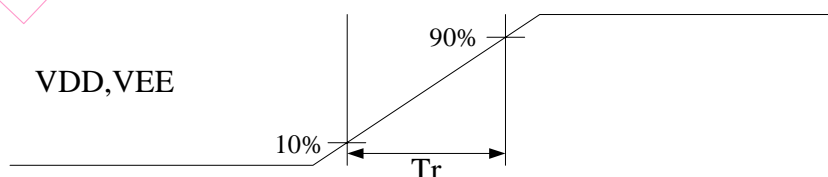
Power OFF Proper Sequence:

- 1) Set the HALT register to "1" or perform a reset operation
- 2) Booster circuit system (VEE) power OFF
- 3) Logic system (VDD) power OFF

If VDD and VEE do NOT have the same potential, cut off VEE first. After the VEE, VOUT, V0, V1, V2, V3, and V4 voltages are below the LCD ON voltage (threshold voltage when the Liquid Crystal is turned on), power off the logic system (VDD).

7.18.3 Power Supply Rising Time

Although there is no constraint on the rising time of the power supply, the Tr (rising time) as illustrated below is recommended for practical applications.



| Item | Recommended Rising Time (Tr) | Applicable Power |
|------|------------------------------|------------------|
| Tr | 30 μ S ~ 10ms* | VDD, VEE |

* The rising time is the time between 10% and 90% of VDD, VEE

Figure 7-21 Recommended Rising Time (Tr) for Practical Application

7.19 Register Setting Examples

7.19.1 Initialization

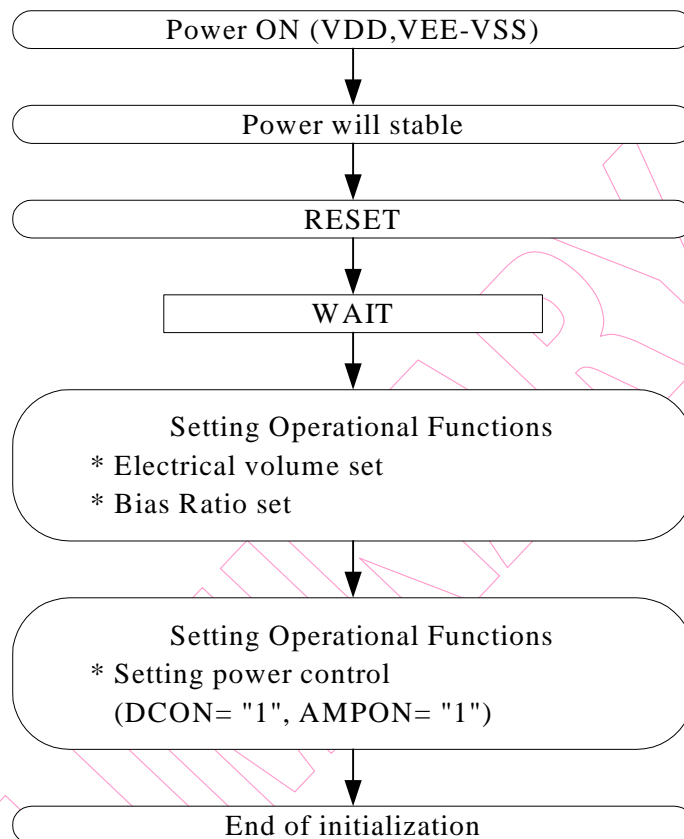


Figure 7-22 Initialization Register Setting Sequential Flow

7.19.2 Display Data

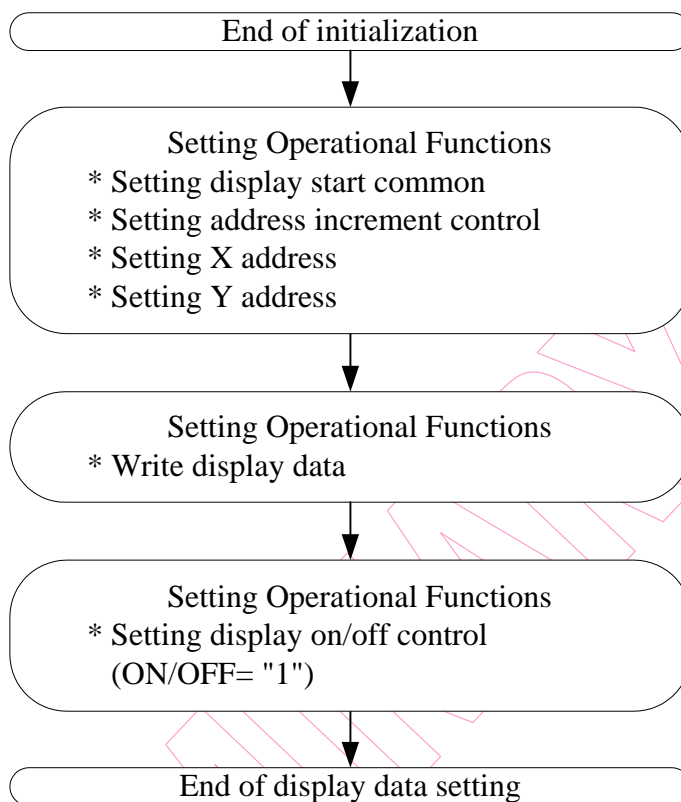


Figure 7-23 Display Data Register Setting Sequential Flow

7.19.3 Power OFF

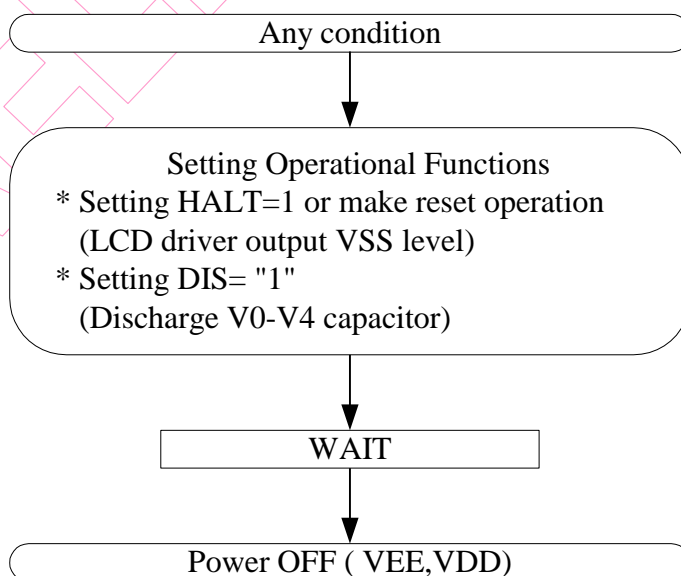


Figure 7-24 Power Off Register Setting Sequential Flow



8 Control Register

8.1 Control Registers

8.1.1 Control Register (Bank 0)

| Control Register | Pins (for 80-Family) & Bank | | | | | | | | Address & Code | | | | | | | | Function |
|--|-----------------------------|----|-----|-----|-----|-----|-----|----|----------------|----|----|-----------|----------|-----------|------------|---|----------|
| | CSB | RS | WRB | RDB | RE2 | RE1 | RE0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| X Address (Lower nibble) [0H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AX3 | AX2 | AX1 | AX0 | Set of X direction Address in display RAM | |
| X Address (Upper nibble) [1H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | AX7 | AX6 | AX5 | AX4 | Set of X direction Address in display RAM | |
| Y Address [2H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | AY3 | AY2 | AY1 | AY0 | Set of Y direction Address in display RAM | |
| n-line alternation (Lower nibble) [3H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | N3 | N2 | N1 | N0 | Set the number of alternate reverse line | |
| n-line alternation (Upper nibble) [4H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | * | N6 | N5 | N4 | Set the number of alternate reverse line | |
| Display control (1) [5H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | SHI FT | * | ALL ON | ON/ OFF | SHIFT: Select common shift direction ALLON All display ON ON/OFF: Display ON/OFF control | |
| Display control (2) [6H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | REV | NLIN | EOR | REF | REV: Display normal/reverse NLIN: n line reverse control EOR: Exclusive OR-ing the AC waveform REF: segment normal/reverse | |
| Increment control [7H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | WIN | AIM | AYI | AXI | WIN: Select window. AIM: Select increment mode AYI: Y increment, AXI: X increment | |
| Power control [8H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | AMP ON | HA LT | DC ON | ACL | AMPON: Internal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting | |
| LCD Duty ratio (Lower nibble) [9H] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | DS3 | DS2 | DS1 | DS0 | Set LCD drive duty ratio | |
| LCD Duty ratio (Upper nibble) [AH] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | DS3 | DS2 | DS1 | DS0 | Set LCD drive duty ratio | |
| Booster [BH] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | * | VU2 | VU1 | VU0 | Set number of boosting step for booster circuit | |
| Bias ratio control [CH] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | B3 | B2 | B1 | B0 | Set bias ratio for LCD driving voltage | |
| Register access control [EH] | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | SC3 | SC2 | SC1 | SC0 | Set common driver start line | |
| Display start common [FH] | 0 | 1 | 0 | 1 | 0/1 | 0/1 | 0/1 | 1 | 1 | 1 | 1 | | RE2 | RE1 | RE0 | RE: set register bank number | |

NOTE: Address for the control register are enclosed in brackets [].

* = Don't Care



8.1.2 Control Register (Bank 1)

| Control Register | Pins (for 80-Family) & Bank | | | | | | | Address & Code | | | | | | | | Function |
|--|-----------------------------|----|-----|-----|-----|-----|-----|----------------|----|----|----|-----|-----|------|------|--|
| | CSB | RS | WRB | RDB | RE2 | RE1 | RE0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Temperature compensation [0H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | * | * | TCS1 | TCS0 | Temperature compensation set |
| Electronic Volume (Low nibble) [1H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | DV3 | DV2 | DV1 | DV0 | Set electronic volume register |
| Electronic Volume (Upper nibble) [2H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | * | DV6 | DV5 | DV4 | |
| Register read control [3H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | RA3 | RA2 | RA1 | RA0 | Set register address for read |
| Set RF [4H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | RF3 | RF2 | RF1 | RF0 | Select RF ratio of OSC circuit |
| Extend Power Control [5H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | BF1 | BF0 | * | DIS | Set booster frequency Discharge V0~V4 capacitors |
| Regulator multiple ratio Control [6H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | * | RM2 | RM1 | RM0 | Set regulator multiple ratio |
| Start address for line reverse (Low nibble) [7H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | LS3 | LS2 | LS1 | LS0 | Set start line for line reverse display |
| Start address for line reverse (Upper nibble) [8H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | LS6 | LS5 | LS4 | |
| End address for line reverse (Low nibble) [9H] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | LE3 | LE2 | LE1 | LE0 | Set end line for line reverse display |
| End address for line reverse (Upper nibble) [AH] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | * | LE6 | LE5 | LE4 | |
| Line reverse [BH] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | * | * | BT | LREV | BT Reverse type select LREV: Line reverse control |
| Window X end address (Low nibble) [CH] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | EX3 | EX2 | EX1 | EX0 | Set X end address for window function access |
| Window X end address (Upper nibble) [DH] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | EX7 | EX6 | EX5 | EX4 | |
| Window Y end Address [EH] | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | EY3 | EY2 | EY1 | EY0 | Set Y end address for window function |
| Register Access Control [FH] | 0 | 1 | 0 | 1 | 0/1 | 0/1 | 0/1 | 1 | 1 | 1 | 1 | * | RE2 | RE1 | RE0 | RE: Set register bank number |

NOTE: Address for the control register are enclosed in brackets [].

* = Don't Care



8.1.3 Control Register (Bank 2)

| Control Register | Pins (for 80-Family) & Bank | | | | | | | Address & Code | | | | | | | Function | |
|---|-----------------------------|----|-----|-----|-----|-----|-----|----------------|----|----|----|------|------|------|----------|-------------------------------|
| | CSB | RS | WRB | RDB | RE2 | RE1 | RE0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | D0 |
| EEPROM mode select [0H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | * | M1 | M0 | VPP_EXT | EEPROM mode select |
| Vop calibration offset select (Low nibble) [1H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | CV3 | CV2 | CV1 | CV0 | Vop calibration offset select |
| Vop calibration offset select (Upper nibble) [2H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | * | * | CV5 | CV4 | |
| EEPROM address select [5H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | * | * | NIB1 | NIB0 | Select EEPROM address |
| Scroll top address (Low nibble) [6H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | STA3 | STA2 | STA1 | STA0 | Set scroll top address |
| Scroll top address (Upper nibble) [7H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | * | STA6 | STA5 | STA4 | |
| Scroll bottom address (Low nibble) [8H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | SBA3 | SBA2 | SBA1 | SBA0 | Set scroll bottom address |
| Scroll bottom address (Upper nibble) [9H] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | * | SBA6 | SBA5 | SBA4 | |
| Scroll specified address (Low nibble) [AH] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | SSA3 | SSA2 | SSA1 | SSA0 | Set scroll specified address |
| Scroll specified address (Upper nibble) [BH] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | * | SSA6 | SSA5 | SSA4 | |
| Scroll start address (Low nibble) [CH] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | SAY3 | SAY2 | SAY1 | SAY0 | Set scroll start address |
| Scroll start address (Upper nibble) [DH] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | * | SAY6 | SAY5 | SAY4 | |
| Scroll mode select [EH] | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | * | * | SM1 | SM0 | Scroll mode select |
| Register Access Control [FH] | 0 | 1 | 0 | 1 | 0/1 | 0/1 | 0/1 | 1 | 1 | 1 | 1 | * | RE2 | RE1 | RE0 | RE: set register bank number |

NOTE: Address for the control register are enclosed in brackets [].

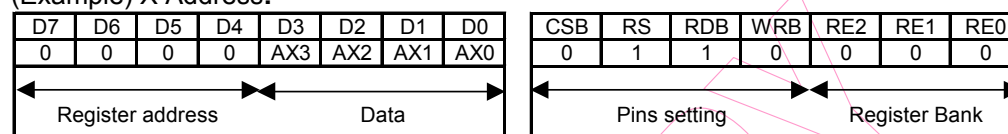
* = Don't Care



8.2 Functions of the Control Registers

The EM65101 has many control registers. When accessing the control registers, the upper nibble of the data bus (D7~D4) represent the register address while the lower nibble of the data bus (D3~D0) represent data. The following figure shows an access example. The Pins CSB, RS, RDB, & WRB) settings are for the 80-family MPU interface. Only the setting of the terminals RDB & WRB are different when it is accessed by the 68-family MPU.

(Example) X Address:



When writing to the control register, it is used directly by addressing D7~D4 of the data bus. When reading, you must first set the RA register for the specific register address before you can read specific register. Therefore, a 2-step procedure is required to perform a read register operation. After reading, the specific register will output to D3~D0 of the data bus. All nibbles, except D3~D0, of the data bus are all "H." Access to undefined register address area is prohibited. When RS is "L," all read/write operations are accessed to display RAM. Then the data bus does not include the register address. When writing, D3~D0 data is written to the register designated at D7~D4 on the rising edge of the WRB signal. When reading, the register can output to data bus during RDB active period. The control register and display RAM have equal access sequence

8.2.1 X Address Register (AX)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | AY3 | AX2 | AY1 | AY0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {AX3, AX2, AX1, AX0} = 0H, read address: 0H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | AX7 | AX6 | AX5 | AX4 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {AX7, AX6, AX5, AX4} = 0H, read address: 1H)

The AX register is set to X-direction address of display RAM. In data setting, command is divided into lower and upper sections at 4-bit of data each in order to accommodate the required 8-bit of total data.

8.2.2 Y Address Register (AY)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | AY3 | AX2 | AY1 | AY0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {AY3, AY2, AY1, AY0} = 0H, read address: 2H)

The AY register is set to Y-direction address of display RAM. 00H to 0FH are applicable to the values for AY3 to AY0.



8.2.3 n Line Alternated Register (N)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|----|----|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | N3 | N2 | N1 | N0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {N3, N2, N1, N0}=3H, read address: 3H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|----|----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 0 | 0 | * | N6 | N5 | N4 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {N7, N6, N5, N4}=0H, read address: 4H)

The EM65101 supports not only the LCD reversed AC drive in one-frame unit, but also the n-line reversed AC drive which alternates in an n-line unit from 2 to 128 lines. The reversed AC drive is controlled by the “NLIN” and “EOR” control bits. The values set up by the alternating register become enabled when the NLIN control bit is “1.” When the NLIN control bit is “0,” the alternate drive waveform is generated reserving each frame. When a problem affecting display quality occurs, the n-line reversed AC drive can improve the quality. Determine the number of the n-line reverse for alternating after confirming the display quality with the actual LCD panel.

However, if the number of AC reversed lines are reduced, the LCD alternating frequency becomes high. As a result, the charge or discharge current is increased in the LCD cells.

| N6 | N5 | N4 | N3 | N2 | N1 | N0 | EOR=0 N Line Number | EOR=1 N Line Number |
|----|----|----|----|----|----|----|------------------------|------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | No operation | No operation |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 2 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 3 | 3 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 4 | 4 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 5 | 5 |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 64 | 64 |
| : | : | : | : | : | : | : | : | Prohibited Code |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 100 | |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 101 | |
| : | : | : | : | : | : | : | : | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 128 | |



8.2.4 Display Control Display (1) Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-------|----|--------|--------|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 0 | 1 | SHIFT | * | ALL ON | ON/OFF | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {SHIFT, ALLON, ON/OFF}=0H, read address: 5H)

ON/OFF: Control display ON/OFF

ON/OFF = "0": Display OFF

ON/OFF = "1": Display ON

ALLON: Regardless of the data for display, all is ON.

This control has priority over display normal/reverse commands.

ALLON = "0": Normal display

ALLON = "1": All display lighted

SHIFT

The shift direction of display scanning data in the common driver output is selected.

SHIFT = "0": COM0→COM127 shift-scan

SHIFT = "1": COM127→COM0 shift-scan

8.2.5 Display Control (2) Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|------|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | REV | NLIN | EOR | REF | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {REV, NLIN, EOR, REF} = 0H, read address: 6H)

REV: To the corresponding display RAM data, the lighting or non-lighting control of the display is set.

REV = "0": When RAM data is "H," and LCD at ON voltage (normal)

REV = "1": When RAM data is "L," and LCD at ON voltage (reverse)

NLIN: The n-line alternate drive NLIN control.

NLIN = "0": n-line alternate drive is OFF. In each frame, the alternate signals (M) are reversed.

NLIN = "1": n-line alternated drive is ON. Depending on data set up in the n-line alternated register, alternation is made.

EOR: The n-line alternate drive EOR control.

EOR=0: M always reverses at the nth raster row regardless of whether the end of a frame is reached.

EOR=1: M reverses at the nth raster row and restarts the raster row count at the start of every frame.

REF: When MPU accesses display RAM, address X and data are switched. The following figure shows the action of the REF.

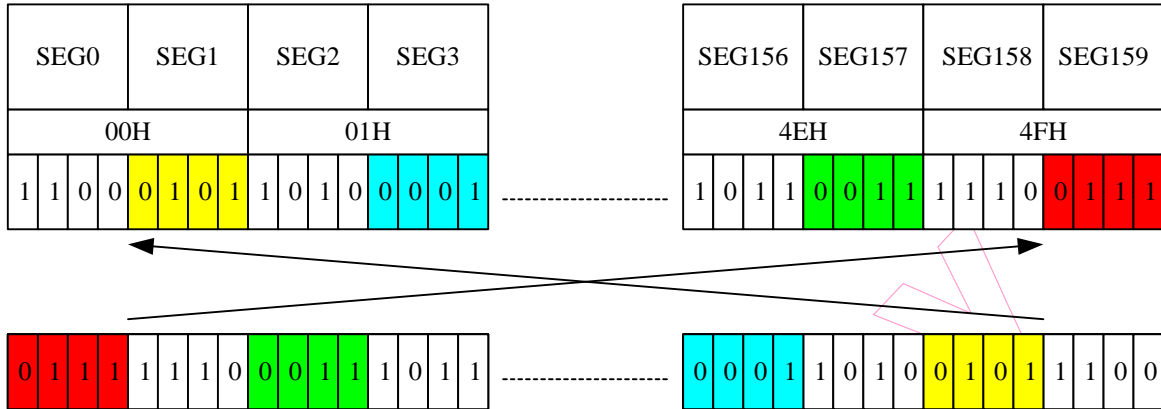


Figure 8-1 REF Register Function

8.2.6 Increment Control Register Set

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 1 | WIN | AIM | AYI | AXI | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {WIN, AIM, AYI, AXI} = 0H, read address: 7H)

This register controls the increment mode and the window function when accessing display RAM. The increment operation of the AXI and AYI registers are controlled by the settings at the AIM, AYI, and AXI registers, and every write or read access to display RAM. The AYI register directly connects to display RAM as Y address. The AXI register connects to the address converter, and then outputs to display RAM as X address in auto increment mode. The AXI and AYI registers are incremented, but do not directly increment the X and Y addresses.

When setting this control register, the address increment operation can be made without setting successive addresses for writing or reading data to display RAM from MPU.

The WIN register is used for window function control.

- WIN="0": Normal RAM access
- WIN="1": Window function access

When using the window function to access RAM, be sure to set the following register first.

WIN="1," AXI="1," AYI="1"

X Address, Y Address, Window X End Address, Window Y End Address

In addition, the following condition must be met.

- Window end X address Window start X address
- Window end Y address Window start Y address



The increment control of X and Y addresses by AIM, AYI, and AXI registers are listed as follows.

| AIM | Address Increment Timing |
|-----|---|
| 0 | When writing to Display RAM or reading from Display RAM This is effective when accessing successive address area |
| 1 | Only when writing to Display RAM This is effective in the case of "Read Modify Write" |

Sequence for Read Modify Write

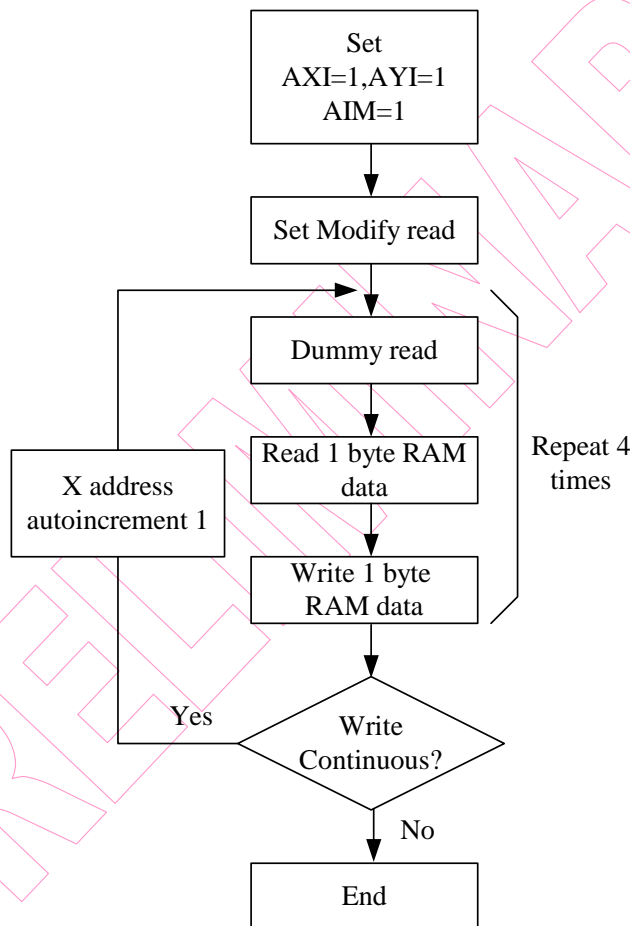


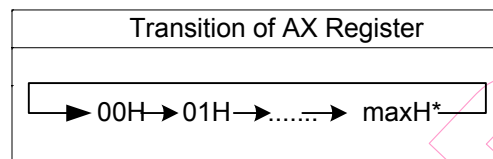
Figure 8-2 Read Modify Write Flow Chart



| AYI | AXI | Select Address Increment Operation | Remark |
|-----|-----|------------------------------------|--------|
| 0 | 0 | Address is not incremented | *1 |
| 0 | 1 | X-Address is incremented | *2 |
| 1 | 0 | Y-Address is incremented | *3 |
| 1 | 1 | X and Y both are incremented | *4 |

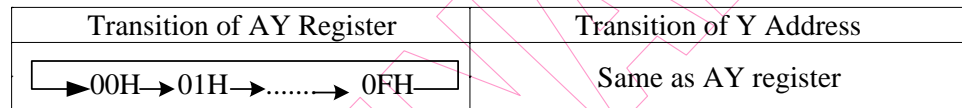
*1 Regardless of AIM, no increment for the AX and AY registers.

*2 Depending on the setting of AIM, address X automatically changes.

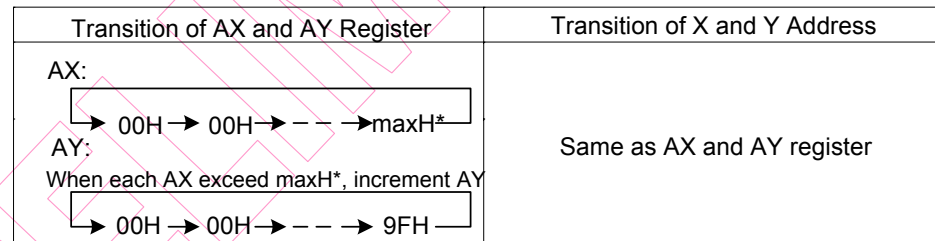


*maxH: The maximum internal X-address value in each access mode

*3 Depending on the setting of AIM, address Y automatically changes.



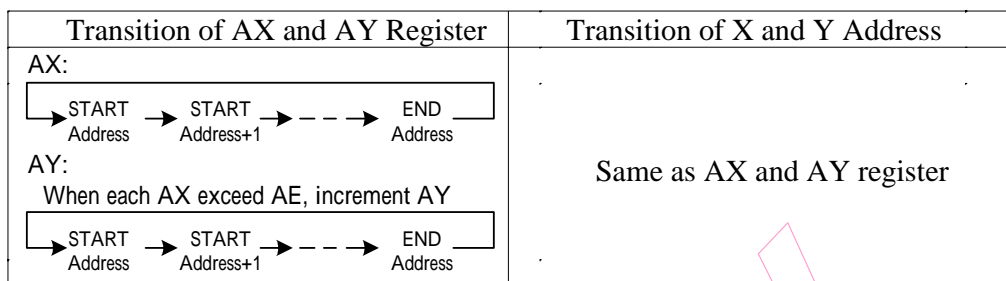
*4 Depending on the setting of AIM, addresses X and Y also change. When the X address exceeds maxH, Y address is incremented.



*maxH: The maximum internal X-address value in each access mode



The following shows how address is incremented when using the window function.



In each operation mode, the following increment operation is performed:

When gradation display mode and 8-bit access are selected

Address is incremented as described above.

8.2.7 Power Control Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-------|------|------|-----|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 0 | AMPON | HALT | DCON | ACL | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {AMPON, HALT, DCON, ACL} = 0H, read address: 8H)

AMPON: This command sets the internal OP-AMP circuit block (voltage regulator, electronic volume, and voltage conversion circuit) ON or OFF.

AMPON = "0": The internal OP-AMP circuit is OFF

AMPON = "1": The internal OP-AMP circuit is ON

HALT: This command sets power saving ON or OFF.

HALT = "0": Normal operation

HALT="1": Power-saving operation

When power-saving is ON, the consumed current can be reduced to a value near to the standby current.

The internal condition at power saving are as follows.

- (1) The oscillating circuit and the power supply circuit are OFF.
- (2) The LCD drive is OFF, and the output of the segment driver and common driver is at the VSS level.
- (3) The clock input from the CK pin is prohibited.
- (4) The contents of Display RAM data are stored.
- (5) The operational mode stores the state of command executed before the power saving command is performed.



DCON: This command sets the internal booster circuit ON or OFF.

DCON = "0": Booster circuit OFF

DCON="1": Booster circuit ON

ACL: This command initializes the internal circuit.

ACL = "0": Normal operation

ACL = "1": Initialization ON

When the reset operation begins internally after the ACL register is set to "1," the ACL register is automatically cleared to "0." The internal reset signal is generated with a clock (built-in oscillation circuit or CK input) for display. Therefore, set the WAIT period to at least two display clock cycles. After the WAIT period, the subsequent operation is then executed.

8.2.8 LCD Duty (DS)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 1 | 0 | 0 | 1 | DS3 | DS2 | DS1 | DS0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {DS3, DS2, DS1, DS0} = 0H, read address: 9H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 1 | 0 | 1 | 0 | DS7 | DS6 | DS5 | DS4 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {DS7, DS6, DS5, DS4} = 8H, read address: AH)

The DS register set to LCD display duty.

| DS7 | DS6 | DS5 | DS4 | DS3 | DS2 | DS1 | DS0 | Selectable Duty ratio |
|-----|-----|-----|-----|-----|-----|-----|-----|-----------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No operation |
| : | : | : | : | : | : | : | : | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1/8 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1/9 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | : |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1/100 |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1/127 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1/128 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | No operation |
| : | : | : | : | : | : | : | : | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

Partial display can be made possible by setting an arbitrary duty ratio.



8.2.9 Booster Setup (VU)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 1 | 1 | * | VU2 | VU1 | VU0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {VU2, VU1, VU0} = 5H, read address: BH)

The booster steps are set to the VU register

| VU2 | VU1 | VU0 | Booster Operation |
|-----|-----|-----|--------------------------------|
| 0 | 0 | 0 | Booster disable (No operation) |
| 0 | 0 | 1 | 2 times voltage output |
| 0 | 1 | 0 | 3 times voltage output |
| 0 | 1 | 1 | 4 times voltage output |
| 1 | 0 | 0 | 5 times voltage output |
| 1 | 0 | 1 | 6 times voltage output |
| 1 | 1 | 0 | Prohibited code |
| 1 | 1 | 1 | |

8.2.10 Bias Setting Register (B)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|----|----|-----|----|-----|-----|-----|-----|-----|
| 1 | 1 | 0 | 0 | B3 | B2 | B1 | B0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {B3, B2, B1, B0} = 8H, read address: CH)

This register is used to set a bias ratio. A bias ratio can be selected from 1/4 to 1/13 through B3, B2, B1, and B0 set up.

| B3 | B2 | B1 | B0 | Bias |
|----|----|----|----|-----------------|
| 0 | 0 | 0 | 0 | 1/4 Bias |
| 0 | 0 | 0 | 1 | 1/5 Bias |
| 0 | 0 | 1 | 0 | 1/6 Bias |
| 0 | 0 | 1 | 1 | 1/7 Bias |
| 0 | 1 | 0 | 0 | 1/8 Bias |
| 0 | 1 | 0 | 1 | 1/9 Bias |
| 0 | 1 | 1 | 0 | 1/10 Bias |
| 0 | 1 | 1 | 1 | 1/11 Bias |
| 1 | 0 | 0 | 0 | 1/12 Bias |
| 1 | 0 | 0 | 1 | 1/13 Bias |
| 1 | 0 | 1 | 0 | Prohibited code |
| : | : | : | : | |
| 1 | 1 | 1 | 1 | |

NOTE

When setting bias=1/4 and 1/5, V4 must be less than the VDD voltage



8.2.11 Display Start Common

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 1 | 1 | 1 | 0 | SC3 | SC2 | SC1 | SC0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

(At the time of reset: {SC3, SC2, SC1, SC0} = 0H, read address: EH)

The SC register sets the scanning start output of the common driver.

| SC3 | SC2 | SC1 | SC0 | Display Starting Common | |
|-----|-----|-----|-----|-------------------------|--------------|
| | | | | When SHIFT=0 | When SHIFT=1 |
| 0 | 0 | 0 | 0 | COM0 | COM127 |
| 0 | 0 | 0 | 1 | COM8 | COM119 |
| 0 | 0 | 1 | 0 | COM16 | COM111 |
| 0 | 0 | 1 | 1 | COM24 | COM103 |
| 0 | 1 | 0 | 0 | COM32 | COM95 |
| 0 | 1 | 0 | 1 | COM40 | COM87 |
| 0 | 1 | 1 | 0 | COM48 | COM79 |
| 0 | 1 | 1 | 1 | COM56 | COM71 |
| 1 | 0 | 0 | 0 | COM64 | COM63 |
| 1 | 0 | 0 | 1 | COM72 | COM55 |
| 1 | 0 | 1 | 0 | COM80 | COM47 |
| 1 | 0 | 1 | 1 | COM88 | COM39 |
| 1 | 1 | 0 | 0 | COM96 | COM31 |
| 1 | 1 | 0 | 1 | COM104 | COM23 |
| 1 | 1 | 1 | 0 | COM112 | COM15 |
| 1 | 1 | 1 | 1 | COM120 | COM7 |

8.2.12 Temperature Compensation Set

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|------|------|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | * | * | TCS1 | TCS0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: { TCS1, TCS0 } = 0H, read address: 0H)

| TCS1 | TCS0 | Temperature Compensation Slope |
|------|------|--------------------------------|
| 0 | 0 | -0.05% per °C |
| 0 | 1 | -0.1% per °C |
| 1 | 0 | -0.15% per °C |
| 1 | 1 | -0.2% per °C |

$V_{REF}(T)$ (Temperature compensation output voltage) is controlled by TCS1, TCS0 and the previous environment temperature T.

$$V_{REF}(T) = V_{REF0} [(1 + TCS(T - 25^{\circ}C))]$$

- TCS is selected by TCS1 and TCS0
- $V_{REF0} = 1.5V$ at $25^{\circ}C$

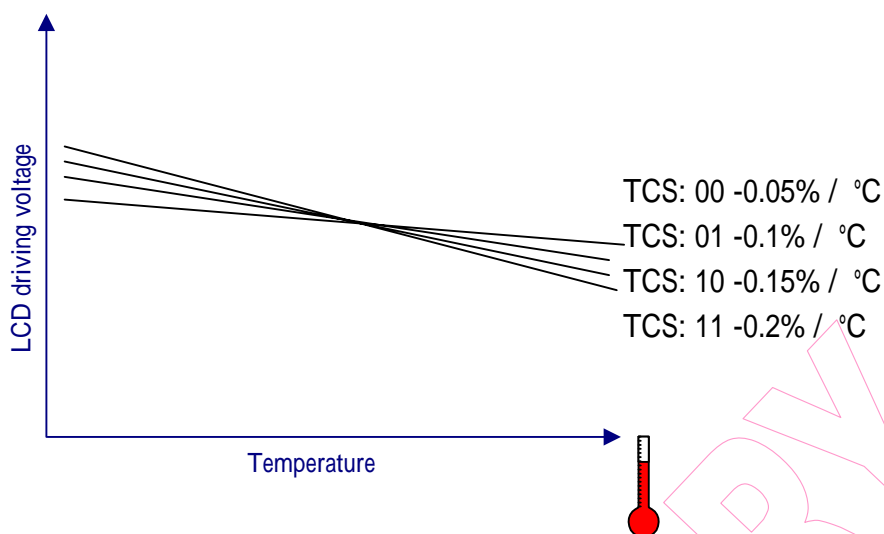


Figure 8-3 Temperature Compensation Slope

8.2.13 Electronic Volume Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | DV3 | DV2 | DV1 | DV0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: { DV3~DV0 } = 0H, read address: 1H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | * | DV6 | DV5 | DV4 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: { DV6~DV4 } = 0H, read address: 2H)

The DV register controls the VBA voltage. This 7-bit register provides up to 65 levels of voltage selections.

| DV6 | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 | Output Voltage |
|-----|-----|-----|-----|-----|-----|-----|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Prohibit code |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| : | : | : | : | : | : | : | |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 32 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| : | : | : | : | : | : | : | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 96 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | |
| : | : | : | : | : | : | : | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | Prohibited code |

$$VBA = (1 + (M + \text{offset}) / 381) * VREF$$

$$V0 = VBA * N$$

M : DV register setting ; offset : CV0~CV5 set on EEPROM function

N : RM register setting

VREF : internal temperature compensation output voltage

In order to prevent the transient voltage from generating when an electronic volume code is set, the circuit design is such that the set value is not reflected as a level immediately. The value is reflected after the upper bits(DV6-DV4) of the electronic code have been set. The set value becomes valid when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

NOTE

When writing code to set the electronic volume register, you must set DV6~DV4 first before setting DV3~DV0.

8.2.14 Internal Register Read Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | RA3 | RA2 | RA1 | RA0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {RA3, RA2, RA1, RA0} = 7H, read address: 3H)

The RA register specifies the address for register read operation. The EM65101 has many registers and one register bank. Therefore, the following 4-step procedure is required to read the specific register.

- (1) Write 01H to the RE register for accessing the RA register
- (2) Writes the specific register address to the RA register
- (3) Write the specific register bank to the RE register
- (4) Read specific contents

8.2.15 Resistance Ratio of the CR Oscillator

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 0 | 1 | RF3 | RF2 | RF1 | RF0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {RF3, RF2, RF1, RF0} = 0H, read address: 8H)

The RF registers can control the resistance ratio of the CR oscillator. Therefore the frame frequency can change the settings at the RF registers.

When changing the RF registers, make sure to check the LCD display quality.

| RF3 | RF2 | RF1 | RF0 | Operation |
|-----|-----|-----|-----|--|
| 0 | 0 | 0 | 0 | Initial Resistance Ratio |
| 0 | 0 | 0 | 1 | 0.52 times of initial Resistance Ratio |
| 0 | 0 | 1 | 0 | 0.60 times of initial Resistance Ratio |
| 0 | 0 | 1 | 1 | 0.68 times of initial Resistance Ratio |
| 0 | 1 | 0 | 0 | 0.74 times of initial Resistance Ratio |
| 0 | 1 | 0 | 1 | 0.80 times of initial Resistance Ratio |
| 0 | 1 | 1 | 0 | 0.88 times of initial Resistance Ratio |
| 0 | 1 | 1 | 1 | 0.94 times of initial Resistance Ratio |
| 1 | 0 | 0 | 0 | 1.06 times of initial Resistance Ratio |
| 1 | 0 | 0 | 1 | 1.12 times of initial Resistance Ratio |
| 1 | 0 | 1 | 0 | 1.20 times of initial Resistance Ratio |
| 1 | 0 | 1 | 1 | 1.28 times of initial Resistance Ratio |
| 1 | 1 | 0 | 0 | 1.36 times of initial Resistance Ratio |
| 1 | 1 | 0 | 1 | 1.44 times of initial Resistance Ratio |
| 1 | 1 | 1 | 0 | 1.52 times of initial Resistance Ratio |
| 1 | 1 | 1 | 1 | 1.60 times of initial Resistance Ratio |



8.2.16 Extended Power Control

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 0 | 1 | BF1 | BF0 | * | DIS | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: {BF1, BF0, DIS} = 0H; read address: 5H)

DIS: is the register that controls the capacitors (connected between the power supply V0-V4 for the LCD drive voltage and VSS) voltage discharged to VSS.

DIS = "0": Disable

DIS = "1": Enable

BF1~BF0: The operating frequency in the booster is selected. When the boosting frequency is high, the driving ability of the booster become high, but the current consumption is increased. You must take the external capacitors and the current consumption into consideration when adjusting the boosting frequency.

| BF1 | BF0 | Operating Clock Frequency in the Booster |
|-----|-----|--|
| 0 | 0 | 3K Hz * 8 |
| 0 | 1 | 3K Hz * 4 |
| 1 | 0 | 3K Hz * 2 |
| 1 | 1 | 3 K Hz |

8.2.17 Regulator Multiple Ratio Control

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | * | RM2 | RM1 | RM0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: {RM2, RM1, RM0} = 6H, read address: 6H)

The V0 modified range setting for RM register

| RM2 | RM1 | RM0 | Regulator Multiple Ratio Control |
|-----|-----|-----|----------------------------------|
| 0 | 0 | 0 | 3.0 times voltage output |
| 0 | 0 | 1 | 4.0 times voltage output |
| 0 | 1 | 0 | 5.0 times voltage output |
| 0 | 1 | 1 | 6.5 times voltage output |
| 1 | 0 | 0 | 8.0 times voltage output |
| 1 | 0 | 1 | 8.5 times voltage output |
| 1 | 1 | 0 | 8.9 times voltage output |
| 1 | 1 | 1 | Prohibited code |

Vref=1.5V, V0 modified range is shown in the following figure:

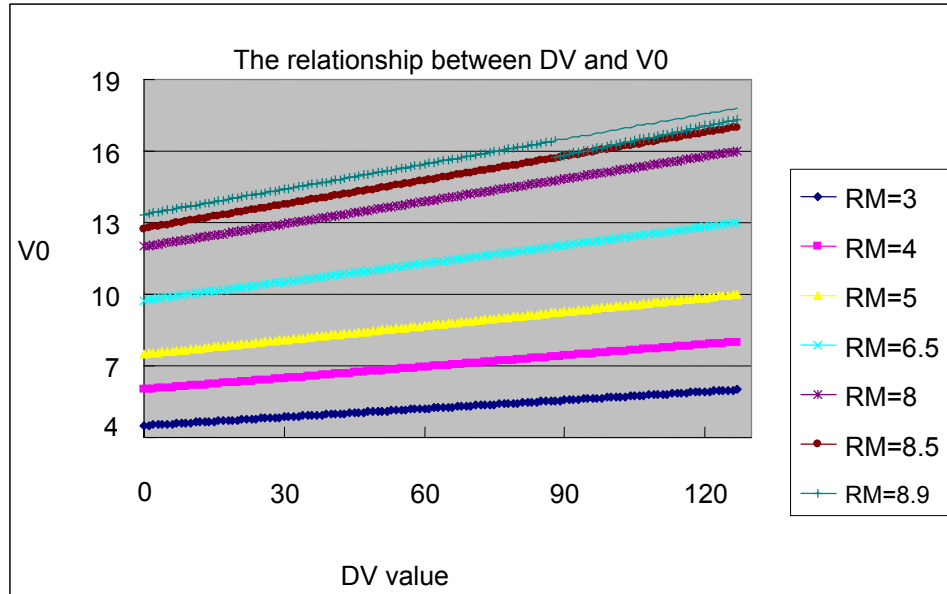


Figure 8-4 V0 Modified Range

8.2.18 Line Reverse Start Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 1 | LS3 | LS2 | LS1 | LS0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {LS3, LS2, LS1, LS0} = 0H, read address: 7H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 0 | * | LS6 | LS5 | LS4 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: {LS6, LS5, LS4} = 0H, read address: 8H)

When setting the line reverse range, the panel on the defined range will be reversed.

NOTE
The RAM data is not changed.

| LS6 | LS5 | LS4 | LS3 | LS2 | LS1 | LS0 | Start Common Number |
|-----|-----|-----|-----|-----|-----|-----|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | COM0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | COM1 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | COM126 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | COM127 |



8.2.19 Line Reverse End Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 1 | LE3 | LE2 | LE1 | LE0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {LE3, LE2, LE1, LE0} = 0H, read address: 9H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 1 | 0 | * | LE6 | LE5 | LE4 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: {LE6, LE5, LE4} = 0H, read address: AH)

The LE registers sets the line reverse end address.

| LE6 | LE5 | LE4 | LE3 | LE2 | LE1 | LE0 | End Common Number |
|-----|-----|-----|-----|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | COM0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | COM1 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | COM126 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | COM127 |

8.2.20 Line Reverse Control

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|----|------|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 1 | 1 | * | * | BT | LREV | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

* = Don't Care

(At the time of reset: {BT, LREV} = 0H, read address: BH)

LREV: is the register that sets the line reverse display function.

LREV = "0": Normal display (Not reverse).

LREV = "1": Line reverse display enable.

The area specified by the Line Reverse Start/End register reverses the display.

BT: is the register that selects the reverse type.

When using the Line Reverse Display function, the LS and LE registers must meet the following condition.

LS LE

The BT register control line reverse type is an option of the line reverse display function. This BTs setting is only available when LREV="1"

BT = "0": Reverse display

BT = "1": Reverse display at each 32 frame.

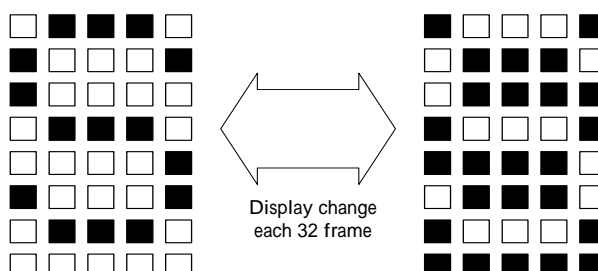


Figure 8-5 Blink Example (LREV="1," BT="1")



8.2.21 Window End X Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 1 | 1 | 0 | 0 | EX3 | EX2 | EX1 | EX0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {EX3, EX2, EX1, EX0} = 1H, read address: CH)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 1 | 1 | 0 | 1 | EX7 | EX6 | EX5 | EX4 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {EX7, EX6, EX5, EX4} = 0H, read address: DH)

The EX registers set the X direction end address of the window function.

| EX7 | EX6 | EX5 | EX4 | EX3 | EX2 | EX1 | EX0 | Window Column Address |
|-----|-----|-----|-----|-----|-----|-----|-----|-----------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Prohibited Code |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 126 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |
| : | : | : | : | : | : | : | : | : |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 158 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 159 |

8.2.22 Window End Y Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|-----|-----|-----|-----|
| 1 | 1 | 1 | 0 | EY3 | EY2 | EY1 | EY0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |

(At the time of reset: {EY3, EY2, EY1, EY0} = 0H, read address: EH)

The EY registers set the Y direction end address of the window function.

| EY3 | EY2 | EY1 | EY0 | Window Y Address |
|-----|-----|-----|-----|------------------|
| 0 | 0 | 0 | 0 | COM7 |
| 0 | 0 | 0 | 1 | COM15 |
| 0 | 0 | 1 | 0 | COM23 |
| 0 | 0 | 1 | 1 | COM31 |
| 0 | 1 | 0 | 0 | COM39 |
| 0 | 1 | 0 | 1 | COM47 |
| 0 | 1 | 1 | 0 | COM55 |
| 0 | 1 | 1 | 1 | COM63 |
| 1 | 0 | 0 | 0 | COM71 |
| 1 | 0 | 0 | 1 | COM79 |
| 1 | 0 | 1 | 0 | COM87 |
| 1 | 0 | 1 | 1 | COM95 |
| 1 | 1 | 0 | 0 | COM103 |
| 1 | 1 | 0 | 1 | COM111 |
| 1 | 1 | 1 | 0 | COM119 |
| 1 | 1 | 1 | 1 | COM127 |



8.2.23 EEPROM Mode Select Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|----|---------|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | * | M1 | M0 | VPP_EXT | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {M1, M0, VPP_EXT} = 6H, read address: 0H)

The (M1,M0) register controls the EEPROM mode

| (M1,M0) | EEPROM Operating Mode | Delay Time |
|---------|-----------------------|------------|
| 00 | Read | > 10 uS |
| 01 | Program | > 4 mS |
| 10 | Erase | > 4 mS |
| 11 | Reserve | - |

The VPP_EXT register controls the EEPROM power selection.

VPP_EXT=0 → Program or Erase EEPROM voltage from internal power.

VPP_EXT=1 → Program or Erase EEPROM voltage from external power. Forces 17~18V from the VPP pin externally.

8.2.24 Vop Calibration Offset Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|-----|-----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | CV3 | CV2 | CV1 | CV0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

(At the time of reset: {CV3, CV2, CV1, CV0} = 0H, read address: 1H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|-----|-----|-----|----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | * | * | CV5 | CV4 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {CV5, CV4} = 0H, read address: 2H)

The CV5~CV0 registers control the Vop calibration offset voltage selection

$$VBA = (1 + (M + offset) / 381) * VREF$$

M : DV register setting ; **offset** : CV5~CV0 setting

| CV5~CV0 | Calibration Offset |
|---------|--------------------|
| 011111 | +31 |
| 011110 | +30 |
| ... | ... |
| 000001 | +1 |
| 000000 | 0 |
| 100000 | -32 |
| 100001 | -31 |
| ... | ... |
| 111111 | -1 |



8.2.25 EEPROM Address Select Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|----|------|------|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 0 | 1 | * | * | NIB1 | NIB0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {NIB1, NIB0} = 0H, read address: 5H)

The NIB register selects whether to access the low nibble or high nibble data of EEPROM.

| NIB1 | NIB0 | EEPROM Address |
|------|------|----------------------|
| 0 | 0 | Bank 2[1H] (CV3~CV0) |
| 0 | 1 | Bank 2[2H] (CV5~CV4) |

NOTE

- When settings CV5~CV0, you must set CV5~CV4 (upper nibble registers) first, then set CV3~CV0 (lower nibble registers), and then start program execution.
- The programming sequence of CV5~CV4 and CV3~CV0 has no restriction.
- When reading from CV5~CV0, you must read EEPROM data to CV5~CV4 (upper nibble registers) first, then read EEPROM data to CV3~CV0 (lower nibble registers).

8.2.26 Scroll Top Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|------|------|------|------|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | STA3 | STA2 | STA1 | STA0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

(At the time of reset: {STA3, STA2, STA1, STA0} = 0H, read address: 6H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|------|------|------|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 1 | * | STA6 | STA5 | STA4 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {STA6, STA5, STA4} = 0H, read address: 7H)

Set the top address of scroll data area in RAM. $0 \leq \text{Scroll top address} \leq 127$; Scroll top address **must be less than** the Scroll bottom address

| STA6 | STA5 | STA4 | STA3 | STA2 | STA1 | STA0 | Top Common Line |
|------|------|------|------|------|------|------|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | COM0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | COM1 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | COM99 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | COM127 |



8.2.27 Scroll Bottom Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|------|------|------|------|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 0 | SBA3 | SBA2 | SBA1 | SBA0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

(At the time of reset: {SBA3, SBA2, SBA1, SBA0} = FH, read address: 8H)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|------|------|------|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 1 | * | SBA6 | SBA5 | SBA4 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {SBA6, SBA5, SBA4} = 7H, read address: 9H)

Set the bottom address of scroll data area in RAM. $0 \leq \text{Scroll bottom address} \leq 127$;
The Scroll top address **must be less than** the scroll bottom address

| SBA6 | SBA5 | SBA4 | SBA3 | SBA2 | SBA1 | SBA0 | bottom common line Mode0 |
|------|------|------|------|------|------|------|--------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | COM0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | COM1 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | COM99 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | COM127 |

8.2.28 Scroll Specified Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|------|------|------|------|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 1 | 0 | SSA3 | SSA2 | SSA1 | SSA0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

(At the time of reset: {SSA3, SSA2, SSA1, SSA0} = 0H, read address: AH)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|----|----|----|----|----|------|------|------|-----|----|-----|-----|-----|-----|-----|
| 1 | 0 | 1 | 1 | * | SSA6 | SSA5 | SSA4 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {SSA6, SSA5, SSA4} = 0H, read address: BH)

Depending on the display panel size or the duty ratio selection, set the specified address in RAM to jump to the scroll bottom address and display the fixed data area.

Scroll specified address = scroll top address + panel scroll area – 1

| SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSA0 | Specified Common Line Mode0 |
|------|------|------|------|------|------|------|-----------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | COM0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | COM1 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | COM99 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | COM127 |

8.2.29 Scroll Start Address

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|------|------|------|------|
| 1 | 1 | 0 | 0 | SAY3 | SAY2 | SAY1 | SAY0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |

(At the time of reset: {SAY3, SAY2, SAY1, SAY0} = 0H, read address: CH)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|------|------|------|
| 1 | 1 | 0 | 1 | * | SAY6 | SAY5 | SAY4 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {SAY6, SAY5, SAY4} = 0H, read address: DH)

Set the starting address of the area scrolling and then execute the area scrolling operation. The scroll start address must be in the scrolling area.

Scroll top address <= Scroll start address <= Scroll bottom address

NOTE

You must set the scroll start address registers in the sequence: SAY[6:4] (Bank 2[DH]) first, then SAY[3:0] (Bank 2[CH]), to avoid any error.

8.2.30 Scroll Mode Select

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|-----|-----|
| 1 | 1 | 1 | 0 | * | * | SM1 | SM0 |

| CSB | RS | RDB | WRB | RE2 | RE1 | RE0 |
|-----|----|-----|-----|-----|-----|-----|
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |

* = Don't Care

(At the time of reset: {SM1, SM0} = 0H, read address: EH)

| SM1 | SM0 | Type of Area Scroll |
|-----|-----|----------------------|
| 0 | 0 | Center screen scroll |
| 0 | 1 | Top screen scroll |
| 1 | 0 | Bottom screen scroll |
| 1 | 1 | Whole screen scroll |

9 Absolute Maximum Ratings

Absolute maximum ratings

| Item | Symbol | Condition | Pin Used | Rating | Unit |
|---------------------|----------------------------|-----------|----------------------------|------------------------------|------------|
| Supply voltage (1) | V _{DD} | Ta=25 | V _{DD} | -0.3 ~ + 4.0 | V |
| Supply voltage (2) | V _{EE} | | V _{EE} | -0.3 ~ + 4.0 | V |
| Supply voltage (3) | V _{OUT} | | V _{OUT} | -0.3 ~ + 19 | V |
| Supply voltage (4) | V ₀ | | V ₀ | -0.3 ~ + 18.5 | V |
| Supply voltage (5) | V _{1, V2, V3, V4} | | V _{1, V2, V3, V4} | -0.3 ~ V ₀ + 0.3 | V |
| Input voltage | V _I | | *1 | -0.3 ~ V _{DD} + 0.3 | V |
| Storage temperature | T _{stg} | | | | -45 ~ +125 |



9.1 Recommended Operating Conditions

| Item | Symbol | Pin | Min. | Typ. | Max. | Unit | Remarks |
|-----------------------|------------------|------------------|------|------|------|------|---------|
| Supply voltage | V _{DD1} | V _{DD} | 2.2 | | 3.3 | V | *1 |
| | V _{DD2} | V _{DD} | 2.4 | | 3.3 | V | *2 |
| | V _{EE} | V _{EE} | 2.4 | | 3.3 | V | *3 |
| Operating voltage | V ₀ | V ₀ | 4.5 | | 18.5 | V | *4 |
| | V _{OUT} | V _{OUT} | | | 19 | V | |
| | V _{REF} | V _{REF} | | 1.5 | | V | *5 |
| Operating temperature | Topr | | -30 | | 85 | | |

- * 1 Power supply for the logic circuit.
- * 2 Power supply for the analog circuit.
- * 3 Power supply for the internal boosting circuit. If applied the same voltage as V_{DD}, connect to V_{DD}.
- * 4 Voltage V₀>V₁>V₂>V₃>V₄>V_{SS} must always be satisfied.
- * 5 Voltage V_{OUT} > V₀ must always be satisfied.

10 DC Characteristics

VSS=0V , VDD = 2.2 ~3.3V , Ta = -30 ~85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|--|------------------|--|--------|--------|--------|------|----------|
| High level input voltage | V _{IH} | | 0.8VDD | 0.9VDD | VDD | V | *1 |
| Low level input voltage | V _{IL} | | 0 | 0.1VDD | 0.2VDD | V | *1 |
| High level output current | I _{OH1} | VOH = VDD-0.4V | -2.7 | -3.2 | -3.5 | mA | *2 |
| Low level output current | I _{OL1} | VOL = 0.4V | 2.7 | 3.2 | 3.5 | mA | *2 |
| High level output current | I _{OH2} | VOH = VDD-0.4V | -0.8 | -1.0 | -1.2 | mA | *3 |
| Low level output current | I _{OL2} | VOL = 0.4V | 0.8 | 1.0 | 1.2 | mA | *3 |
| Input leakage current | I _{LI1} | VI = VSS or VDD | -2 | 0 | 2 | μA | *4 |
| Output leakage current | I _{LO} | VI = VSS or VDD | -2 | 0 | 2 | μA | *5 |
| LCD driver output resistance | RON | Δ Von = 0.5V V0=10V | 1.0 | 1.3 | 1.6 | KΩ | *6 |
| | | V0=6V | 1.2 | 1.7 | 2.2 | | |
| Standby current through VDD pin | I _{STB} | CK=0, CSB=VDD, Ta=25 , VDD=3V | | 5 | 15 | μA | *7 |
| Oscillator frequency (16 gradation mode) | Fosc | VDD=3V, Ta=25 , Rf setting = (Rf2,Rf1,Rf0)=(000) | 330 | 340 | 350 | KHz | *8 |



| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|------------------------------------|--------|---|-------------|-------------|-------------|------|----------|
| Booster output voltage on VOUT pin | VOUT1 | Six times boosting RL = 500KΩ (VOUT-VSS) | 6*VEE *0.95 | 6*VEE *0.98 | 6*VEE *0.99 | V | *9 |
| | VOUT2 | Five times boosting RL = 500KΩ (VOUT-VSS) | 5*VEE *0.95 | 5*VEE *0.98 | 5*VEE *0.99 | V | *10 |
| | VOUT3 | Four times boosting RL = 500KΩ (VOUT-VSS) | 4*VEE *0.95 | 4*VEE *0.98 | 4*VEE *0.99 | V | *11 |
| | VOUT4 | Three times boosting RL = 500KΩ (VOUT-VSS) | 3*VEE *0.95 | 3*VEE *0.98 | 3*VEE *0.99 | V | *12 |
| | VOUT5 | Two times boosting RL = 500KΩ(VOUT-VSS) | 2*VEE *0.95 | 2*VEE *0.98 | 2*VEE *0.99 | V | *13 |
| Current consumption | IDD1 | VDD = 3V, 6 times booster All ON pattern | | 270 | | μA | *14 |
| | IDD2 | VDD = 3V, 6 times booster Checker pattern | | 380 | | μA | *15 |
| VBA output voltage | VBA | VDD =2.4V~3.3V | 1.5 | | 2.0 | V | *16 |
| VREF output voltage | VREF | VDD = 2.4 ~ 3.3V | | 1.5 | | V | *17 |
| V0 output voltage | V0 | VDD = 2.4 ~ 3.3V | 0.99*V0 | V0 | 1.01*V0 | V | - |

- *1 D0-D7, CSB, RS, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins
- *2 D0~D7 pins
- *3 CLK pins
- *4 CSB, RS, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins
- *5 Applied when D0~D7 are in high impedance state
- *6 SEG0~SEGA159, COM0~COM127 pins Resistance when applied 0.5V between each output pin and each power supply (V0, V1, V2, V3, V4) and when applied 1/12 bias
- *7 VDD pin, VDD pin current without loading when the internal oscillating clock stops and CSB=VDD
- *8 Oscillating frequency when the built-in oscillating circuit (16 gray scale level display mode) is used
- *9 VOUT pin. When the built-in oscillating circuit, the built-in power supply, and the voltage (boosted 6 times) are used, this pin is applied. When VEE = 2.4 ~ 3.3V, the electronic control is set to code ("1 1 1 1 1 1").
Measuring conditions: bias=1/4~1/13, 1/128 duty, without loading. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," BF="11"
- *10 VOUT pin. When the built-in oscillating circuit, the built-in power supply, and the voltage (boosted 5 times) are used, this pin is applied. When VEE = 2.4 ~ 3.3V, the electronic control is set to code ("1 1 1 1 1 1").
Measuring conditions: bias=1/4~1/13, 1/128 duty, without loading. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," BF="11"
- *11 VOUT pin. When the built-in oscillating circuit, the built-in power supply, and the voltage (boosted 4 times) are used, this pin is applied. When VEE = 2.4 ~ 3.3V, the electronic control is set to code ("1 1 1 1 1 1").
Measuring conditions: bias=1/4~1/13, 1/128 duty, without loading. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," BF="11"



- *12 VOUT pin. When the built-in oscillating circuit, the built-in power supply, and the voltage (boosted 3 times) are used, this pin is applied. When VEE = 2.4 ~ 3.3V, the electronic control is set to code ("1 1 1 1 1 1").
 Measuring conditions: bias=1/4~1/13, 1/128 duty, without loading. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," BF="11"
- *13 VOUT pin. When the built-in oscillating circuit, the built-in power supply, and the voltage (boosted 2 times) are used, this pin is applied. When VEE = 2.4 ~ 3.3V, the electronic control is set to code ("1 1 1 1 1 1").
 Measuring conditions: bias=1/4~1/13, 1/128 duty, without loading. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," BF="11"
- *14 VDD, VEE pin. When the built-in oscillating circuit and the built-in power supply are used and there is no access from MPU, this pin is applied. Display ALL ON pattern {Rf3, Rf2, Rf1, Rf0 = ("0 0 0 0")} and the LCD driver pin has no loading. Measuring conditions: VDD=VEE=3V, V0=15V, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," NLIN="0," 1/128 duty, 1/12 bias
- *15 VDD, VEE pin. When the built-in oscillating circuit and the built-in power supply are used and there is no access from MPU, this pin is applied. Voltage which is boosted 6 times is used and the electronic control is set to code. Display a checkered pattern, {Rf3, Rf2, Rf1, Rf0 = ("0 0 0 0")} and the LCD driver pin has no loading. Measuring conditions: VDD=VEE=3V, V0=15V, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON="1," NLIN="0," 1/128 duty, 1/12 bias
- *16 VBA pin. Measuring conditions: N times boosting (N=2~6), electronic control = "1 1 1 1 1 1," display a checkered pattern, DCON=AMPON="1," NLIN="0," 1/128 duty, VDD=VEE, C1=C2=1.0μF, C3=0.1μF, no loading
- *17 VREF pin. Measuring conditions: VDD = 3 volt, N times boosting (N=2 ~ 6), electronic control = "1 1 1 1 1 1," DCON=AMPON="1," NLIN="0," 1/128 duty.

The relationship of oscillating frequency (fosc) and external clock frequency (fCK) with LCD frame frequency (fFLM) in each display mode is shown below:

| Original Oscillating Clock | Display Mode | Ratio of Display Duty Cycle (1/D) | | | | |
|--|-----------------------------|-----------------------------------|-----------------|-----------------|------------------|------------------|
| | | 1/128 to 1/89 | 1/88 to 1/44 | 1/43 to 1/22 | 1/21 to 1/11 | 1/10~1/8 |
| When using the built-in oscillating circuit (fosc) | Simple 16 gray scale levels | $fosc/(2*16*D)$ | $fosc/(4*16*D)$ | $fosc/(8*16*D)$ | $fosc/(16*16*D)$ | $fosc/(32*16*D)$ |
| When using the external clock from CK pin (fCK) | Simple 16 gray scale levels | $fCK/(2*16*D)$ | $fCK/(4*16*D)$ | $fCK/(8*16*D)$ | $fCK/(16*16*D)$ | $fCK/(32*16*D)$ |

11 AC Characteristic

NOTE

All the timings must be specified relative to 20% and 80% of the VDD voltage.

11.1 80-Family MCU Write Timing

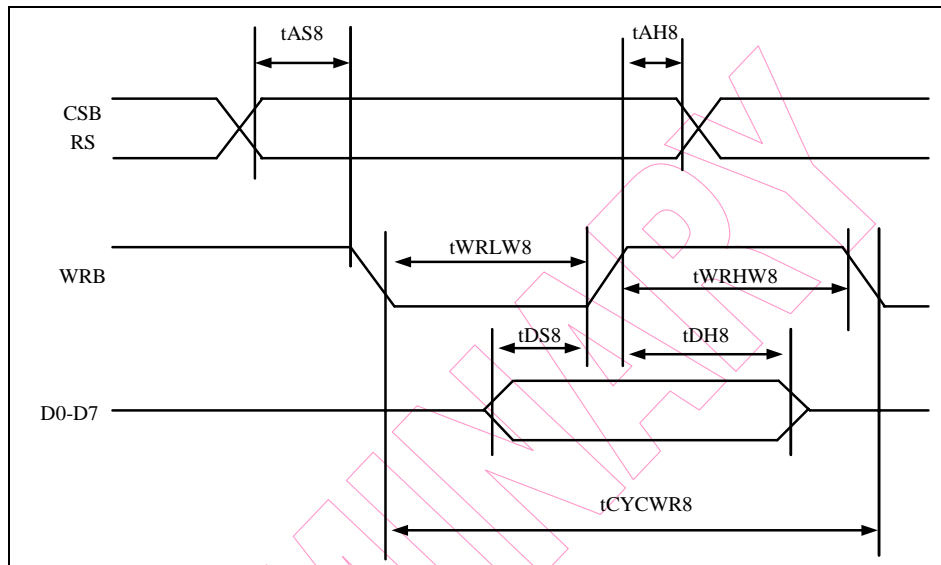


Figure 11-1 80-Family MCU Write Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|----------------------------|---------|-----------|------|------|------|------|---------------|
| Address hold time | tAH8 | | 0 | | | ns | CSB RS |
| Address setup time | tAS8 | | 0 | | | ns | |
| System cycle time in write | tCYCWR8 | | 200 | | | ns | WRB (R/WB) |
| Write pulse "L" width | tWRLW8 | | 30 | | | ns | |
| Write pulse "H" width | tWRHW8 | | 135 | | | ns | |
| Data setup time | tDS8 | | 60 | | | ns | D0~D7 |
| Data hold time | tDH8 | | 5 | | | ns | |

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|----------------------------|---------|-----------|------|------|------|------|---------------|
| Address hold time | tAH8 | | 0 | | | ns | CSB RS |
| Address setup time | tAS8 | | 0 | | | ns | |
| System cycle time in write | tCYCWR8 | | 250 | | | ns | WRB (R/WB) |
| Write pulse "L" width | tWRLW8 | | 50 | | | ns | |
| Write pulse "H" width | tWRHW8 | | 160 | | | ns | |
| Data setup time | tDS8 | | 80 | | | ns | D0~D7 |
| Data hold time | tDH8 | | 10 | | | ns | |



VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|----------------------------|---------|-----------|------|------|------|------|---------------|
| Address hold time | tAH8 | | 0 | | | ns | CSB RS |
| Address setup time | tAS8 | | 0 | | | ns | |
| System cycle time in write | tCYCWR8 | | 500 | | | ns | WRB (R/WB) |
| Write pulse "L" width | tWRLW8 | | 100 | | | ns | |
| Write pulse "H" width | tWRHW8 | | 350 | | | ns | |
| Data setup time | tDS8 | | 100 | | | ns | D0~D7 |
| Data hold time | tDH8 | | 20 | | | ns | |

11.2 80-Family MCU Read Timing

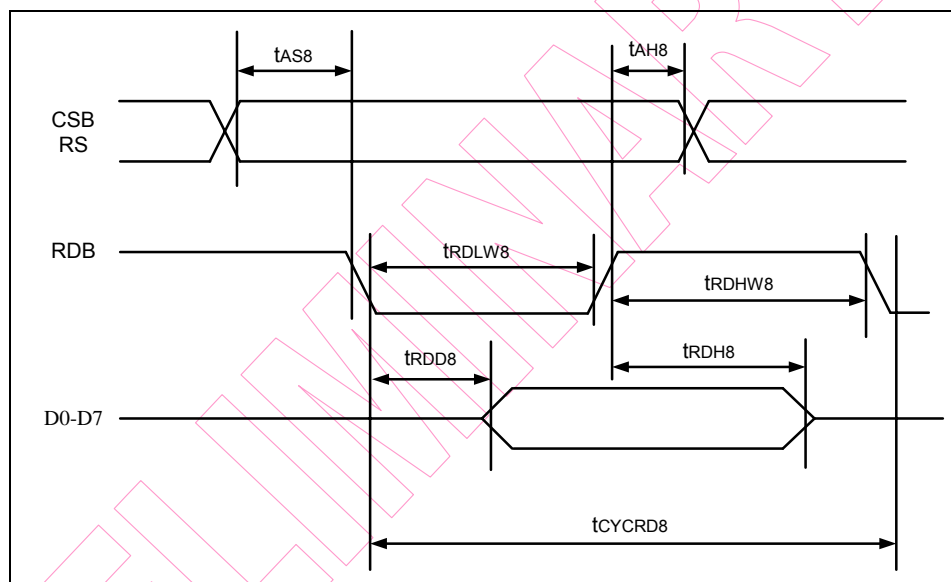


Figure 11-2 80-Family MCU Read Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------------|---------|------------|------|------|------|------|-----------|
| Address hold time | tAH8 | | 0 | | | ns | CSB RS |
| Address setup time | tAS8 | | 0 | | | ns | |
| System cycle time in read | tCYCRD8 | | 380 | | | ns | RDB(E) |
| Read pulse "L" width | tRDLW8 | | 200 | | | ns | |
| Read pulse "H" width | tRDHW8 | | 170 | | | ns | |
| Data setup time | tRDD8 | CL = 80 pF | | | 210 | ns | D0~D7 |
| Data hold time | tRDH8 | | 10 | | | ns | |



VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------------|---------|------------|------|------|------|------|-----------|
| Address hold time | tAH8 | | 0 | | | ns | CSB RS |
| Address setup time | tAS8 | | 0 | | | ns | |
| System cycle time in read | tCYCRD8 | | 540 | | | ns | RDB(E) |
| Read pulse "L" width | tRDLW8 | | 290 | | | ns | |
| Read pulse "H" width | tRDHW8 | | 230 | | | ns | |
| Data setup time | tRDD8 | CL = 80 pF | | | 300 | ns | D0~D7 |
| Data hold time | tRDH8 | | 10 | | | ns | |

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------------|---------|------------|------|------|------|------|-----------|
| Address hold time | tAH8 | | 0 | | | ns | CSB RS |
| Address setup time | tAS8 | | 0 | | | ns | |
| System cycle time in read | tCYCRD8 | | 840 | | | ns | RDB(E) |
| Read pulse "L" width | tRDLW8 | | 440 | | | ns | |
| Read pulse "H" width | tRDHW8 | | 380 | | | ns | |
| Data setup time | tRDD8 | CL = 80 pF | | | 450 | ns | D0~D7 |
| Data hold time | tRDH8 | | 10 | | | ns | |

11.3 68-Family MCU Write Timing

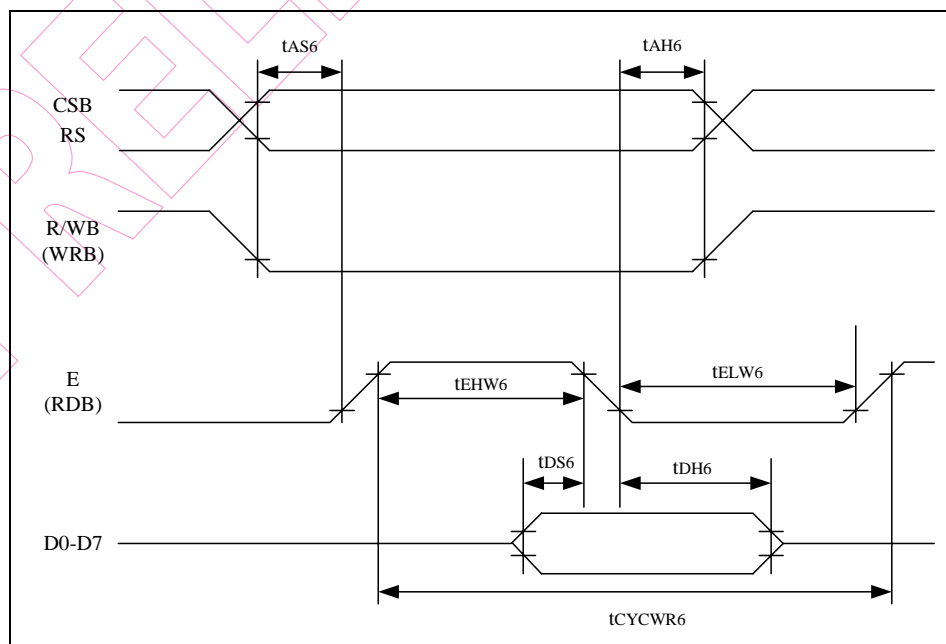


Figure 11-3 68-Family MCU Write Timing Diagram



VSS=0V, VDD = 2.7 ~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|----------------------------|---------|-----------|------|------|------|------|-----------|
| Address hold time | tAH6 | | 0 | | | ns | CSB RS |
| Address setup time | tAS6 | | 0 | | | ns | |
| System cycle time in write | tCYCWR6 | | 200 | | | ns | RDB(E) |
| Write pulse "L" width | tELW6 | | 135 | | | ns | |
| Write pulse "H" width | tEHW6 | | 30 | | | ns | |
| Data setup time | tDS6 | | 60 | | | ns | D0~D7 |
| Data hold time | tDH6 | | 5 | | | ns | |

VSS=0V, VDD = 2.4 ~2.7V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|----------------------------|---------|-----------|------|------|------|------|-----------|
| Address hold time | tAH6 | | 0 | | | ns | CSB RS |
| Address setup time | tAS6 | | 0 | | | ns | |
| System cycle time in write | tCYCWR6 | | 250 | | | ns | RDB(E) |
| Write pulse "L" width | tELW6 | | 160 | | | ns | |
| Write pulse "H" width | tEHW6 | | 50 | | | ns | |
| Data setup time | tDS6 | | 80 | | | ns | D0~D7 |
| Data hold time | tDH6 | | 10 | | | ns | |

VSS=0V, VDD = 2.2 ~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|----------------------------|---------|-----------|------|------|------|------|-----------|
| Address hold time | tAH6 | | 0 | | | ns | CSB RS |
| Address setup time | tAS6 | | 0 | | | ns | |
| System cycle time in write | tCYCWR6 | | 500 | | | ns | RDB(E) |
| Write pulse "L" width | tELW6 | | 350 | | | ns | |
| Write pulse "H" width | tEHW6 | | 100 | | | ns | |
| Data setup time | tDS6 | | 100 | | | ns | D0~D7 |
| Data hold time | tDH6 | | 20 | | | ns | |

11.4 68-Family MCU Read Timing

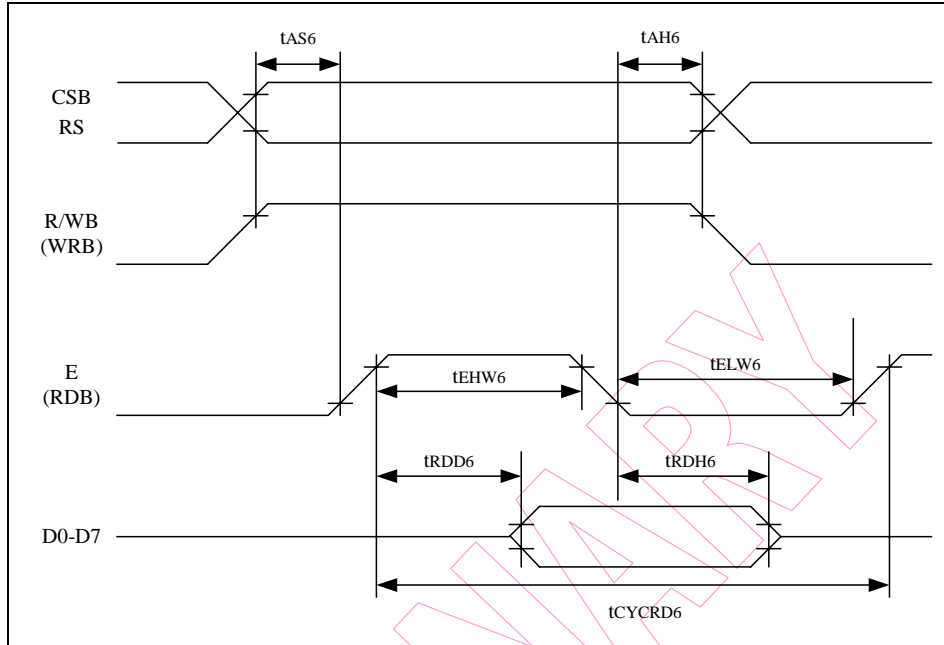


Figure 11-4 68-Family MCU Read Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------------|---------|-----------|------|------|------|------|----------|
| Address hold time | tAH6 | | 0 | | | ns | CSB |
| Address setup time | tAS6 | | 0 | | | ns | RS |
| System cycle time in read | tCYCRD6 | | 380 | | | ns | |
| Write pulse "L" width | tELW6 | | 200 | | | ns | RDB(E) |
| Write pulse "H" width | tEHW6 | | 170 | | | ns | |
| Data setup time | tRDD6 | CL=50pF | | | 210 | ns | D0~D7 |
| Data hold time | tRDH6 | | 10 | | | ns | |

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------------|---------|-----------|------|------|------|------|----------|
| Address hold time | tAH6 | | 0 | | | ns | CSB |
| Address setup time | tAS6 | | 0 | | | ns | RS |
| System cycle time in read | tCYCRD6 | | 540 | | | ns | |
| Write pulse "L" width | tELW6 | | 290 | | | ns | RDB(E) |
| Write pulse "H" width | tEHW6 | | 230 | | | ns | |
| Data setup time | tRDD6 | CL=50pF | | | 300 | ns | D0~D7 |
| Data hold time | tRDH6 | | 10 | | | ns | |



VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------------|---------|-----------|------|------|------|------|-----------|
| Address hold time | tAH6 | | 0 | | | ns | CSB RS |
| Address setup time | tAS6 | | 0 | | | ns | |
| System cycle time in read | tCYCRD6 | | 1000 | | | ns | RDB(E) |
| Write pulse "L" width | tELW6 | | 450 | | | ns | |
| Write pulse "H" width | tEHW6 | | 500 | | | ns | |
| Data setup time | tRDD6 | CL=50pF | | | 650 | ns | D0~D7 |
| Data hold time | tRDH6 | | 10 | | | ns | |

11.5 Serial Interface Timing Diagram

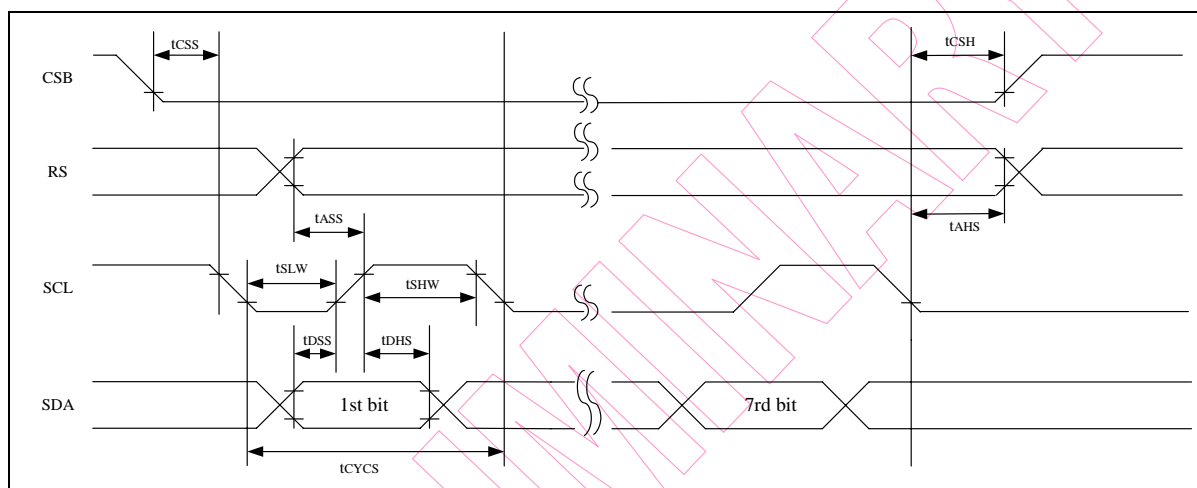


Figure 11-5 Serial Interface Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------|--------|-----------|------|------|------|------|----------|
| Serial clock period | tCYCS | | 200 | | | ns | SCL |
| SCL pulse "H" width | tSHW | | 80 | | | ns | |
| SCL pulse "L" width | tSLW | | 80 | | | ns | |
| Address setup time | tASS | | 40 | | | ns | RS |
| Address hold time | tAHS | | 40 | | | ns | |
| Data setup time | tDSS | | 80 | | | ns | SDA |
| Data hold time | tDHS | | 80 | | | ns | |
| CSB-SCL time | tCSS | | 40 | | | ns | CSB |
| CSB hold time | tCSH | | 40 | | | ns | |



VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------|--------|-----------|------|------|------|------|----------|
| Serial clock period | tCYCS | | 200 | | | ns | SCL |
| SCL pulse "H" width | tSHW | | 80 | | | ns | |
| SCL pulse "L" width | tSLW | | 80 | | | ns | |
| Address setup time | tASS | | 50 | | | ns | RS |
| Address hold time | tAHS | | 50 | | | ns | |
| Data setup time | tDSS | | 80 | | | ns | SDA |
| Data hold time | tDHS | | 80 | | | ns | |
| CSB-SCL time | tCSS | | 50 | | | ns | CSB |
| CSB hold time | tCSH | | 60 | | | ns | |

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|---------------------|--------|-----------|------|------|------|------|----------|
| Serial clock period | tCYCS | | 230 | | | ns | SCL |
| SCL pulse "H" width | tSHW | | 100 | | | ns | |
| SCL pulse "L" width | tSLW | | 100 | | | ns | |
| Address setup time | tASS | | 80 | | | ns | RS |
| Address hold time | tAHS | | 80 | | | ns | |
| Data setup time | tDSS | | 100 | | | ns | SDA |
| Data hold time | tDHS | | 100 | | | ns | |
| CSB-SCL time | tCSS | | 80 | | | ns | CSB |
| CSB hold time | tCSH | | 100 | | | ns | |

11.6 Clock Input Timing

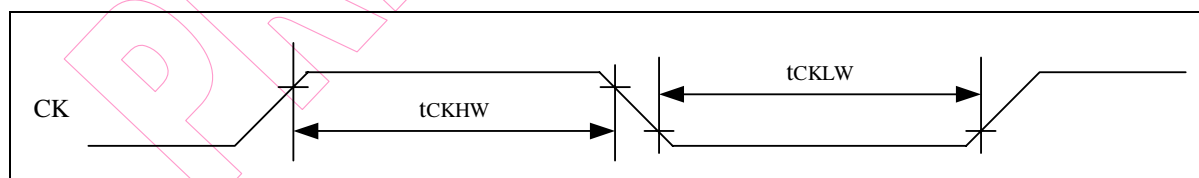


Figure 11-6 Clock Input Timing Diagram

VSS=0V, VDD = 2.4~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|--------------------|---------|-----------|------|------|------|------|----------|
| CK pulse "H" width | tTCKHW2 | | 5.4 | | 6.5 | μs | CK 1 |
| CK pulse "L" width | tTCKLW2 | | 5.4 | | 6.5 | μs | |

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|--------------------|--------|-----------|------|------|------|------|----------|
| CK pulse "H" width | tCKHW2 | | 5.4 | | 6.5 | μs | * |
| CK pulse "L" width | tCKLW2 | | 5.4 | | 6.5 | μs | |

* CK pin. Applied when using the 16 gray scale gradation display mode

11.7 Reset Timing

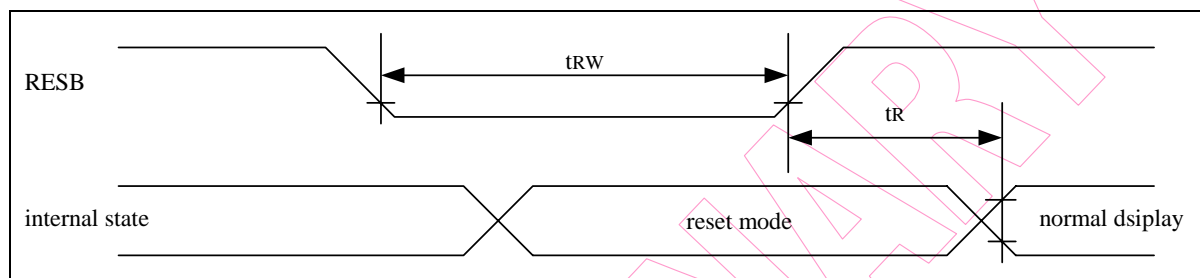


Figure 11-7 Reset Timing Diagram

VSS=0V, VDD = 2.4~3.3V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|-----------------------|--------|-----------|------|------|------|------|----------|
| Reset time | tR | | | | 1 | μs | |
| Reset pulse "L" width | tRW | | 40 | | | μs | RESB |

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin Used |
|-----------------------|--------|-----------|------|------|------|------|----------|
| Reset time | tR | | | | 1.5 | μs | |
| Reset pulse "L" width | tRW | | 40 | | | μs | RESB |

12 Application Circuit

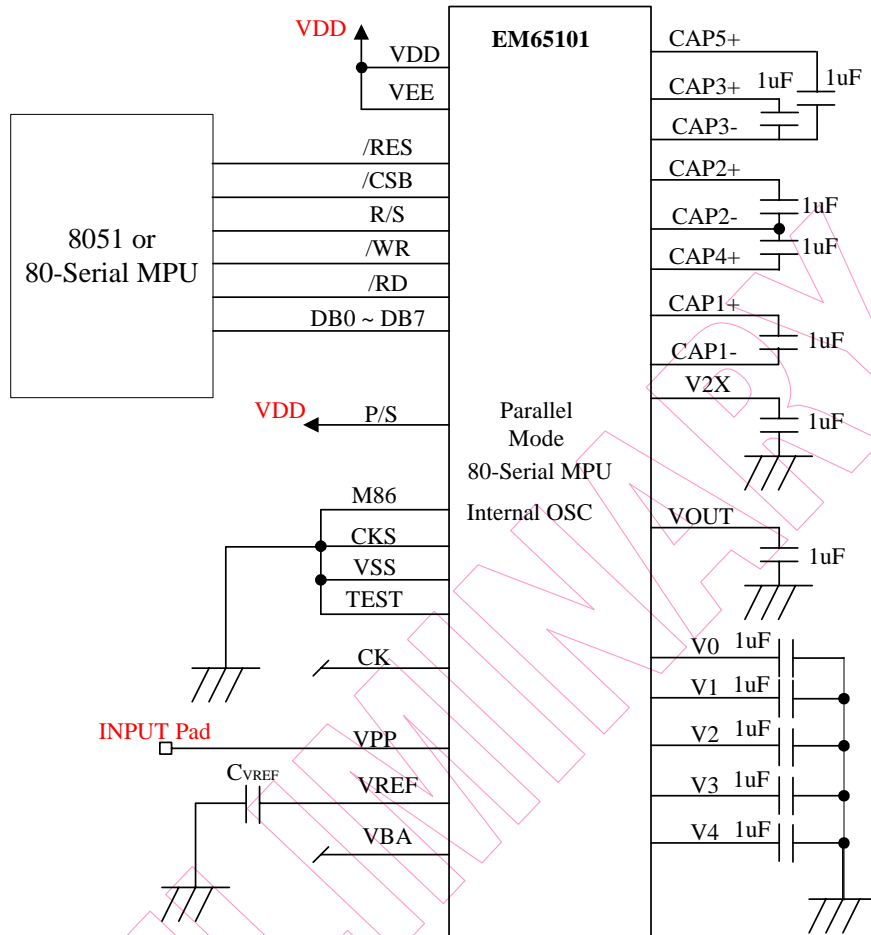


Figure 12-1 EM65101 Application Circuit

NOTE

To obtain a stable voltage, it is recommended that you use VREF to connect a 0.1uF capacitor CVREF to VSS.

13 Tray Information

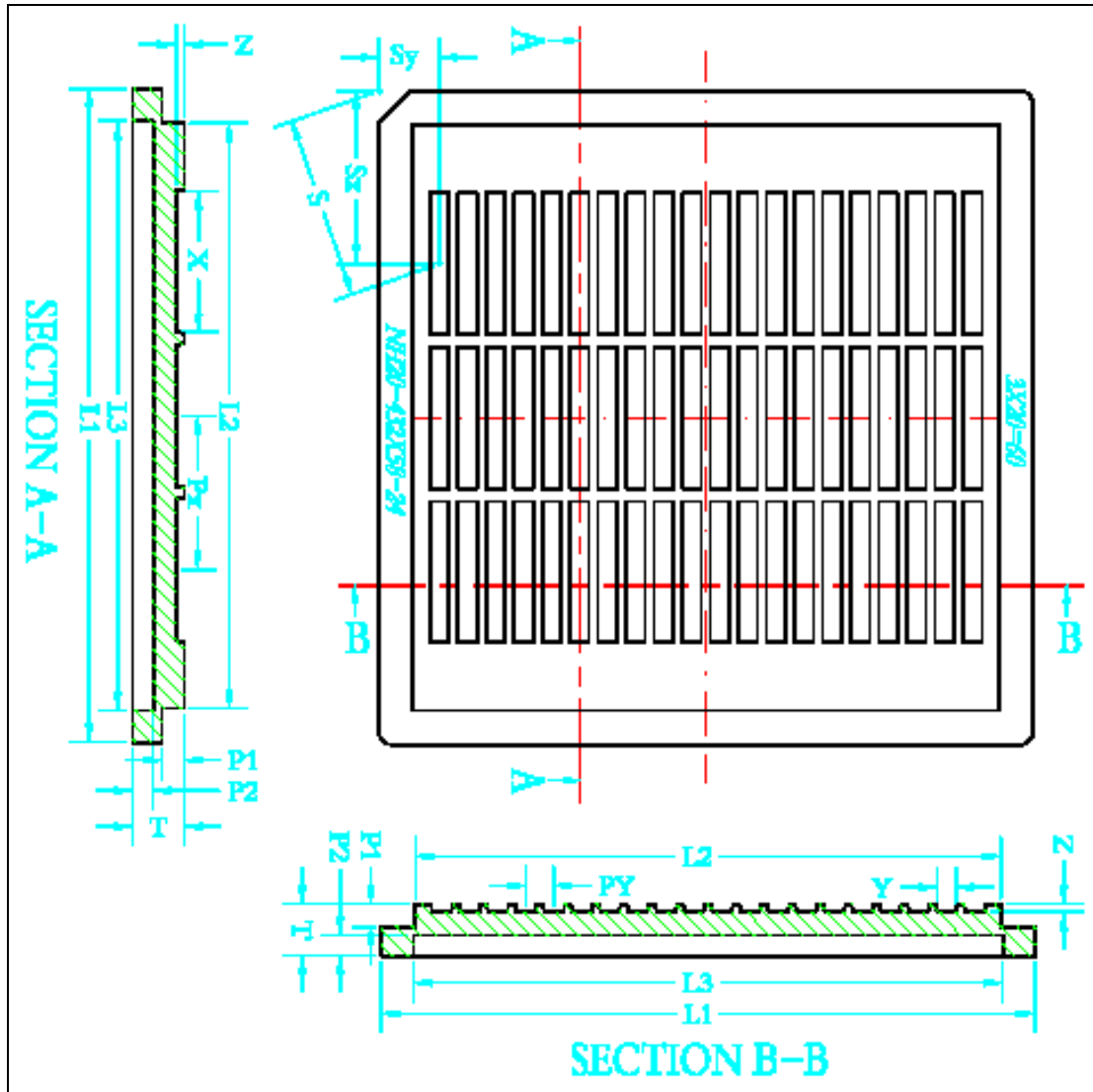


Figure 13-1 EM65101 Tray Diagram

Tray Dimensions (Unit: mm):

| Symbol | Dimensions (mm) | Symbol | Dimensions (mm) |
|--------|-----------------|--------|-----------------|
| L1 | 50.80 | Z | 0.61 ± 0.05 |
| L2 | 45.50 | Px | 11.97 |
| L3 | 45.80 | Py | 2.18 |
| T | 4.00 | Nx | 3 |
| Sx | 13.43 | Ny | 20 |
| Sy | 4.69 | N | 60 |
| S | 14.22 | P1 | 1.76 |
| X | 10.97 ± 0.05 | P2 | 1.60 |
| Y | 1.48 ± 0.05 | | |



PRELIMINARY