GENERAL INSTRUMENT

ER3400
ER3400I/IR
ER3400HR

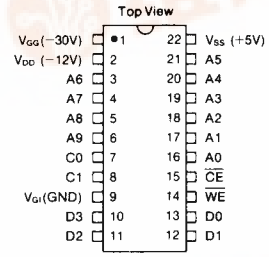
4096 Bit Electrically Alterable Read Only Memory

FEATURES

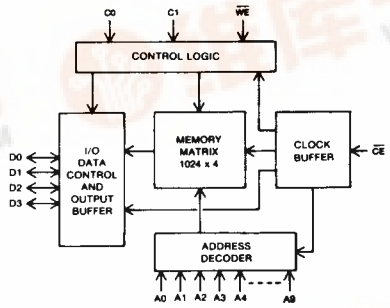
- 1024 word x 4 bit organization
- Latched address and data inputs
- Word or block alterable
- 10 year data storage for ER3400
- 1 year data storage for ER3400IR at +85° C
- and ER3400HR at +95° C
- TTL compatible with pull-up resistors on inputs
- Tri-state outputs
- Read access time: 900ns max.
- Write time: 1ms. Erase time: 10ms
- 10^9 Read cycles/word between refreshes
- 10^7 Read cycles/word for ER3400IR and ER3400HR
- Two extended temperature ranges

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The ER3400 is a 1024 x 4 bit fully decoded Electrically Alterable Read Only Memory fabricated in General Instrument's proven MNOS technology. Address, control and data inputs are latched on board the device thus releasing these lines during Erase and Write operations. Selection of one of the four modes of operation is made by setting the appropriate binary code on control lines C0 and C1. $\overline{CE}$ is used for chip selection and latching of address and control lines. $\overline{WE}$ is used to sample and latch input data on D0-D3 during a Write operation.

Power sequencing protection circuitry is provided on the ER3400 to protect against the accidental alteration of data during power Up/Down. However, due to the unpredictable nature of power up and power down sequences in some systems, it is important to apply and remove the programming voltage V_{GG} only when V_{SS} and V_{DD} are within their specified limits.

For applications requiring extended temperature ranges the ER3400I, ER3400IR and ER3400HR are available.

RELATED APPLICATION NOTES

1217	The ER3400: an easy to use 4K EAROM
1218	Interfacing the ER3400 to an eight bit microcomputer
1220	Generating EAROM programming voltages from a 5 volt supply
1210	Data retention testing of the ER3400

PIN FUNCTIONS

Name	Function
A0-A9	10-Bit Word Address
D0-D3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C0, C1	Mode Control Inputs C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_{GG} (with respect to V_{SS}) .... −20V to +0.3V
Storage temperature (without data retention) ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

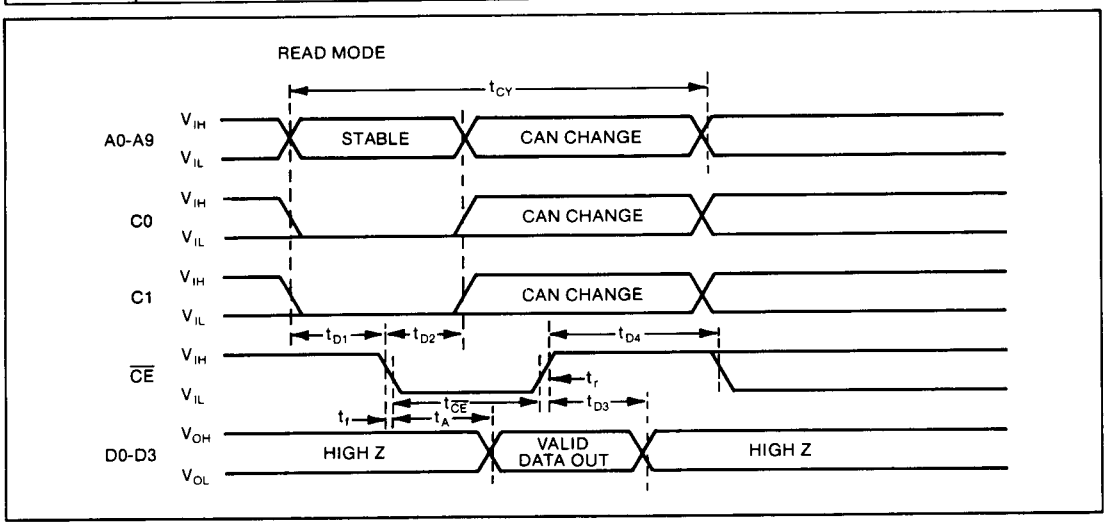
*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Condition (unless otherwise noted)

V_{SS} = +5V to ±5%
V_{DD} = −12V ±5%
V_{GG} = −30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0° C to +70° C (ER3400)
−40° C to +85° C (ER3400I/IR)
−55° C to +95° C (ER3400HR)

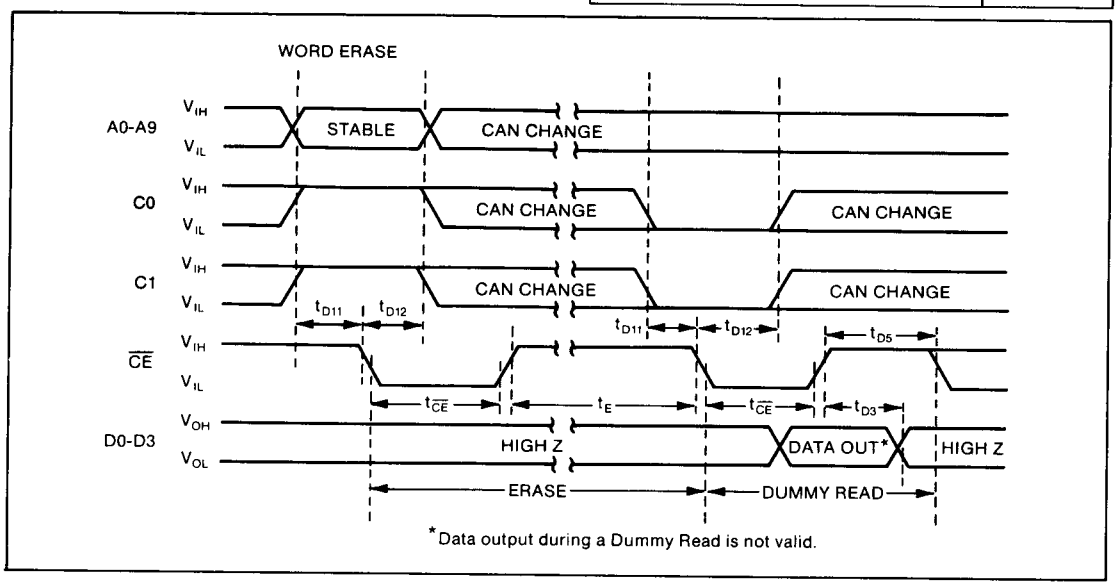
		ER3400			ER3400IR/ER3400HR				
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.15	V_{SS} −1.0	—	V_{SS} +0.15	V	
Input Logic "0"	V_{IL}	−10	—	0.8	−10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 2mA
Output Logic "0"	V_{OL}	—	—	0.4	—	—	0.5	V	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	−2.0	—	—	−2.0	μA	V_{ON} = V_{SS} −15 Volts
Data Input Leakage	I_{LD}	—	—	−10.0	—	—	−10.0	μA	V_{IN} = V_{SS} −15 Volts
Power Supply Current									
V_{DD} Supply Current: Chip selected	I_{DD}	—	—	−25.0	—	—	−30.0	mA	V_{DD} = V_{SS} −17 Volts
Chip de-selected	I_{DD}	—	—	−12.0	—	—	−15.0	mA	V_{DD} = V_{SS} −17 Volts
V_{GG} Supply Current: Write mode	I_{GG}	—	—	−4.0	—	—	−5.0	mA	V_{GG} = V_{SS} −35 Volts
V_{SS} Supply Current: Chip selected	I_{SS}	—	—	−31.0	—	—	−37.0	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
Chip de-selected	I_{SS}	—	—	−14.5	—	—	−18.0	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
AC CHARACTERISTICS									
Input capacitance—control inputs	C_I	—	6	8	—	6	8	pf	
Input capacitance—data inputs	C_D	—	8	10	—	8	10	pf	



Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Read Cycle Time	t_{CY}	1700	—	1750	—	ns	
Address and Control to $\overline{CE}$	t_{D1}	100	—	100	—	ns	
Address and Control Hold Time	t_{D2}	250	—	350	—	ns	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High	t_{D4}	700	—	750	—	ns	
Access Time	t_A	—	900	—	1000	ns	Load = 2K + 100pf to V_{SS}
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{CE}$ Rise, Fall Time	t_r, t_f	10	100	10	100	ns	
Number of Read Accesses per Location Between Refresh	N_{RA}	10^9	—	10^7	—	—	

READ OPERATION

Address and control line inputs are latched on the falling edge of $\overline{CE}$. With control lines C0 and C1 both low a read cycle will be initiated. After the access time t_A the data read will be output on data lines D0-D3. $\overline{CE}$ must be held high for a minimum of 700ns between memory read cycles. To reduce power consumption the ER3400 may be operated with V_{GG} held at V_{SS} in the read mode.



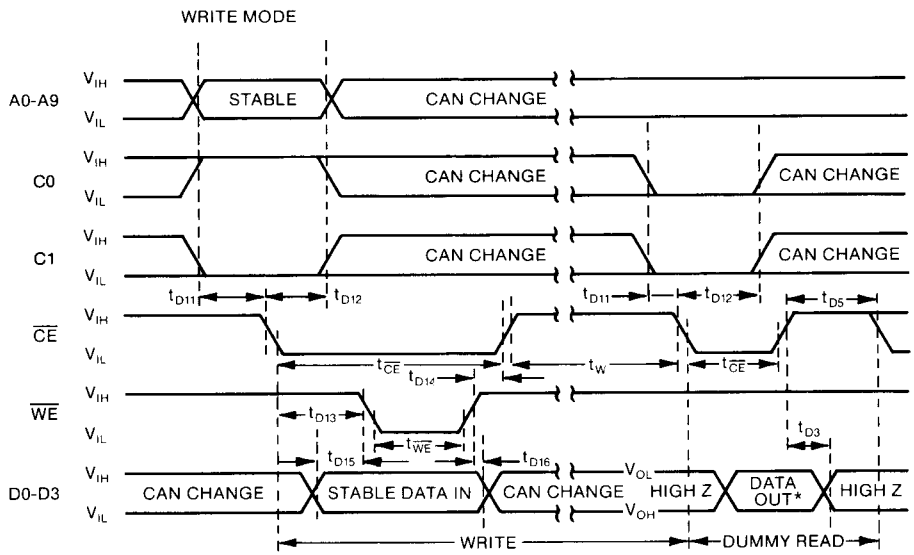
Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	250	—	ns	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
Erase Time	t_E	10	20	10	20	ms	

WORD ERASE OPERATION

An erase cycle is required prior to a write in order to precondition the memory cells to be written. A word erase operation erases only the four bits of the addressed memory location. The falling edge of $\overline{CE}$ latches the control inputs and the address of the word to be erased. The rising edge of $\overline{CE}$ in the erase mode signals the start of the erase cycle which produces a positive shift in the threshold of the selected MNOS memory transistors. An erase operation must be terminated by a dummy read operation. The dummy read need not occur on the same location as the preceding erase, therefore, the state of the address lines A0-A9 are immaterial during the dummy read cycle. Data output during a dummy read cycle is not valid data.

BLOCK ERASE OPERATION

A block erase operation erases all 4096 bits of memory to the "1" state, in all other respects the operation is identical to the word erase operation described above.



*Data output during a Dummy Read is not valid.

Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	350	—	ns	
$\overline{CE}$ Fall to $\overline{WE}$ Fall Delay	t_{D13}	0	—	0	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$
$\overline{WE}$ Rise to $\overline{CE}$ Rise Delay	t_{D14}	−50	—	−100	—	ns	rise by 50ns maximum
Data Stable to $\overline{WE}$	t_{D15}	0	—	0	—	ns	
$\overline{WE}$ Rise to End of Data Stable	t_{D16}	100	—	100	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{WE}$ Pulse Width	$t_{\overline{WE}}$	500	—	650	—	ns	
Write Time	t_W	1	2	1	2	ms	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
Unpowered Data Storage Time	t_S	10	—	1	—	YRS.	See Note 1
Number of Reprogramming Cycles	N_W	10^3	—	10^3	—	—	See Note 1
Number of Read Accesses/Location between Refresh	N_{RA}	10^9	—	10^9	—	—	

NOTE 1: Does not imply end of useful life. See "Write Operation" for further information.

WRITE OPERATION

Control lines C0 and C1 along with address lines A0-A9 are latched on the falling edge of $\overline{CE}$. Input data on D0-D3 is latched on the rising edge of $\overline{WE}$. $\overline{WE}$ may be tied to $\overline{CE}$ for all operations, however, this separate latching allows the ER3400 to be used in certain systems where address and data busses are multiplexed. The writing of the selected memory transistors is initiated by the rising edge of $\overline{CE}$. $\overline{CE}$ must remain high for the duration of the write time. A write operation can only be terminated by a dummy read. To avoid bus contention, the data lines must be tri-stated prior to initiating the dummy read cycle. The data output by a dummy read cycle is not valid data. The dummy read need not occur on the same location as the previous write, therefore, address line A0-A9 may be allowed to change during the dummy read cycle.

The specification of 10 years non-volatile data retention after a minimum of 10^3 reprogramming cycles is merely one point on the curve of retention versus reprogramming cycles and does not imply a sudden cut-off or end of life. As the number of Erase/Write cycles per address increases, a gradual, logarithmic reduction in data retention capability occurs with 1 year of retention being a typical figure after 10^4 cycles.

TYPICAL CHARACTERISTIC CURVES

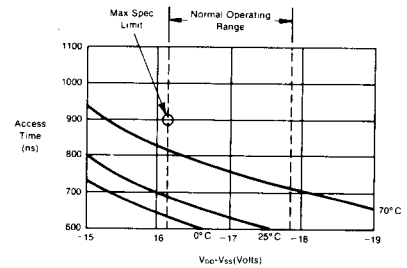


Fig.3 TYPICAL ACCESS TIME vs. POWER SUPPLY VOLTAGE

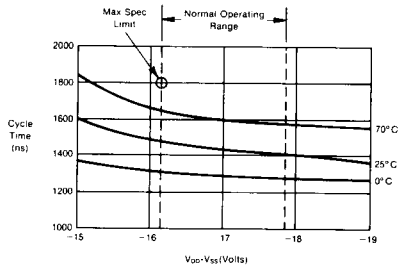


Fig.4 TYPICAL CYCLE TIME vs. POWER SUPPLY VOLTAGE

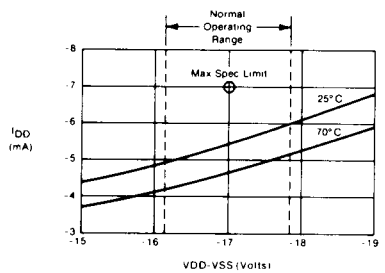


Fig.5 I_{DD} vs. V_{DD}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

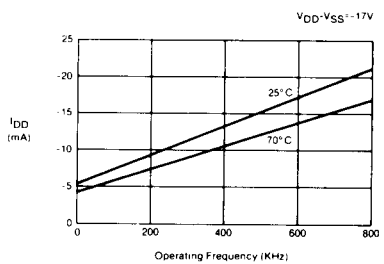


Fig.6 I_{DD} vs. OPERATING FREQUENCY IN READ MODE AND SELECTED

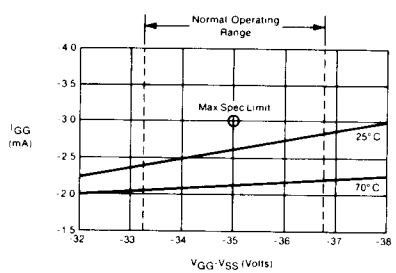


Fig.7 I_{GG} vs. V_{GG}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED