eorex

64MB/128MB/256MB/512MB Secure Digital Card

Description

ESSDC64 / ESSDC128 / ESSDC256 / ESSDC512 are different memory capacities from 64MB to 512MB of the Secure Digital Card. They are non-volatile, which means no external power required to retain the information stored on these. Besides, They are also the solid-state device that without moving parts to skip or break down. ESMSDC64 / ESMSDC128 / ESMSDC256 / ESMSDC512 can offer an incredible combination of fast data transfer, great flexibility, excellent security and incredibly small size.

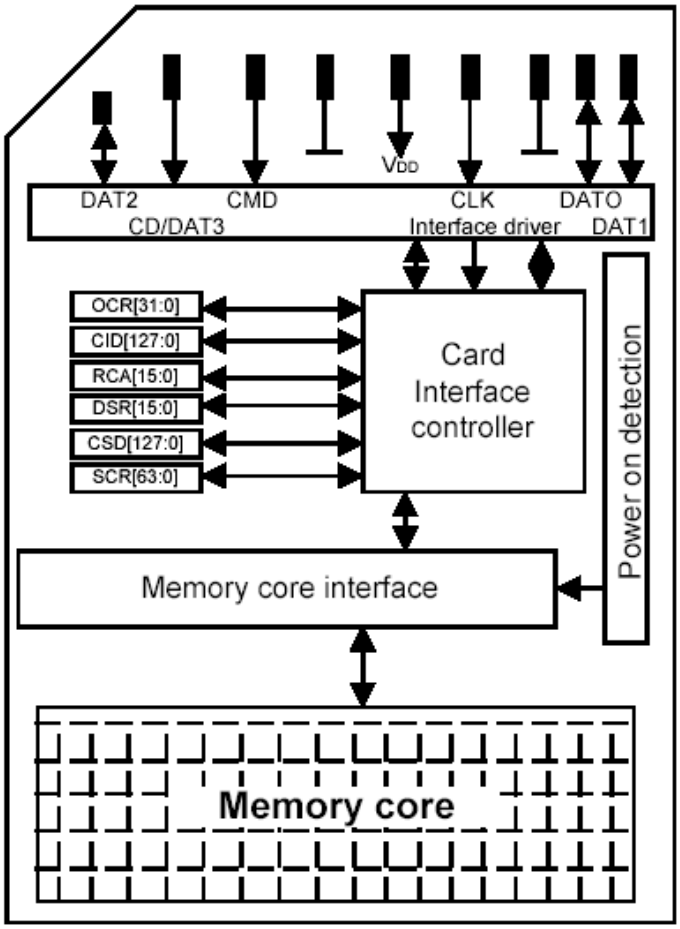
Features

- Operating Voltage: 2.7V ~ 3.6V
- Operating Temperature: -25℃ ~ 85℃
- Data Transfer Rate: Average 2MB/s
- Durability: 10,000 insertion/removal cycles
- Mechanical Write Protection Switch
- SD Host allows MultiMediaCard upward compatibility
- Form Factor: 24mm x 32mm x 2.1mm

Pin Definition

Pin No.	Name	Type	Description
1	CD/DA	I/O/PP	Card Detect/Data Line[Bit3]
2	CMD	PP	Command/Response
3	V_{SS1}	S	Supply voltage ground
4	V_{DD}	S	Supply voltage
5	CLK	I	Clock
6	V_{SS2}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]
8	DAT1	I/O/PP	Data Line [Bit1]
9	DAT2	I/O/PP	Data Line [Bit2]

Architecture



Bus Operating Conditions

1. General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

2. Power Supply Voltage

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	V_{DD}	2.0	3.6	V	CMD0, 12, 55, ACMD41 commands
Supply voltage specified in OCR register					Except CMD0, 15, 55, ACMD41 commands
Supply voltage differentials (V_{SS1}, V_{SS2})		-0.3	0.3	V	
Power up time			250	ms	From 0V to V_{DD} Min.

Note: The current consumption of any card during the power-up procedure must not exceed 10mA.

3. Bus Signal Line Load

The total capacitance C_L of each line of the MultiMediaCard bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:

$C_L = C_{HOST} + C_{BUS} + N^* C_{CARD}$

Where N is the number of connected cards. Requiring the sum of the host and bus capacitance's not to exceed 30pF for up to 10 cards, and 40pF up to 30 cards, the following values must not be exceeded:

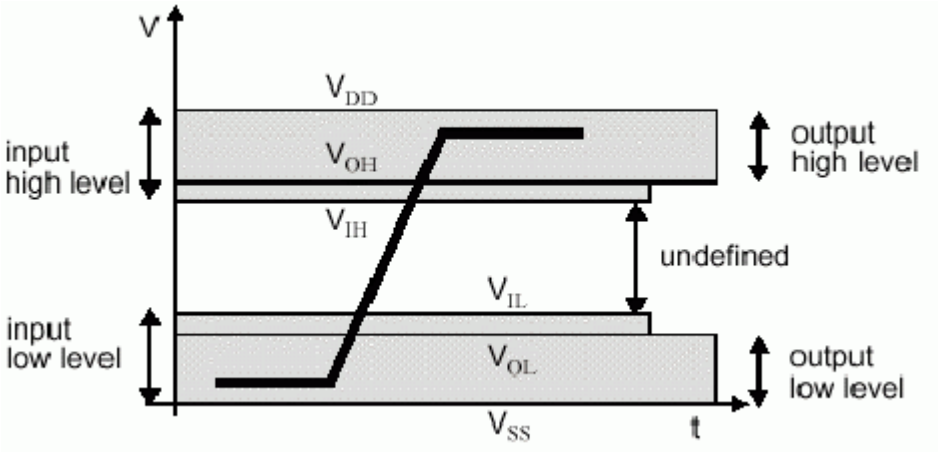
Parameter	Symbol	Min	Max	Unit	Remark
Bus signal line capacitance	C_L		100	pF	fpp≦20MHz, 7 cards
Signal card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	fpp≦20MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	KΩ	May be used for card detection

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD}, R_{DAT}	10	100	KΩ	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	fpp≦5MHz, 21 cards

4. Bus Signal Levels

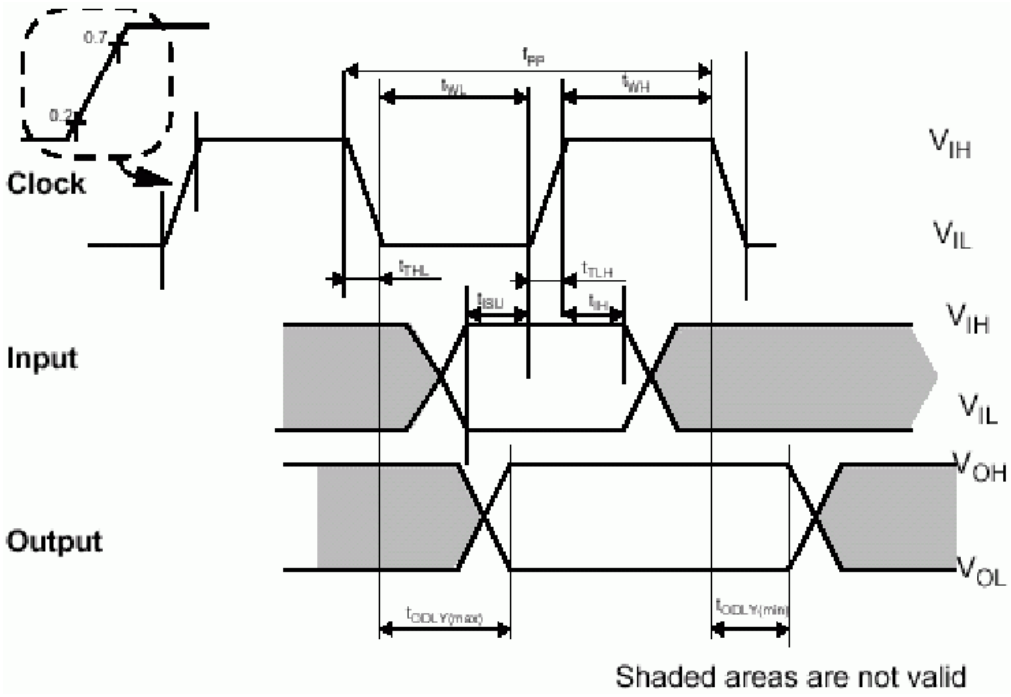
As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min	Max	Unit	Remark
Output HIGH voltage	V_{OH}	0.75* V_{DD}		V	I_{OH}=-100μA @V_{DD} min
Output LOW voltage	V_{OL}		0.125* V_{DD}	V	I_{OL}=-100μA @V_{DD} min
Input HIGH voltage	V_{IH}	0.625* V_{DD}	V_{DD}+0.3	V	
Input LOW voltage	V_{IL}	V_{SS}-0.3	0.25* V_{DD}	V	

5. Bus Timing



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{pp}	0	20	MHz	CL<100pF,(7 cards)
Clock frequency Identification Mode (The low freq. is required for MultiMediaCard compatibility.)	f_{OD}	0	400	KHz	CL<250pF,(21 cards)
Clock low time	t_{WL}	10		ns	CL≤100pF, (7 cards)
		50		ns	CL≤250pF, (21 cards)
Clock high time	t_{WH}	10		ns	CL≤100pF, (7 cards)
		50		ns	CL≤250pF, (21 cards)
Clock rise time	t_{TLH}		10	ns	CL≤100pF, (7 cards)
			50	ns	CL≤250pF, (21 cards)
Clock fall time	t_{THL}		10	ns	CL≤100pF, (7 cards)
			50	ns	CL≤250pF, (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	f_{ISU}	5		ns	CL<25pF,(1 cards)
Input hold time	f_{IH}	5		ns	CL<25pF,(1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time	f_{ODLY}	0	14	ns	CL<25pF,(1 cards)

6. Reliability and Durability

Temperature	Operation: -25℃ / 85℃ (Target spec) Storage: -40℃ (168h) / 85℃ (500h) Junction temperature: max. 95℃
Moisture and corrosion	Operation: 25℃ / 95% rel. humidity Storage: 40℃ / 93% rel. hum./ 500h Salt Water Spray: 3% NaCI/35C; 24h acc. MIL STD Method 1009
Durability	10,000 mating cycles; test procedure: tbd.
Bending	t.b.d
Torque	t.b.d
Drop test	1.5m free fall
UV light exposure	UV: 200nm, 15Ws/cm^2 according to ISO7816-1
Visual inspection Shape and form	No warp page; no mold skin; complete form; no cavities surface smoothness <= -0.1mm/cm^2 within contour; no cracks; no pollution (fat, oil dust, etc.)
Minimum moving force of WP witch	40gf (Ensures that the WP switch will not slide while it is inserted to the connector.)
WP Switch cycles	t.b.d

Above technical information is based on industry standard data and tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the tight to make changes in specifications at any time without prior notice.