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3-W Mono Filterless Class-D Audio Power Amplifier

DESCRIPTION

The EUA2011 is a high efficiency, 3W mono class-D audio power amplifier. A low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplifying design.

Operating in a single 5V supply, EUA2011 is capable of driving 4Ω speaker load at a continuous average output of 3W/10% THD+N or 2W/1% THD+N. The EUA2011 has high efficiency with speaker load compared to a typical class AB amplifier. With a 3.6V supply driving an 8Ω speaker , the efficiency for a 400mW power level is 88%.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the EUA2011. The gain of EUA2011 is externally configurable which allows independent gain control from multiple sources by summing signals from separate sources.

The EUA2011 is available in space-saving WCSP and TDFN packages.

FEATURES

- Unique Modulation Scheme Reduces EMI Emissions
- Efficiency at 3.6V With an 8-Ω Speaker:
  - 88% at 400 mW
  - 80% at 100 mW
- Low 2.4-mA Quiescent Current and 0.5-μA Shutdown Current
- 2.5V to 5.5V Wide Supply Voltage
- Shutdown Pin Compatible with 1.8V Logic GPIO
- Optimized PWM Output Stage Eliminates LC Output Filter
- Improved PSRR (−72 dB) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- Internally Generated 250-kHz Switching Frequency
- Integrated Pop and Click Suppression Circuitry
- 1.5mm× 1.5mm Wafer Chip Scale Package (WCSP) and 3mm× 3mm TDFN-8 package
- RoHS compliant and 100% lead(Pb)-free

APPLICATIONS

- Ideal for Wireless or cellular Handsets and PDAs

Typical Application Circuit

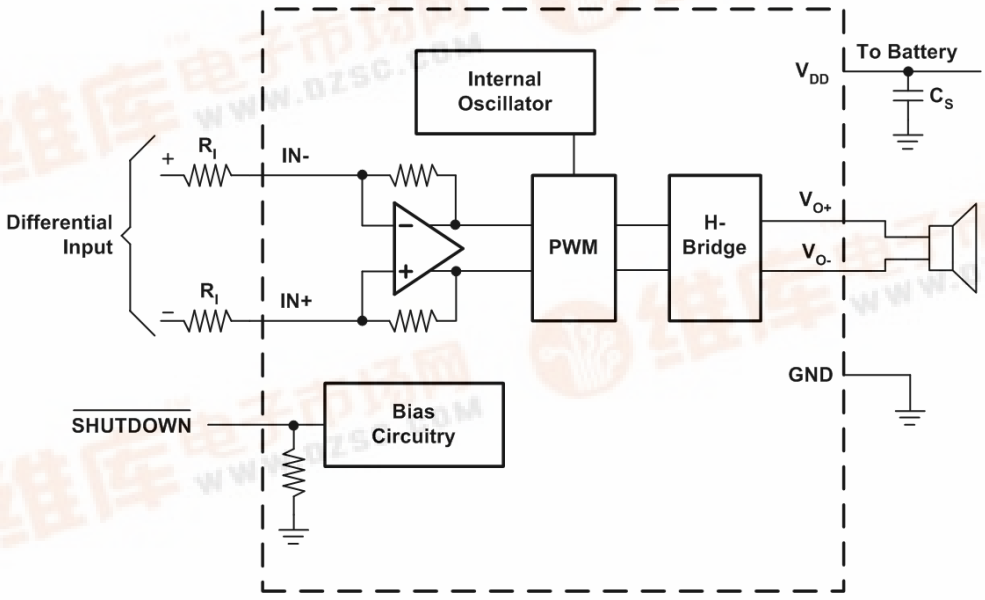
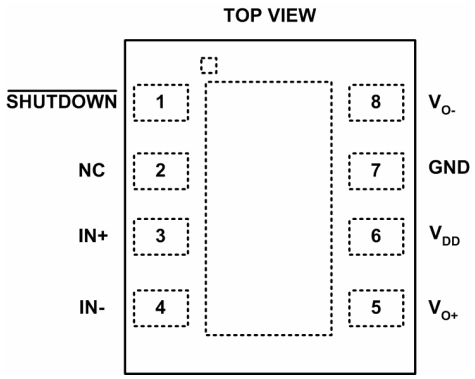
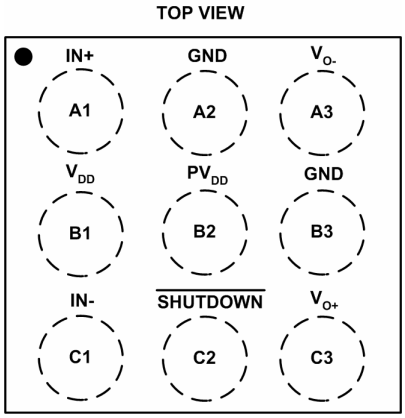


Figure1.

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TDFN-8		WCSP-9	

Pin Description

PIN	TDFN-8	WCSP-9	I/O	DESCRIPTION
$\overline{\text{SHUTDOWN}}$	1	C2	I	Shutdown terminal (active low logic)
PV_{DD}	-	B2	I	Power Supply
+IN	3	A1	I	Positive differential input
-IN	4	C1	I	Negative differential input
V_{O-}	8	A3	O	Negative BTL output
V_{DD}	6	B1	I	Power supply
GND	7	A2/B3	I	High-current ground
V_{O+}	5	C3	O	Positive BTL output
NC	2	-		No internal connection

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA2011JIR1	TDFN-8	xxxxx A2011	-40 °C to 85°C
EUA2011HIR1	WCSP-9	xxx c0	-40 °C to 85°C

EUA2011 □ □ □ □

- Lead Free Code
  1: Lead Free 0: Lead
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  J: TDFN
  H: WCSP

Absolute Maximum Ratings

- Supply Voltage, V_{DD} ---------- -0.3 V to 6V
- Voltage at Any Input Pin ---------- -0.3 V to V_{DD} +0.3V
- Junction Temperature, T_{JMAX} ---------- 150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to 150°C
- ESD Susceptibility ---------- 2kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance
  - θ_{JA} (TDFN) ---------- 47°C/W
  - θ_{JA} (WCSP) ---------- 77.5°C/W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{DD}		2.5	5.5	V
High-level input voltage, V_{IH}	$\overline{SHUTDOWN}$	1.3	V_{DD}	V
Low-level input voltage, V_{IL}	$\overline{SHUTDOWN}$	0	0.35	V
Input resistor, R_I	Gain ≤ 20V/V (26dB)	15		kΩ
Common mode input voltage range, V_{IC}	V_{DD}=2.5V,5.5V,CMRR ≤ -49dB	0.5	V_{DD}-0.8	V
Operating free-air temperature, T_A		-40	85	°C

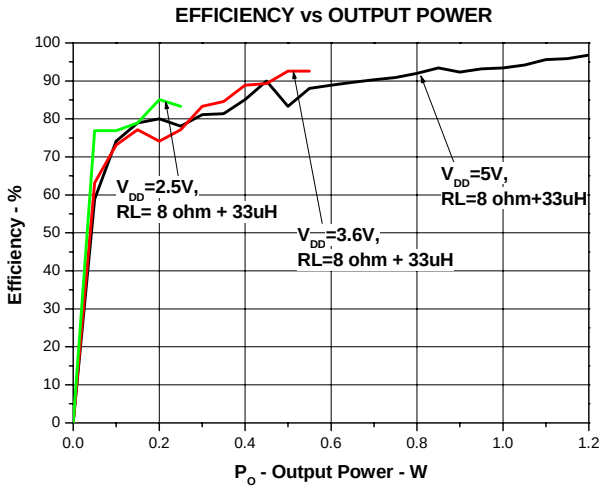
Electrical Characteristics T_A = 25°C (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2011			Unit
			Min	Typ	Max.	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I= 0V,A_V=2 V/V, V_{DD}=2.5V to 5.5V		1	25	mV
PSRR	Power supply rejection ratio	V_{DD}= 2.5V to 5.5V		-72	-55	dB
CMRR	Common mode rejection ratio	V_{DD}= 2.5V to 5.5V, V_{IC}= V_{DD}/2 to 0.5V, V_{IC}= V_{DD}/2 to V_{DD} -0.8 V		-60	-48	dB
$\|I_{IH}\|$	High-level input current	V_{DD}= 5.5V, V_I= 5.8V			100	µA
$\|I_{IL}\|$	Low-level input current	V_{DD}= 5.5V, V_I= -0.3V			5	µA
$I_{(Q)}$	Quiescent current	V_{DD}= 5.5V, no load		3.5	4.9	mA
		V_{DD}= 3.6V, no load		2.4		
		V_{DD}= 2.5V, no load		2		
$I_{(SD)}$	Shutdown current	V($\overline{SHUTDOWN}$)=0.35V, V_{DD}= 2.5V to 5.5V		0.5		µA
rDS(on)	Static drain-source on-state resistance	V_{DD}= 2.5V		700		mΩ
		V_{DD}= 3.6V		500		
		V_{DD}= 5.5V		400		
	Output impedance in $\overline{SHUTDOWN}$	V($\overline{SHUTDOWN}$)=0.4V		>1		kΩ
$f_{(sw)}$	Switching frequency	V_{DD}= 2.5V to 5.5V	200	250	300	kHz
	Resistance from shutdown toGND			300		kΩ

Electrical Characteristics T_A = 25°C ,Gain= 2V/V,R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2011 Min	EUA2011 Typ	EUA2011 Max.	Unit
P_O	Output power	THD+N=10%, f=1kHz, R_L=4Ω	V_{DD}= 5V		3		W
			V_{DD}= 3.6V		1.4		
			V_{DD}= 2.5V		0.65		
		THD+N=1%, f=1kHz, R_L=4Ω	V_{DD}= 5V		2.15		W
			V_{DD}= 3.6V		1.06		
			V_{DD}= 2.5V		0.49		
		THD+N=10%, f=1kHz, R_L=8Ω	V_{DD}= 5V		1.67		W
			V_{DD}= 3.6V		0.84		
			V_{DD}= 2.5V		0.39		
		THD+N=1%, f=1kHz, R_L=8Ω	V_{DD}= 5V		1.36		W
			V_{DD}= 3.6V		0.66		
			V_{DD}= 2.5V		0.30		
THD+N	Total harmonic distortion plus noise	V_{DD}= 5V,P_O=1W, R_L=8Ω, f=1kHz			0.18		%
		V_{DD}= 3.6V,P_O=0.5W, R_L=8Ω, f=1kHz			0.18		
		V_{DD}= 2.5V,P_O=200mW, R_L=8Ω, f=1kHz			0.17		
kSVR	Supply ripple rejection ratio	V_{DD}= 3.6V, Inputs ac-grounded with C_I= 2μF	f=217 Hz, $V_{(RIPPLE)}$=200mVpp		-60		dB
SNR	Signal-to-noise ratio	V_{DD}= 5V,P_O=1W, R_L=8Ω			93		dB
Vn	Output voltage noise	V_{DD}= 3.6V, f=20Hz to 20kHz,Inputs ac-grounded with C_I= 2μF	No weighting		62		μV_{RMS}
			A weighting		45		
CMRR	Common mode rejection ratio	V_{DD}= 3.6V, V_{IC}=1 V_{PP}	f=217 Hz		-55		dB
Z_I	Start-up time from shutdown	V_{DD}= 3.6V			11.5		ms

Typical Operating Characteristics



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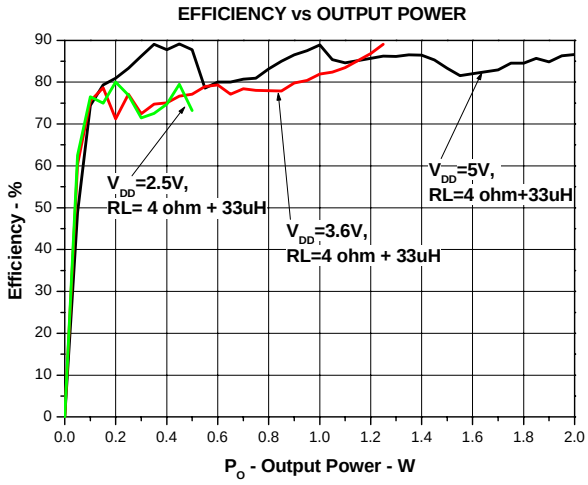

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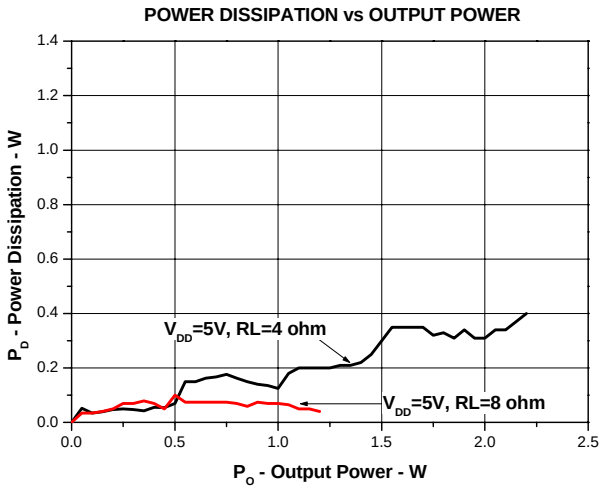

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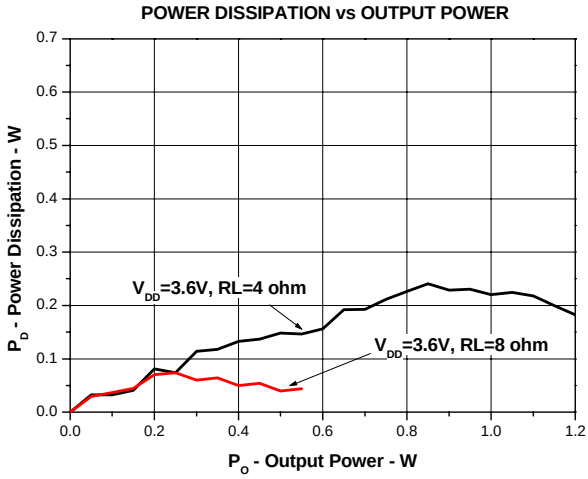

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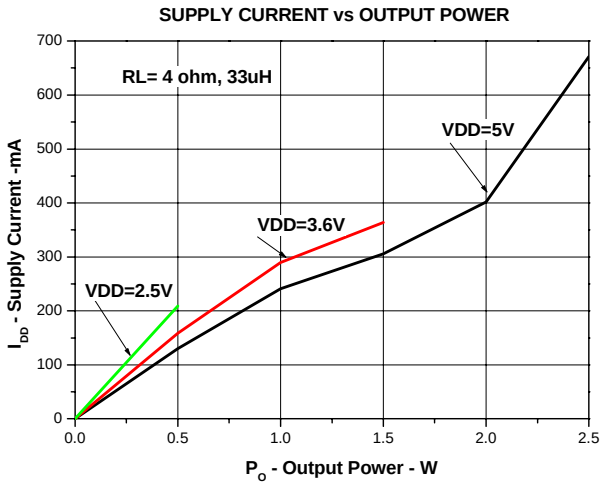

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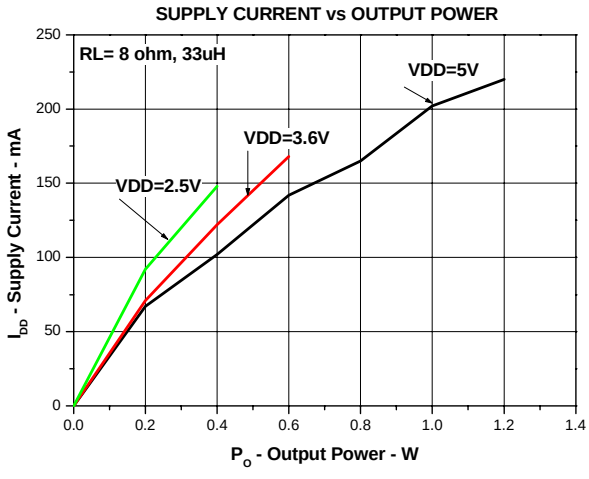

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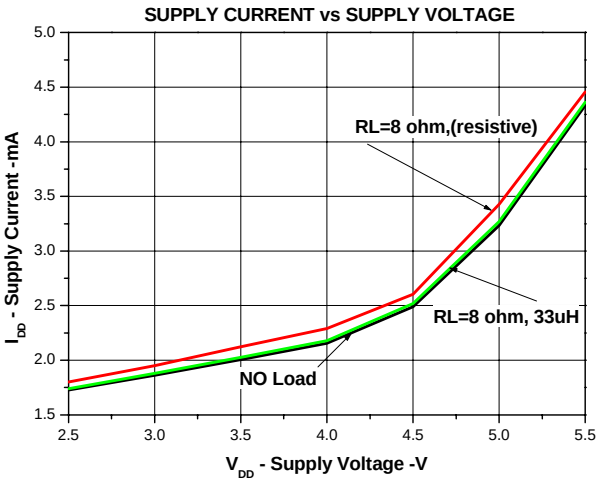

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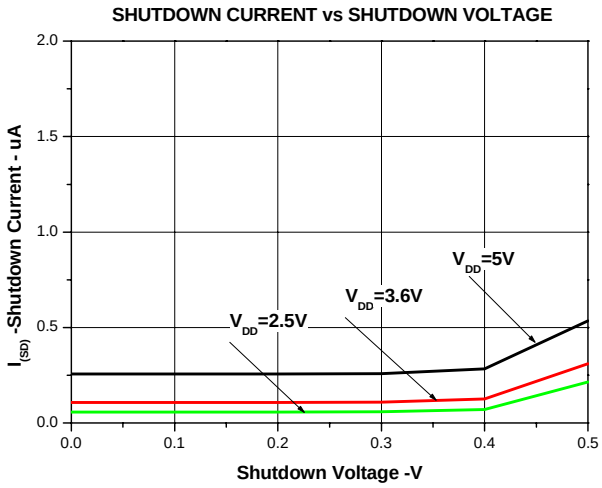

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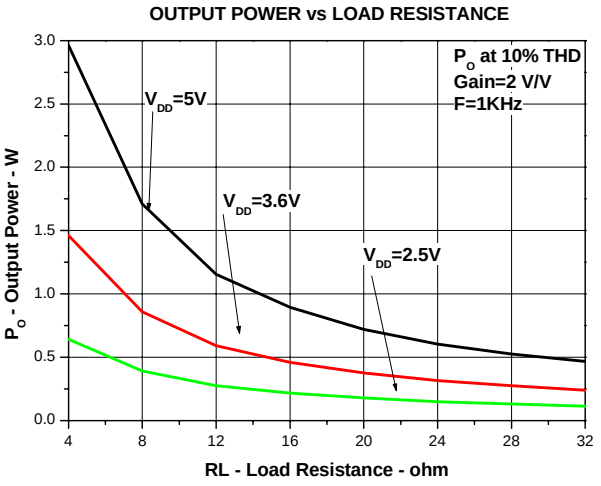

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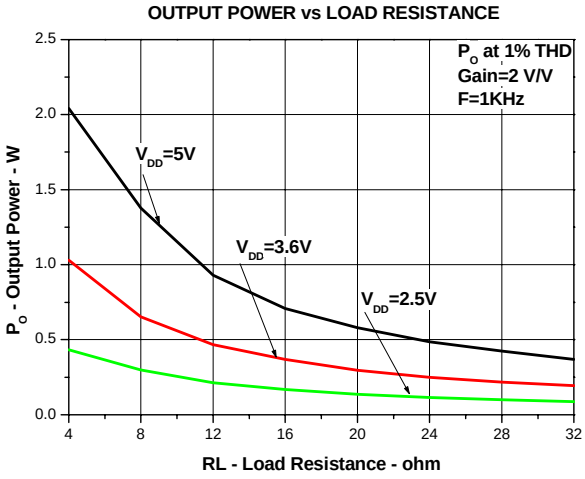

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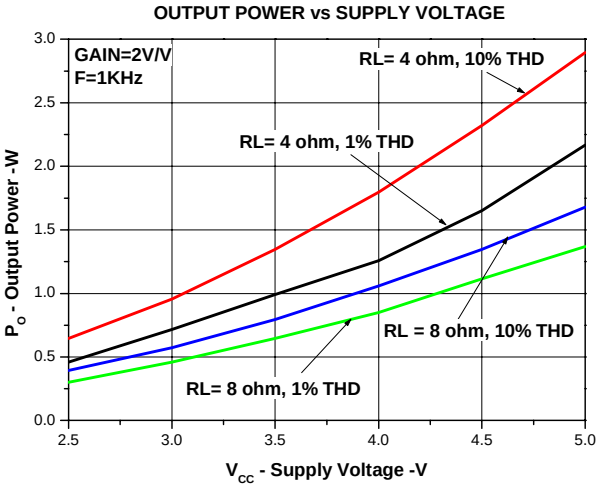

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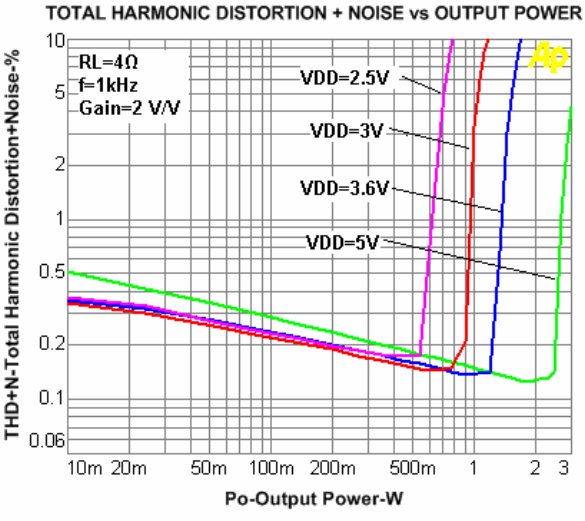

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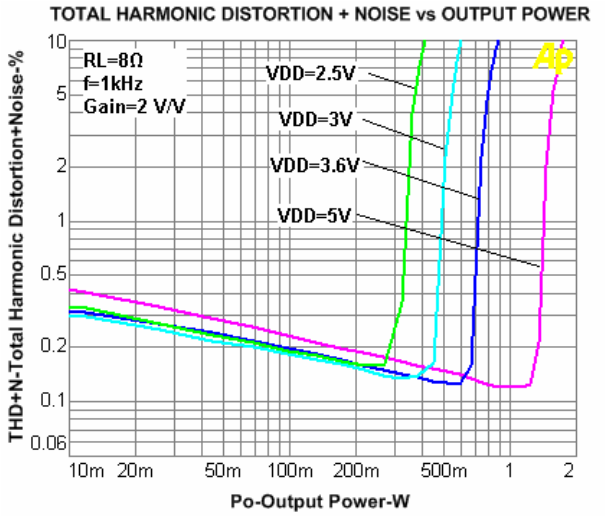

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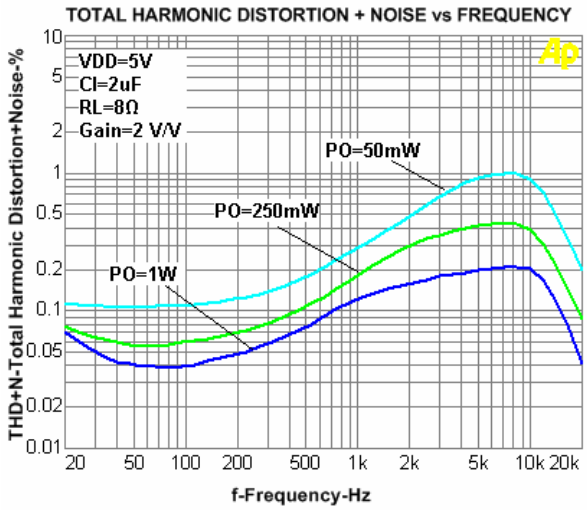

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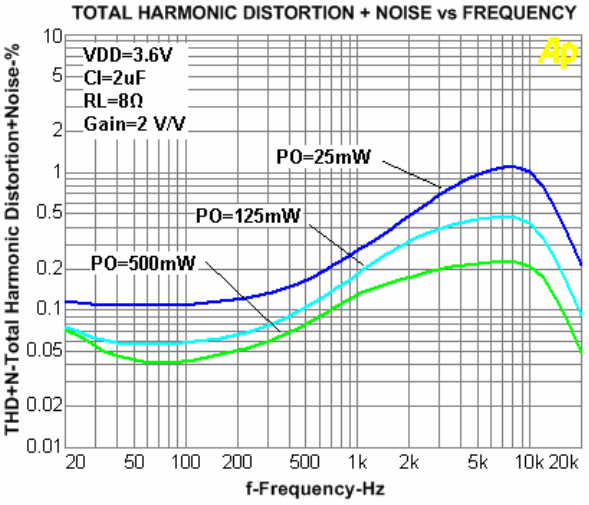

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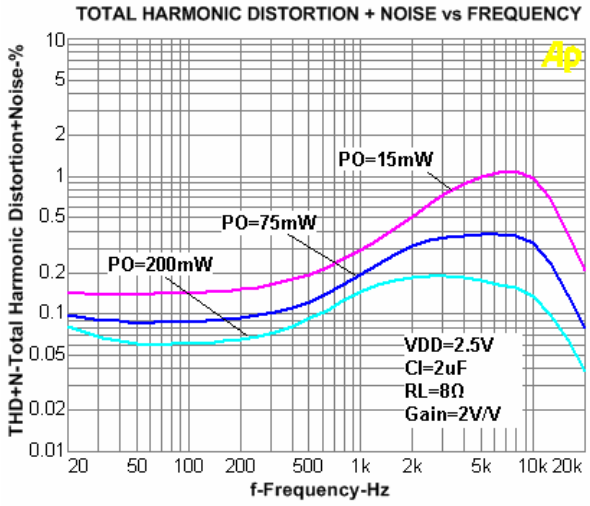

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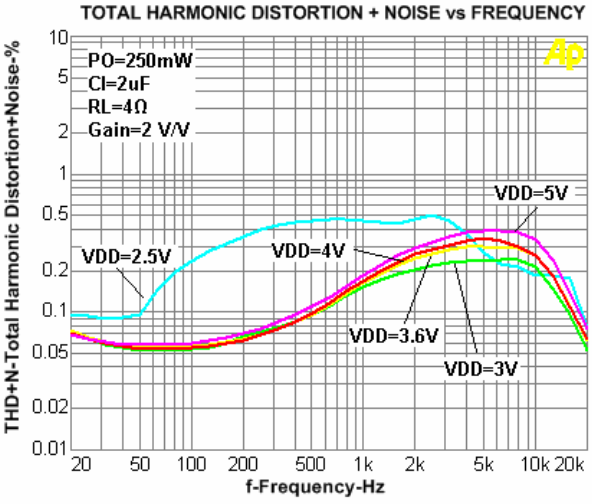

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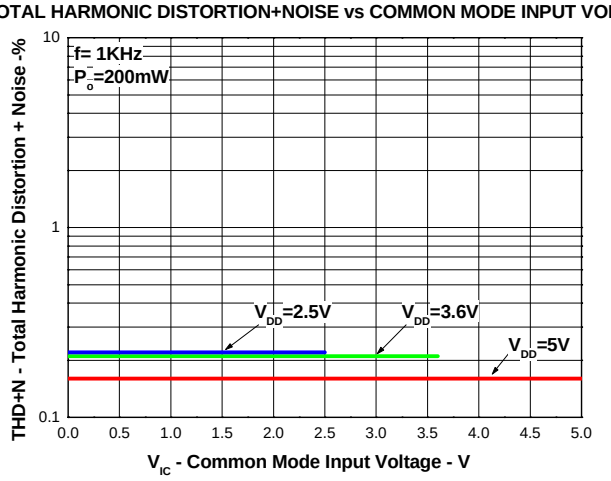

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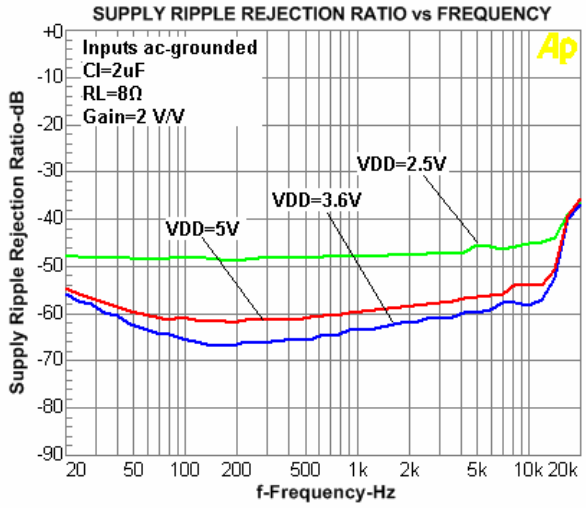

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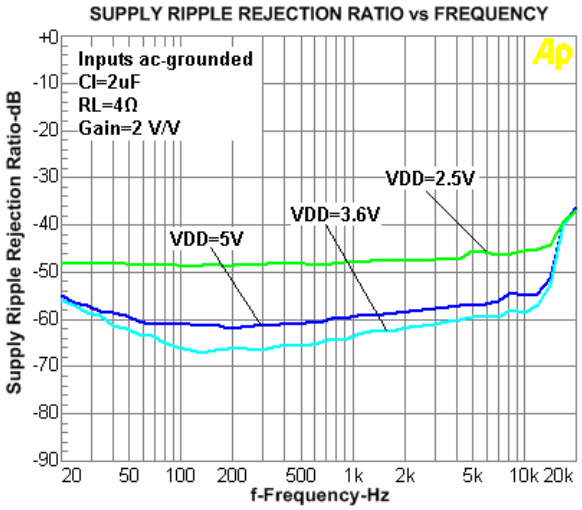

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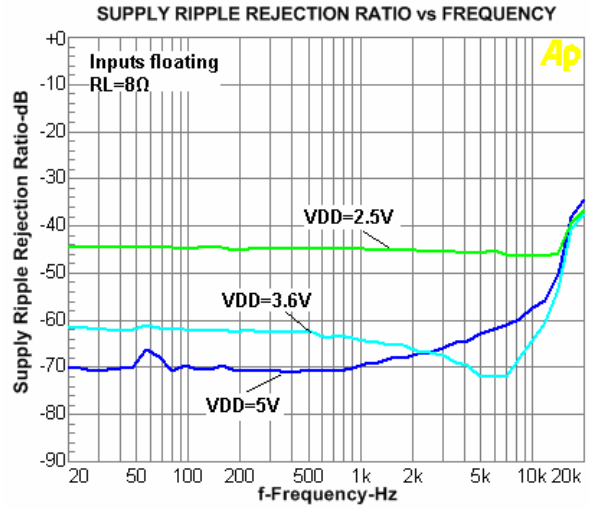

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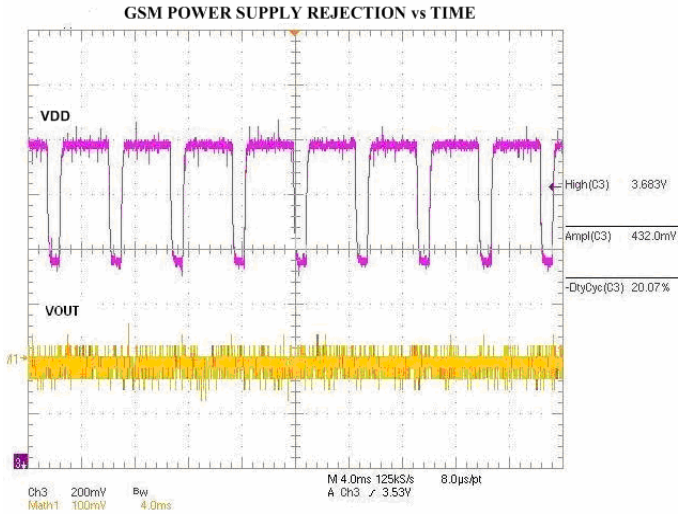

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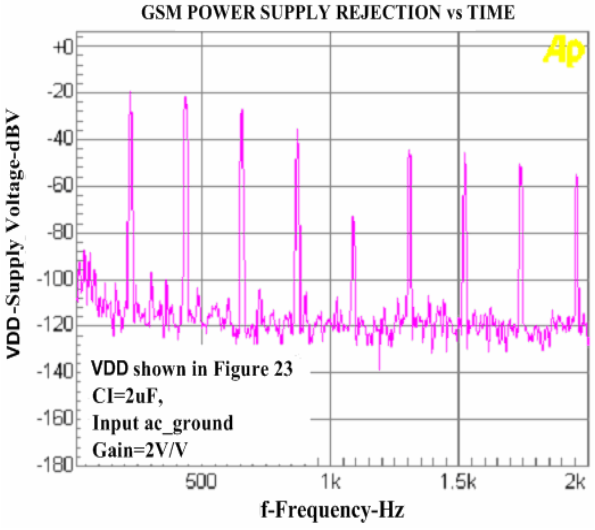

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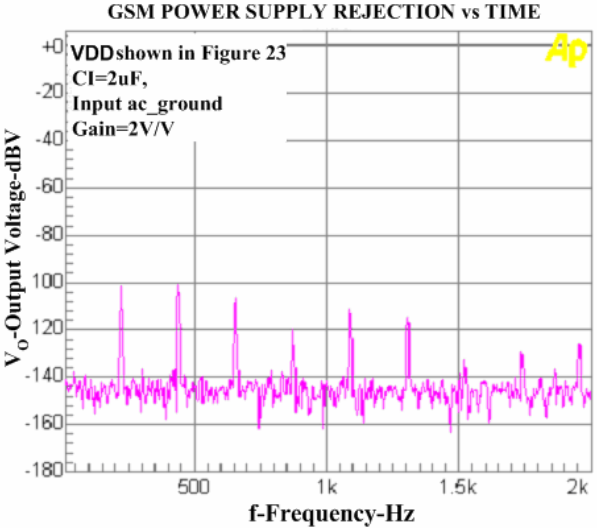

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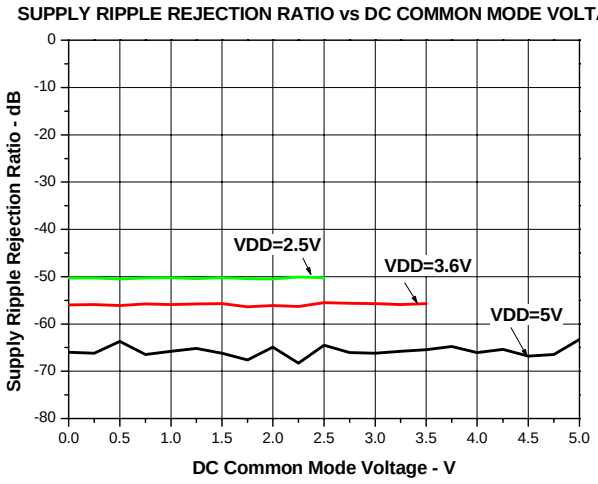

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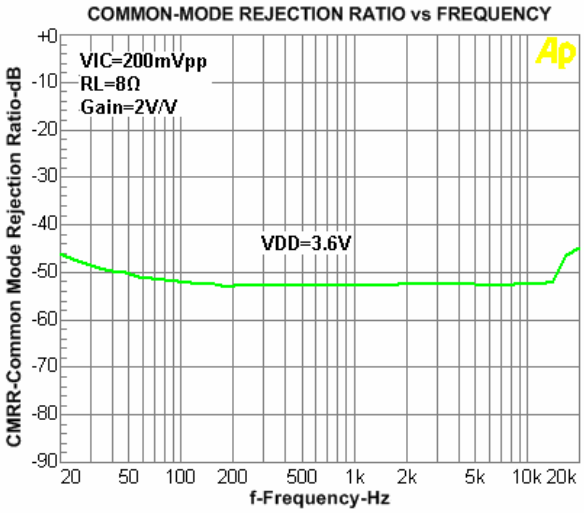

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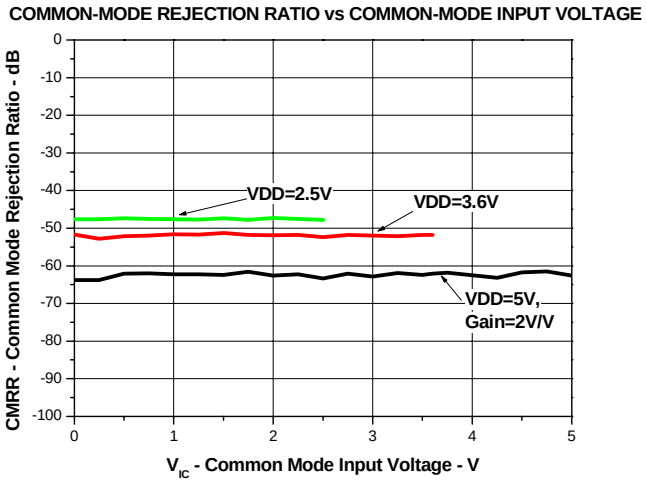

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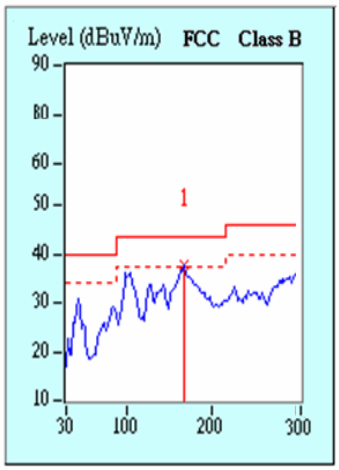


Figure29. EMI Test and FCC Limits

Application Information

Fully Differential Amplifier

The EUA2011 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential EUA2011 can still be used with a single-ended input; however, the EUA2011 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:

  - The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the EUA2011, the common-mode feedback circuit will adjust, and the EUA2011 outputs will still be biased at midsupply of the EUA2011. The inputs of the EUA2011 can be biased from 0.5V to V_{DD} − 0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.

- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:

  - The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.

- Better RF−immunity:

  -GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

Component Selection

Figure 30 shows the EUA2011 typical schematic with differential inputs and Figure 31 shows the EUA2011 with differential inputs and input capacitors, and Figure 32 shows the EUA2011 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

Table 1. Typical Component Values

REF DES	VALUE
R_I	150kΩ (± 0.5%)
C_S	1μF (+22%,-80%)
C_I (1)	3.3nF (± 10%)

(1) C_I is only needed for single-ended input or if V_{ICM} is not between 0.5 V and V_{DD} – 0.8 V. C_I = 3.3 nF (with R_I = 150 kΩ) gives a high-pass corner frequency of 321 Hz.

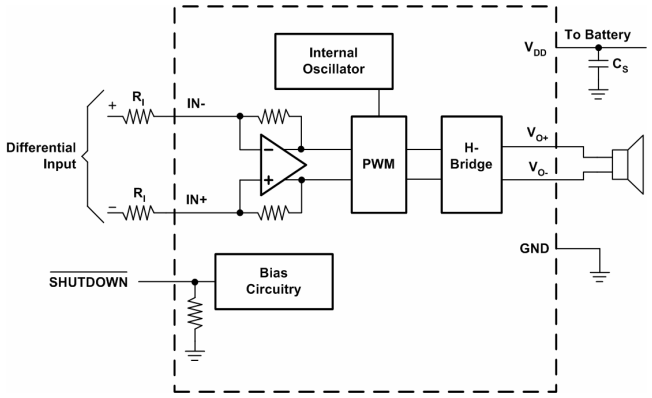


Figure 30. Typical Application Schematic with Differential Input for a Wireless Phone

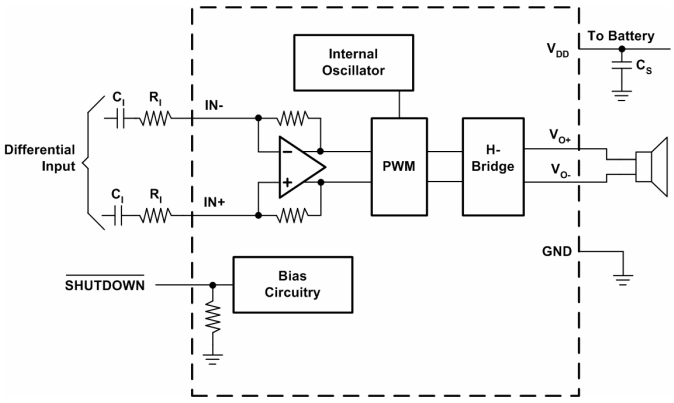


Figure 31. Typical Application Schematic with Differential Input and Input Capacitors

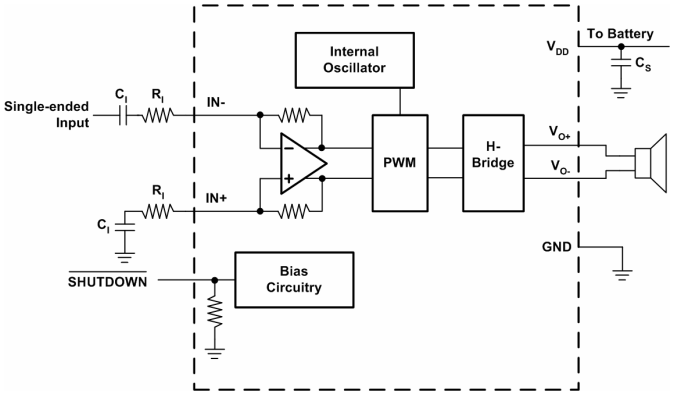


Figure 32. Typical Application Schematic with Single-Ended Input

Input Resistors (R_I)

The input resistors (R_I) set the gain of the amplifier according to equation (1).

$$\text{Gain} = \frac{2 \times 150\text{k}\Omega}{R_I} \left(\frac{V}{V}\right) \quad \text{----------(1)}$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.
Place the input resistors very close to the EUA2011 to limit noise injection on the high-impedance nodes.
For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the EUA2011 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

Decoupling Capacitor (C_S)

The EUA2011 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the EUA2011 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Input Capacitors (C_I)

The EUA2011 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} – 0.8 V (shown in Figure 31). If the input signal is not biased within the recommended common −mode input range, if needing to use the input as a high pass filter (shown in Figure 32), or if using a single-ended source (shown in Figure 33), input coupling capacitors are required.
The input capacitors and input resistors form a high-pass filter with the corner frequency, fc, determined in equation (2).

$$f_c = \frac{1}{(2\pi R_I C_I)} \quad \text{----------(2)}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.
Equation (3) is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi R_I f_c)} \quad \text{----------(3)}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.
For a flat low-frequency response, use large input coupling capacitors (1 μF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

Single-Ended Input Depop Function

In single-ended input application, there is an inherently voltage difference in input pairs when shutdown is released. In order to eliminate pop noise, the pop cancellation circuit need to charge the input capacitor C_I until fully-differential inputs are balanced and output power to load gradually.
The RC time constant should within the de-pop delay, if 150kΩ R_I is chosen, the recommended C_I should small than 10nF for a good pop immunity.

Summing Input Signals

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The EUA2011 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see equations (4) and (5), and Figure 33).

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left(\frac{V}{V}\right) \text{----------(4)}$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left(\frac{V}{V}\right) \text{----------(5)}$$

If summing left and right inputs with a gain of 1 V/V, use $R_{I1} = R_{I2} = 300\ k\Omega$.

If summing a ring tone and a phone signal, set the ring-tone gain to Gain 2 = 2 V/V, and the phone gain to Gain 1 = 0.1 V/V. The resistor values would be. . .

R_{I1}=3MΩ, and=R_{I2}=150kΩ

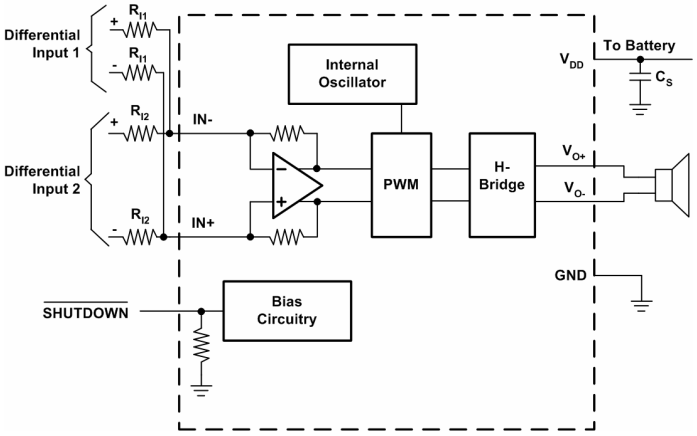


Figure 33. Application Schematic with EUA2011 Summing Two Differential Inputs

Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 34 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{I2}, shown in equation (8). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left(\frac{V}{V}\right) \text{---------- (6)}$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left(\frac{V}{V}\right) \text{----------(7)}$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \text{----------(8)}$$

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, the resistor values would be…

R_{I1}=3kΩ, and=R_{I2}=150kΩ

The high pass corner frequency of the single-ended input is set by CI2. If the desired corner frequency is less than 20 Hz...

$$C_{I2} > \frac{1}{(2\pi 150k\Omega 20Hz)}$$

$$C_{I2} > 53nF$$

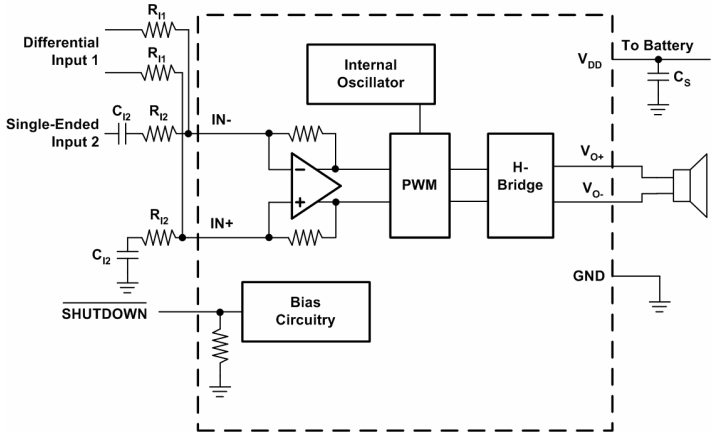


Figure 34. Application Schematic with EUA2011 Summing Input and Single-Ended Input Signals

Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (fc1 and fc2) for each input source can be set independently (see equations (9) through (12), and Figure 35). Resistor, RP, and capacitor, CP, are needed on the IN+ terminal to match the impedance on the IN− terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$Gain1 = \frac{V_O}{V_{I1}} = \frac{2 \times 150k\Omega}{R_{I1}} \left(\frac{V}{V}\right) \text{----------(9)}$$

$$Gain2 = \frac{V_O}{V_{I2}} = \frac{2 \times 150k\Omega}{R_{I2}} \left(\frac{V}{V}\right) \text{----------(10)}$$

$$C_{I1} = \frac{1}{(2\pi R_{I1} f_{c1})} \text{----------(11)}$$

$$C_{I2} = \frac{1}{(2\pi R_{I2} f_{c2})} \text{----------(12)}$$

$$CP = C_{I1} + C_{I2} \text{----------(13)}$$

$$R_P = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \text{---------- (14)}$$

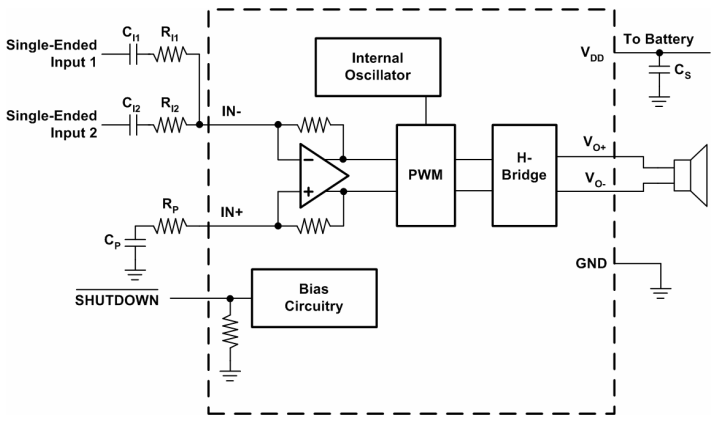


Figure 35. Application Schematic with EUA2011 Summing Two Single-Ended Input

PCB Layout

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the EUA2011 and the load results is lower output power and decreased efficiency. Higher trace resistance between the supply and the EUA2011 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasite capacitors that help to filter the power supply line.

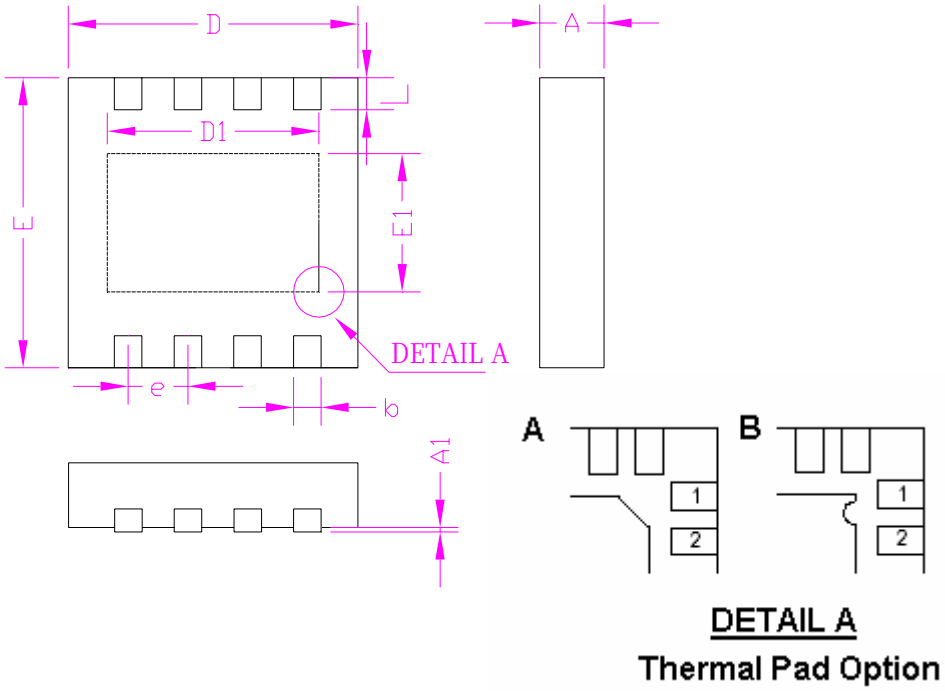
The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the EUA2011 and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.

Ferrite chip inductors placed close to the EUA2011 may be needed to reduce EMI radiation. The value of the ferrite chip is very application specific.

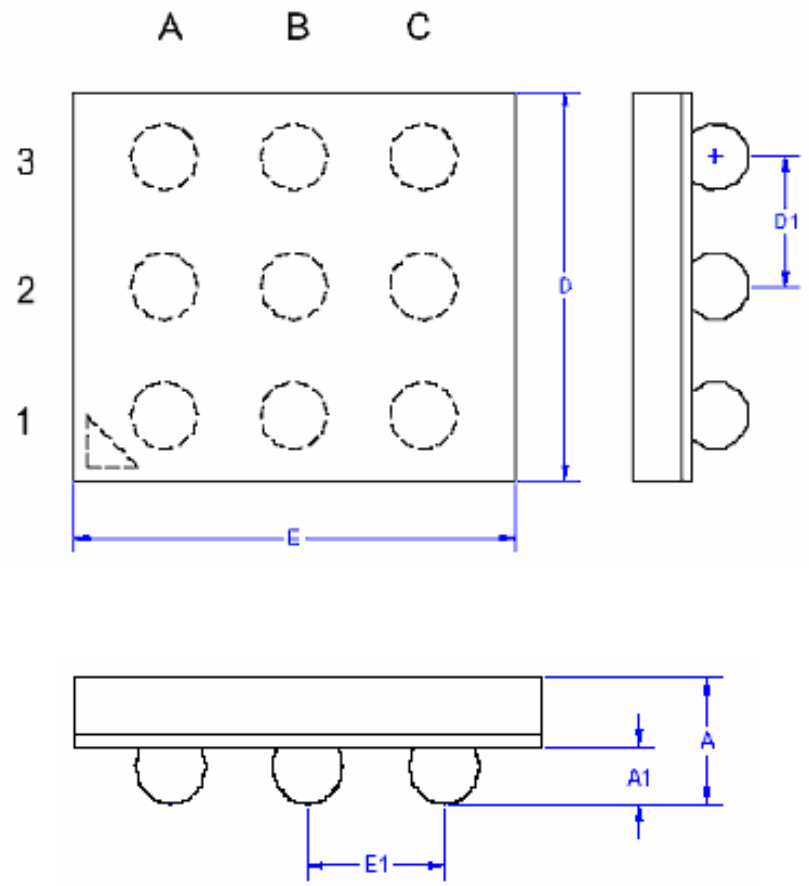
Packaging Information

TDFN-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.40	0.008	0.016
D	2.90	3.10	0.114	0.122
D1	2.30		0.090	
E	2.90	3.10	0.114	0.122
E1	1.50		0.059	
e	0.65		0.026	
L	0.25	0.45	0.010	0.018

WCSP-9



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	0.675	-	0.027
A1	0.15	0.35	0.006	0.014
D	1.45	1.55	0.057	0.061
D1	0.50		0.020	
E	1.45	1.55	0.057	0.061
E1	0.50		0.020	