FAIRCHILD SEMICONDUCTOR®

February 2008

FAN5078D3 — Complete ACPI Compliant Power Solution for DDR3 Memory System

Features

- PWM regulator for VDDQ
- Linear LDO regulator generates VTT = VDDQ/2, 1.5A peak sink/source capability
- AMT / M-state support
- Control to generate 5V USB
- ACPI drive and control for 5V DUAL generation
- 3.3V internal LDO for 3V-ALW generation
- 300kHz fixed-frequency switching
- $R_{DS(ON)}$ current sensing or optional current-sense resistor for precision over-current detect
- Internal synchronous boot diode
- Common Power-Good signal for all voltages
- Input under-voltage lockout (UVLO)
- Thermal shutdown
- Latched multi-fault protection
- Precision reference output for ULDO controllers
- 24-pin 5x5mm MLP package

Applications

- DDR VDDQ and VTT voltage generation with ACPI support for DDR3
- Memory Power Solutions for Desktop PCs
- Memory Power Solutions for Servers

Description

The FAN5078D3 DDR memory regulator combines a high-efficiency Pulse-Width Modulated (PWM) controller to generate the memory supply voltage, VDDQ, and a linear regulator to generate termination voltage (VTT).

FAN5078D3 can be configured to provide VDDQ and VTT power requirements for DDR3 version. For power requirements of DDR1 and DDR2 memory systems, refer to FAN5078.

Synchronous rectification provides high efficiency over a wide range of load currents. Efficiency is further enhanced by using the low-side MOSFET's $R_{DS(ON)}$ to sense current.

The VDDQ PWM regulator is a sampled, current-mode control with external compensation to achieve fast load-transient response and provide system design optimization.

The VTT regulator derives its reference and takes its power from the VDDQ PWM regulator output. The VTT termination regulator is capable of sourcing or sinking up to 1.5A peak currents.

In S5 M1 mode, the VDDQ switcher, VTT regulator, and the 3.3V regulators remain on. S3 mode keeps these regulators on and turns on an external P-channel to provide 5V USB.

A single soft-start capacitor enables controlled slew rates for both VDDQ and 3.3V-ALW outputs.

PGOOD becomes true in S0 only after all regulators have achieved stable outputs.

In S5 (EN = 0), the 3.3V internal LDO stays on while the other regulators are powered down.

Related Resources

Application Note AN-6005: Synchronous Buck MOSFET Loss Calculations with Excel Model

Application Note AN-6006: FAN5068/FAN5078D3 Components Calculations and Simulation Tools

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5078D3MPX	-10°C to +85°C	24-Lead, 5x5mm, Molded Leadless Package (MLP)	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Block Diagrams

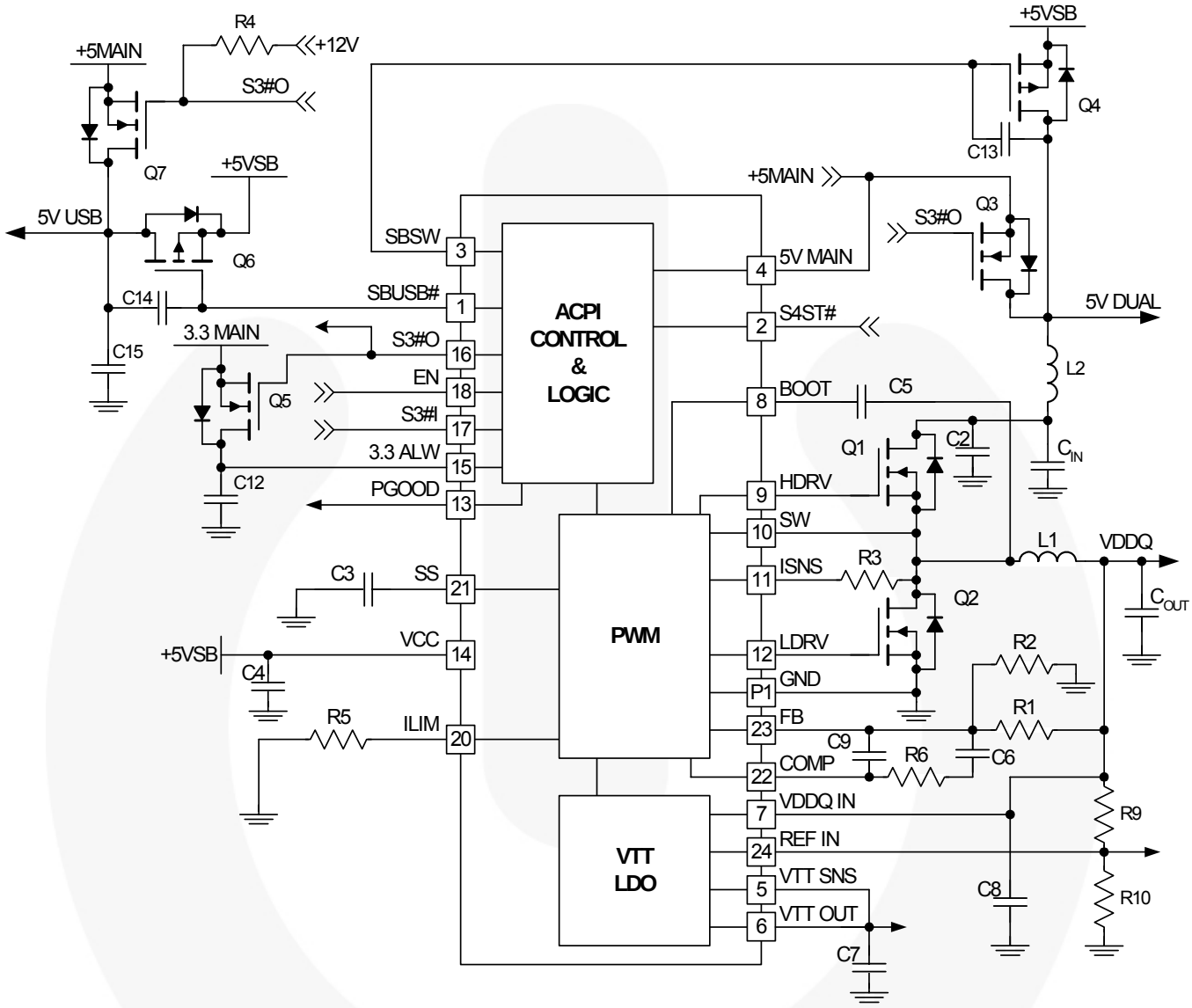


Figure 1. Typical DDR/ACPI System Regulation Schematic

Components are selected for a 15A VDDQ output.

Table 1. BOM for Figure 1

Ref.	Qty	Description	Mfg. and Part Number
Q1	1	NFET, V_{DS}=25V, DPAK V_{GS}=10V, I_D=35A, $R_{DS(ON)}$=6.5mΩ (Typ) V_{GS}=4.5V, I_D=35A, $R_{DS(ON)}$=9.1mΩ (Typ)	Fairchild Semiconductor FDD8780
Q2	1	NFET, V_{DS}=25V, DPAK V_{GS}=10V, I_D=35A, $R_{DS(ON)}$=6.5mΩ (Typ) V_{GS}=4.5V, I_D=35A, $R_{DS(ON)}$=9.1mΩ (Typ)	Fairchild Semiconductor FDD8780
Q3	1	NFET, V_{DS}=30V, DPAK V_{GS}=10V, I_D=35A, $R_{DS(ON)}$=7mΩ (Typ) V_{GS}=4.5V, I_D=35A, $R_{DS(ON)}$=9mΩ (Typ)	Fairchild Semiconductor FDD8880
Q4, Q6	2	PFET, 20V, 5.5A, 30mΩ, SSOT6	Fairchild Semiconductor FDC602P
Q5	1	NFET, 20V, 6.2A, 20mΩ, SSOT6	Fairchild Semiconductor FDC637AN
Q7	1	NFET, 30V, 30A, 22mΩ, DPAK	Fairchild Semiconductor FDD6612A
C12,C15	2	330µf, 10V, 20%, 110mΩ	
C13	1	10nf, 50V, 10%, X7R	
C14	1	3.3nf, 50V, 10%, X7R	
C2	1	4.7µf, 25V, 20%, X5R	
C4, C8	2	1.0µf, 10V, 10%, X5R	
C3, C5	2	0.1µf, 16V, 10%, X7R	
C6	1	4.7nf, 50V, 10%, X7R	
C7	1	820µf, 6.3V, 20%, 36mΩ	
C9	1	82pf, 50V, 5%, NPO	
CIN	4	1200µf, 6.3V, 20%, 18mΩ	
COUT	3	1200µf, 6.3V, 20%, 18mΩ	
L1	1	IND, 1.8µH, 16A, 3.2mΩ	Inter-Technical SC5018-1R8M
L2	1	IND, 470nH, 16A, 2.6mΩ	Inter-Technical SC2511-R47M
R1,R2,R3,R9,R10	5	1.21K, 1%	
R4	1	3.9K, 5%	
R5	1	71.5K, 1%	
R6	1	15.0K, 1%	

Contact a Fairchild Semiconductor representative for complete reference design and / or evaluation board.

Bypass Capacitor Notes:

1. Input capacitor C_{IN} is typically chosen based on the ripple current requirements. C_{OUT} is typically selected based on both current ripple rating and ESR requirement *(see AN-6006 for these calculations)*.
2. C7, C12, and C15 selection is largely determined by ESR and load transient response requirements. In each case, the number of capacitors required depends on the capacitor technology chosen. Oscons can meet the requirements with less space, but higher cost, than low-ESR electrolytics.

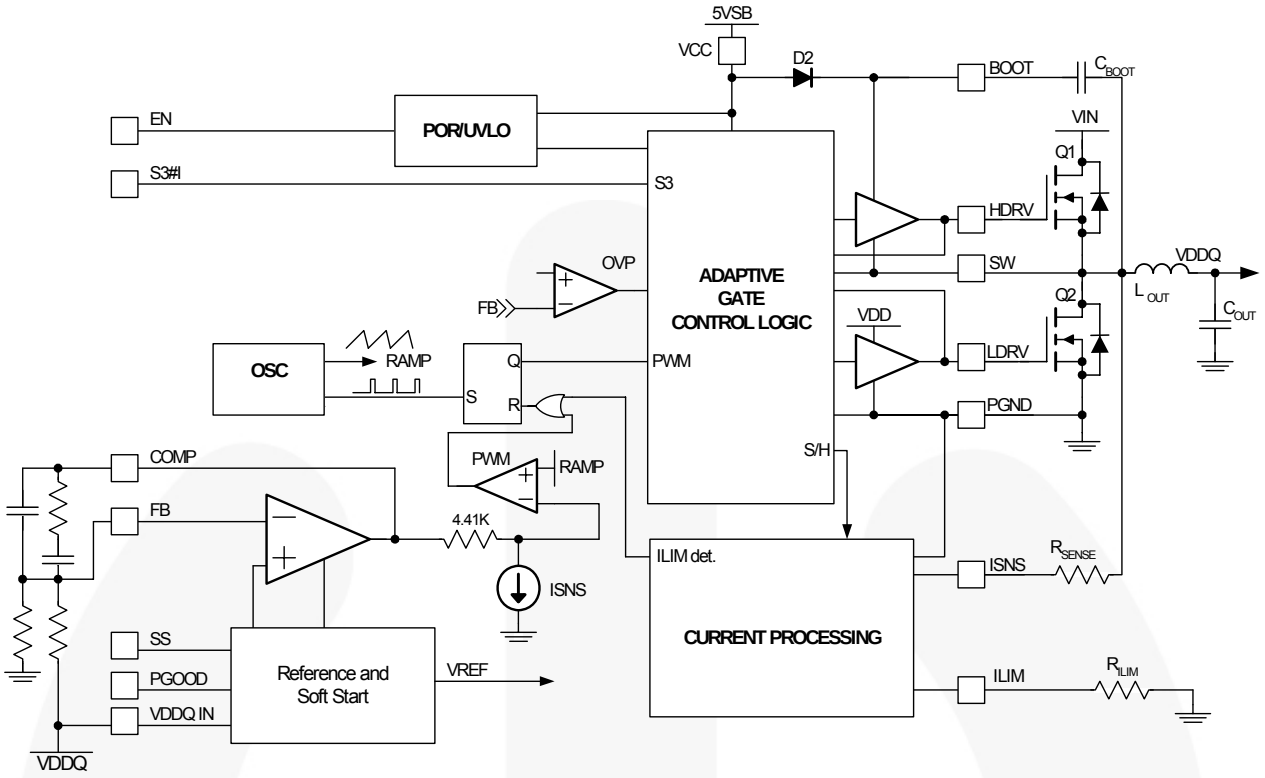


Figure 2. PWM Modulator Block Diagram

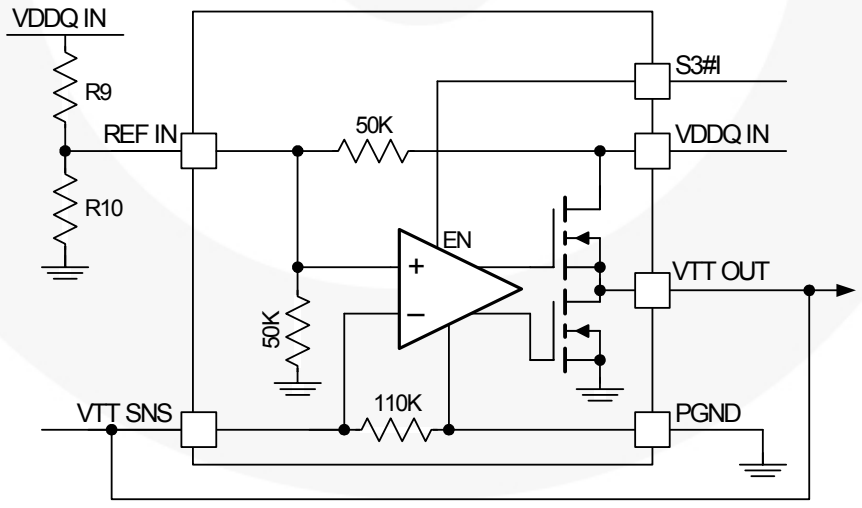


Figure 3. VTT Regulator Block Diagram

Pin Configuration

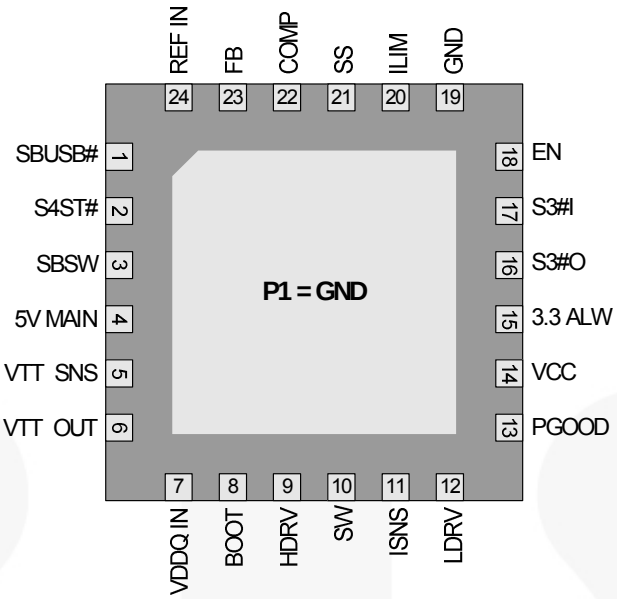


Figure 4. 5x5mm MLP Package (θ_{JA} = 38°C/W)
(Connect P1 pad to GND)

Pin Definitions

Pin #	Name	Description
1	SBUSB#	**USB Standby**. Pulls LOW with constant current to limit slew rate in S3 if S4ST# is HIGH. Drives a P-channel MOSFET to connect 5V SB to 5V USB.
2	S4ST#	**S4_STATE#** Connect to system logic signal that enables 5V USB power in S3.
3	SBSW	**Standby Switch**. Drives the P-channel MOSFET to power 5V DUAL from 5V SB when in S3. HIGH in S0 and S5.
4	5V MAIN	**5V MAIN**. When this pin is below 4.5V, transition from S3 to S0 is inhibited.
5	VTT SNS	**VTT** remote sense input.
6	VTT OUT	**VTT** regulator power output.
7	VDDQ IN	**VDDQ Input** from PWM. Connect to VDDQ output voltage. This is the VTT regulator power input.
8	BOOT	**Boot**. Positive supply for the upper MOSFET driver. Connect as shown in Figure 1. IC contains a boot diode to V_{CC}.
9	HDRV	**High-Side Drive**. High-side (upper) MOSFET driver output. Connect to gate of high-side MOSFET.
10	SW	**Switching Node**. Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and low-side MOSFET drain.
11	ISNS	**Current Sense Input**. Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback and current limiting.
12	LDRV	**Low-Side Drive**. The low-side (lower) MOSFET driver output. Connect to gate of low-side MOSFET.
13	PGOOD	**Power Good Flag**. An open-drain output that pulls LOW when FB is outside of a ±10% range of the 0.9V reference or the VTT output is < 80% or > 110% of its reference. PGOOD goes LOW when the IC is in the S5 state. The power-good signal from the PWM regulator enables the VTT regulator.

Pin Definitions (Continued)

Pin #	Name	Description
14	VCC	**VCC**. Provides IC bias and gate drive power. The IC is held in standby until this pin is above the UVLO threshold.
15	3.3 ALW	**3.3V LDO Output**. Internal LDO output. Turned OFF in S0; ON in S5 or S3.
16	S3#O	**S3#O Output**. Open-drain output that pulls the gate of the N-channel blocking MOSFETs LOW in S5 and S3. This pin goes HIGH (open) in S0.
17	S3#I	**S3 Input**. When LOW, turns off VTT and turns on the 3.3V regulator. Also causes S3#O to pull LOW to turn off blocking switch Q3, as shown in Figure 1. PGOOD is LOW when S3#I is LOW.
18	EN	**ENABLE**. Typically tied to the system logic signal S5#. When this pin is LOW, the IC is in a low quiescent current state, all regulators are OFF, and S3#O is LOW.
19, P1	GND	**GROUND** for the IC is tied to this pin and is also connected to P1.
20	ILIM	**Current Limit**. A resistor from this pin to GND sets the current limit.
21	SS	**Soft Start**. A capacitor from this pin to GND programs the slew rate of the PWM and all LDOs during initialization and transitions between states.
22	COMP	**COMP**. Output of the PWM error amplifier. Connect the compensation network between this pin and FB.
23	FB	**VDDQ Feedback**. The feedback from PWM output. Used for regulation as well as PGOOD, under-voltage, and over-voltage protection and monitoring.
24	REF IN	**VTT Reference**. Input that provides the reference for the VTT regulator. A precision internal divider from VDDQ IN (which can be overridden with external resistors) is provided.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter		Min.	Max.	Units
V_{CC}			6.5	V
SW, ISNS, HDRV, S3#O			28	V
BOOT to SW			6.5	V
SW, ISNS, HDRV to PGND	Continuous	-1	20	V
	Transient (t ≤ 100ns)	-5	20	V
All Other Pins		-0.3	Vcc+0.3	V
Junction Temperature (T_J)		-20	+150	°C
Storage Temperature		-65	+150	°C
Lead Soldering Temperature, 10 Seconds			+300	°C
I_{VTT} Peak (Duration < 2ms)		-1.5	+1.5	A
I_{VTT} RMS		-1.0	+1.0	A
ESD Rating, Human Body Model			1500	V
ESD Rating, Charged Device Model			1600	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage V_{CC}		4.5	5.0	5.5	V
I(3.3 ALW)				1.25	A
Ambient Temperature (T_A)		-10		+85	°C

Electrical Specifications

Recommended operating conditions; component values per Figure 1, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
Power Supplies						
V_{CC} Current	S0	LDRV, HDRV Open, FB forced above regulation point, I(VTT) = 0, EN=1, S3#I=1		15	24	mA
	S3	EN=1, S3#I = LOW, I(3.3) < 10mA		15	24	mA
	S5	EN=0, I(3.3) = 0		2	4	mA
V_{CC} UVLO Threshold		Rising V_{CC}	4.0	4.2	4.4	V
		Falling	3.9	4,1	4.3	V
		Hysteresis		0.15		V
5V MAIN UVLO Threshold		Rising	4.3	4.4	4.6	V
		Falling	3.9	4.1	4.2	V
		Hysteresis		0.30		V
5V MAIN Input Resistance		to GND	35	62		KΩ
Oscillator						
Frequency			255	300	345	KHz
Ramp Amplitude, pk–pk[1]				1.8		V
Ramp Offset				0.5		V
Reference and Soft Start						
Internal Reference Voltage at 25°C			0.891	0.900	0.909	V
Reference Temperature Coefficient				20	30	PPM/°C
I_{LIM} Reference Voltage		-2µA ≥ I_{ILIM} ≥ -18µA	0.882	0.900	0.918	V
Average Soft-Start Current (I_{SS})		Initial ramp after power-up		4.2		µA
		During PWM / LDO soft start		45		
SS Discharge Resistance		EN = 0		150		Ω
SS Complete Threshold				1.5		V
SS Complete Hysteresis				50		mV
PWM Converter						
Load Regulation		I_{OUT} from 0 to 15A	-2		+2	%
FB Bias Current			-1.8	-1.3	-0.8	µA
Under-Voltage Shutdown		as % of set point, 2µs noise filter	65	75	80	%
Over-Voltage Threshold		as % of set point	110	115	120	%
I_{SNS} Over-Current Threshold		R_{ILIM}= 56KΩ	-195	-170	-145	µA
VDDQ IN Discharge Resistance		EN = 0	20		55	Ω
COMP Source Current		V_{COMP} = 2.5V		650		µA
COMP Sink Current		V_{COMP} = 2.5V		100		µA
Error Amp GBW Product[1]				5.5		MHz
Error Amp DC Gain[1]				82		dB

Continued on the following page…

Electrical Specifications (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
PWM Output Driver					
HDRV Output Resistance	Sourcing		1.8	3.0	Ω
	Sinking		1.8	3.0	Ω
LDRV Output Resistance	Sourcing		1.8	3.0	Ω
	Sinking		1.2	2.0	Ω
PGOOD output					
Lower Threshold	as % of set point, 2µs noise filter	86		92	%
Upper Threshold	as % of set point, 2µs noise filter	108		115	%
PGOOD Output Low	I_{PGOOD} = 1.5 mA			0.5	V
Leakage Current	V_{PULLUP} = 5V			1	µA
3.3V LDO					
Regulation	I(3.3) from 0-1.25A, $V_{CC} \geq$ 4.75V	3.2	3.3	3.4	V
VTT Regulator					
VDDQ IN Current	S0 mode, I_{VTT}=0		35	70	mA
VREF IN to VTT Differential Output Voltage	I_{VTT} = 0, T_A=25°C	-20		20	mV
	I_{VTT} = ± 1.25A (pulsed)	-40		40	
VTT Current Limit	Pulsed (300ms maximum)(1)	±1.5	±3.0	±4.0	A
VTT Leakage Current	EN = LOW	-20		20	µA
VTT SNS Input Resistance	VTT SNS to GND		110		KΩ
VTT PGOOD Threshold	Measured at VTT SNS	80		110	% VTT REF
Drop-out Voltage	I_{VTT} = ±1.5A	-0.7		+0.7	V
Control Functions					
EN, S4ST# Input Threshold		1.00	1.25	1.55	V
S3#I Input Threshold		1.3	1.5	1.7	V
S3#I, EN, S4ST# Input Current		-1		1	µA
Over-Temperature Shutdown			150		°C
Over-Temperature Hysteresis			25		°C
S3#O Output Low $R_{DS(ON)}$			170	300	Ω
S3#O Output High Leakage	V(S3#O) = 12V		1	5	µA
SBSW Pull-down Resistance	5V MAIN OK		150	200	Ω
SBSW Pull-up Resistance			900	1200	Ω
SBUSB# Pull-down Resistance	5V MAIN OK		150	200	Ω
SBUSB# Pull-up Resistance			550	750	Ω
SBSW, SBUSB# Output Current	5V MAIN < UVLO		500		nA

Note:

1. Guaranteed by design and characterization; not tested in production.

Circuit Description

Overview

The FAN5078D3 provides five functions:

1. A general purpose PWM regulator, typically used to generate VDDQ for DDR Memory.
2. A low-dropout linear VTT regulator capable of sinking and sourcing 1.5A peak.
3. Control to generate 5V DUAL using an external N-channel to supply power from 5V MAIN in S0 and an external P-channel to provide power from 5V standby (5V SB) in S3.
4. Drive to generate 5V USB. This signal drives a P-Channel MOSFET to connect 5V USB to +5V SB in S3.
5. An internal LDO that regulates 3.3V-ALW in S3 mode from V_{CC} (5V SB). In S3 or S5, this regulator is capable of 1.25A peak currents with average currents limited by the thermal design of the PCB.

At initial power-up, or when transitioning from S5, the PWM regulator is disabled until 5V MAIN is above the UVLO threshold.

Table 2. ACPI States

STATE	EN (S5#)	S3#I	S4ST#	SBSW	SBUSB#	S3#O	VDDQ	VTT	3.3 ALW LDO	3.3 ALW	5V Dual	5V USB
S5	L	X	X	H	H	L	OFF	OFF	ON	LDO	OFF	OFF
S5 M1	H	L	L	L	H	L	ON	ON	ON	LDO	+5VSB	OFF
S3	H	L	H	L	L	L	ON	ON	ON	LDO	+5VSB	+5VSB
S0	H	H	X	H	H	H	ON	ON	OFF	3.3V MAIN	+5 MAIN	+5 MAIN

Regulator Sequencing

The VCC pin provides power to all logic and analog control functions of the regulator, including:

1. Power for the 3.3V regulator
2. LDRV gate driver current
3. HDRV boot diode charging current
4. The regulator analog control and logic.

This pin must be decoupled with a X5R ceramic capacitor (1μF or larger recommended) as close as possible to the VCC pin. After V_{CC} is above UVLO, the start-up sequence begins (see Figure 9).

UVLO on VCC discharges SS and resets the IC.

T0 to T3: After initial power-up, the IC ignores logic inputs for a period (T3-T0) of approximately:

$$T3 - T0 \approx 1.7 \bullet C_{SS} \quad (1)$$

where T3-T0 is in ms if C_{SS} is in nF. At T2 (about 2/3 of the way from T1 to T3), the 3.3V-ALW LDO is in regulation. The 3.3V LDO slew rate is limited by the discharge slope of CSS. If 3.3V MAIN has come up prior to this time, the 3.3V-ALW node is already pre-charged through the body diode of Q5 (see Figure 1).

T3 to T4: The IC starts VDDQ only if 5V MAIN is above the UVLO threshold (5V MAIN OK). Provided 5V MAIN is up before T3, the IC waits about 100μs before initiating soft-start on VDDQ to allow CSS time to fully discharge. The IC is in "SLEEP" or S5 state when EN is LOW. In S5, only the 3.3V LDO is ON. If the IC is in S5 at T4, CSS is held to 0V.

T4 to T5: After VDDQ is stabilized (when C_{SS} is at about ~1.3V), an internal VDDQ OK is generated that allows the VTT LDO to start. To ensure that the VDDQ output is not subjected to large transient currents, the VTT slew rate is limited by the slew rate of the SS cap. In addition, the VTT regulator is current limited. VTT is in regulation once C_{SS} reaches about 3.8V.

S0 to S3 or S5 M1: The system signals this transition by dropping the S3#I signal. When this occurs, S3#O goes LOW, and the 3.3V LDO turns on. SBSW pulls low to turn ON the P-channel 5V DUAL switch. SBUSB# pulls LOW to turn on Q6 when S4ST# is HIGH.

S3 or S5 M1 to S0: The system signals this transition by raising the S3#I signal. S0 mode is not entered until 5V MAIN OK, then the following occurs:

- S3#O releases.
- SBSW and SBUSB# both pull HIGH to turn off their P-channel switches.
- The 3.3V LDO turns off.

In most systems, the ATX power supply is enabled when S3#I goes HIGH. At that time, 5V and 3.3V MAIN starts to rise. When the FAN5078D3's 5V MAIN pin is above its UVLO threshold, Q3 and Q5 turn on. This can cause about a 10% "dip" in both 5V DUAL and 3.3V ALW when Q3 and Q5 turn on, since at that point, 5V MAIN and 3.3V MAIN are at 90% of their regulation value.

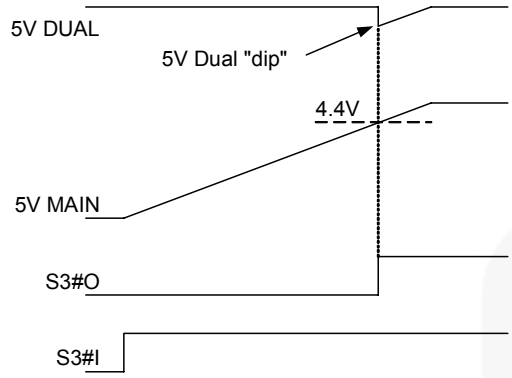


Figure 5. S3 to S0 Transition: 5V DUAL

This dip can also occur in 5V USB and 3.3V-ALW if 5V and 3.3V are not fully charged before the 5V MAIN pin exceeds its threshold. To eliminate the dip, add delay to the 5V MAIN pin, as shown below. The 5V MAIN pin does not supply power to the IC; it is only used to monitor the voltage level of the 5V MAIN supply. The pin has a pull-down resistor impedance of about 62K and therefore requires a low value R_{DLY} resistor *(see Figure 6 below)*.

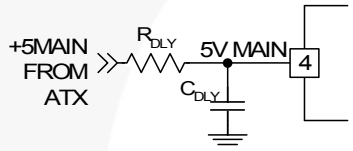


Figure 6. Adding Delay to 5V MAIN

Another method of eliminating the potential for this dip is to connect the ATX power supply PWR_OK signal to the 5V MAIN pin. Some systems cannot tolerate the long delay for PWR_OK (>100ms) to assert, so the solution in Figure 6 may be preferable.

If the PWR_OK signal is used, the voltage at the 5V MAIN pin must reach the 5V MAIN threshold. Since the internal pull-down resistance of the 5V MAIN pin is 62K, a low value pull-up should be used. A lower current solution can also be used by employing the 12V supply to provide adequate pull-up capability. The circuit in Figure 7 requires that PWR_OK, 12V, and +5MAIN from the ATX are all up before allowing the IC to go to S0.

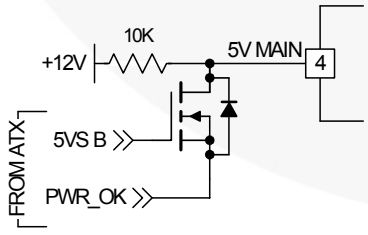


Figure 7. Using PWR_OK to Enable 5V MAIN

Care should also be taken to ensure that 3.3V-ALW does not glitch during the transition to S0. As shown in Figure 8, the 3.3V internal regulator turns off as soon as 5V MAIN crosses its rising threshold, releasing S3#O. While the gate capacitances of Q5, Q7, and Q3 charge sufficiently to turn Q5 ON, the load current on 3.3-ALW is supplied by C12. There is an initial "ESR step" of $I_{3.3}$ x ESR_{C12}, where $I_{3.3}$ is the 3.3-ALW load current. This is followed by a discharge of C12 whose slope is proportional to $\frac{I_{3.3}}{C12}$. To ensure that the drop in 3.3-ALW during this transition does not cause system problems, use sufficiently low-ESR capacitors and a sufficiently low value for R4 to ensure that 3.3-ALW remains inside the required system tolerance.

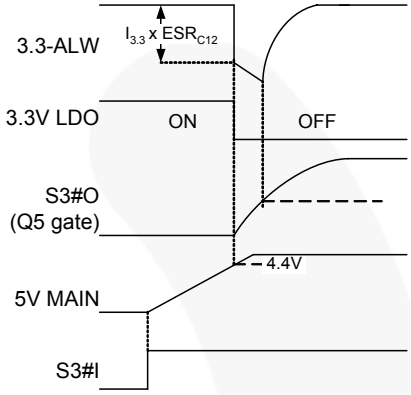


Figure 8. 3.3V-ALW Transition to S0

S5 to S5 M1 or S3: During S5 to S3 transition, the IC pulls SBSW (or SBUSB# if enabled by S4ST#) LOW with a 500nA current sink to limit inrush in Q4 if 5V MAIN is below its UVLO threshold. At that time, 5V DUAL and 5V USB are discharged. The limited gate drives control the inrush current through Q4 or Q6 as they charge their respective load capacitances on 5V DUAL and 5V USB, respectively. Depending on the C_{GD} of Q4 and Q6, the current available from 5V SB, and the size of C_{IN} and C15, C13, and C14 may be omitted.

$$I_{Q4(INRUSH)} = \frac{C_{IN} \bullet 5X10^{-7}}{C13 + C_{GD(Q4)}}$$
$$I_{Q6(INRUSH)} = \frac{C15 \bullet 5X10^{-7}}{C14 + C_{GD(Q6)}} \quad (2)$$

If 5V MAIN is above its UVLO threshold, SBSW (or SBUSB# if enabled by S4ST#) is pulled down with an impedance of ~150Ω. VDDQ and VTT do not start until 5V MAIN OK is true.

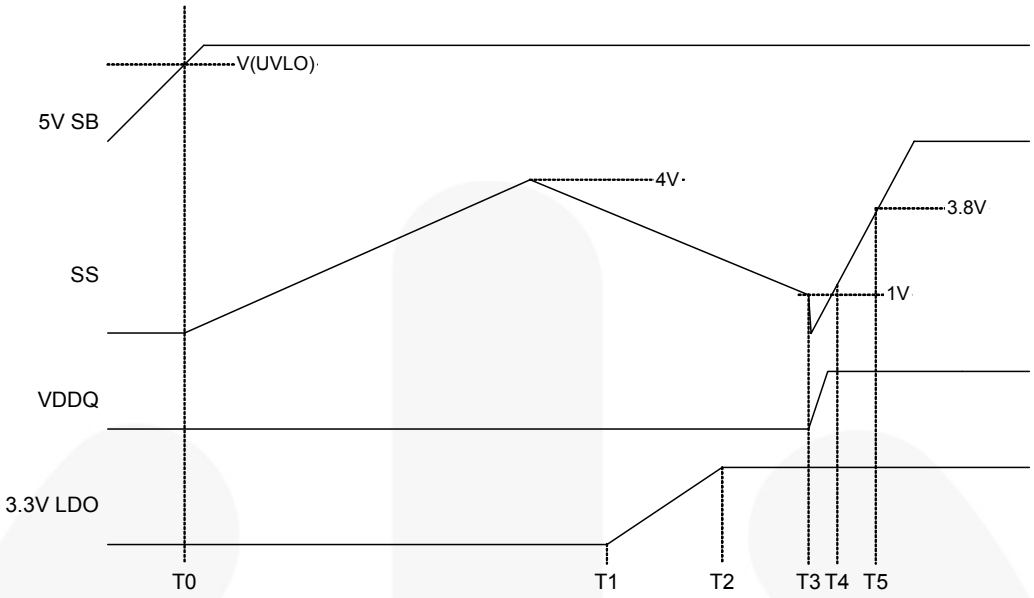


Figure 9. Start-up Sequence into S0

PWM Regulator

A PSPICE model and spreadsheet calculator are available in Application Note AN-6006 for the VDDQ PWM regulator to select external components and verify loop stability. The topics covered below provide the explanation behind the calculations in the spreadsheet.

Setting the Output Voltage

The output voltage of the PWM regulator can be set in the range of 0.9V to 80% of its power input by an external resistor divider.

The internal reference is 0.9V. The output is divided down by an external voltage divider to the FB pin (for example, R1 and R2 in Figure 1). There is also a 1.3μA current sourced out of FB to ensure that if the pin is open, VDDQ remains LOW. The output voltage therefore is:

$$\frac{0.9V}{R2} = \frac{V_{OUT} - 0.9V}{R1} + 1.3\mu A \quad (3a)$$

To minimize noise pickup on this node, keep the resistor to GND (R2) below 2K. In the example below, R2 is 1.82K and R1 is calculated:

$$R1 = \frac{R2 \bullet (V_{OUT} - 0.9)}{0.9 - 1.3\mu A} = 1.815K \approx 1.82K \quad (3b)$$

The synchronous buck converter is optimized for 5V input operation. The PWM modulator uses an average current mode control for simplified feedback loop compensation.

Oscillator

The oscillator frequency is 300Khz. The internal PWM ramp is reset on the rising clock edge.

PWM Soft Start

When the PWM regulator is enabled, the circuit waits until the VDDQ IN pin is below 100mV to ensure that the soft-start cycle does not begin with a large residual voltage on the PWM regulator output.

When the PWM regulator is disabled, 40Ω is connected from VDDQ IN to PGND to discharge the output. The circuit waits until the FB pin is below 100mV to ensure that the soft-start cycle does not begin with a large residual voltage on the VDDQ regulator output.

The voltage at the positive input of the error amplifier is limited to $V_{CSS,}$ which is charged with about 45μA. Once C_{SS} reaches 0.9V, the output voltage is in regulation.

The time it takes SS to reach 0.9V and VDDQ to achieve regulation is:

$$T_{0.9} \approx \frac{0.9 \, X \, C_{SS}}{45} \quad (4)$$

where $T_{0.9}$ is in ms if C_{SS} is in nF.

C_{SS} charges another 400mV before the PWM regulator's fault latch is enabled. When C_{SS} reaches 1.2V, the VTT regulator begins its soft-start. After VTT is in regulation, PGOOD is allowed to go HIGH (open).

Reference Output for ULDO Controllers

The ILIM pin (pin 20) may be used as a precision 0.9V reference for external ULDO controllers, as shown in Figure 10. The ILIM pin is ON during all ACPI states.

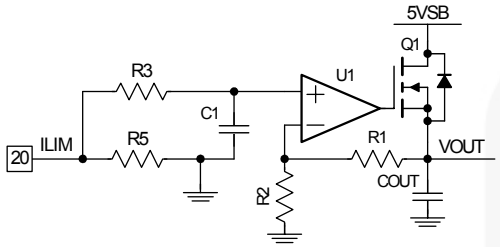


Figure 10. Using ILIM as a ULDO Reference

R5 in Figure 1 is the current limit setting resistor and comprises the only DC current path from the ILIM pin to GND. The circuit is configured so that the reference for the ULDO is presented at the positive terminal of U1 and draws negligible DC current. R3 and C1 filter noise that might be induced if there is significant PCB trace length. C1 should be placed as close as possible to the op-amp's input pin. R3 should be placed as close as possible to pin 20 of the FAN5078D3 and should be greater than 10K to isolate the ILIM pin from noise.

Recommended values for the circuit of Figure 10:

R3	50K
R5	*See AN-6006*
C1	1nF
R1, R2	Per desired V_{OUT}: $V_{OUT} = 0.9 \bullet \left(1 + \frac{R1}{R2}\right)$

Current Processing Section

The following discussion refers to Figure 11.

The current through R_{SENSE} resistor (I_{SNS}) is sampled shortly after Q2 is turned on. That current is held and summed with the output of the error amplifier. This effectively creates a current-mode control loop. R_{SENSE} sets the gain in the current feedback loop. For stable operation, the voltage induced by the current feedback at the PWM comparator input should be set to 30% of the ramp amplitude at maximum load current and line voltage.

Equation 5 estimates the recommended value of R_{SENSE} as a function of the maximum load current ($I_{LOAD(MAX)}$) and the value of the MOSFET $R_{DS(ON)}$:

$$R_{SENSE} = \frac{I_{LOAD(MAX)} \bullet R_{DS(ON)} \bullet 4.41K}{30\% \bullet 0.125 \bullet V_{IN(MAX)}} - 100 \quad (5)$$

where $R_{DS(ON)}$ is the maximum $R_{DS(ON)}$ of the low-side MOSFET at its maximum temperature.

R_{SENSE} must, however, be kept higher than:

$$R_{SENSE(MIN)} = \frac{I_{LOAD(MAX)} \bullet R_{DS(ON)}}{145\mu A} - 100 \quad (6)$$

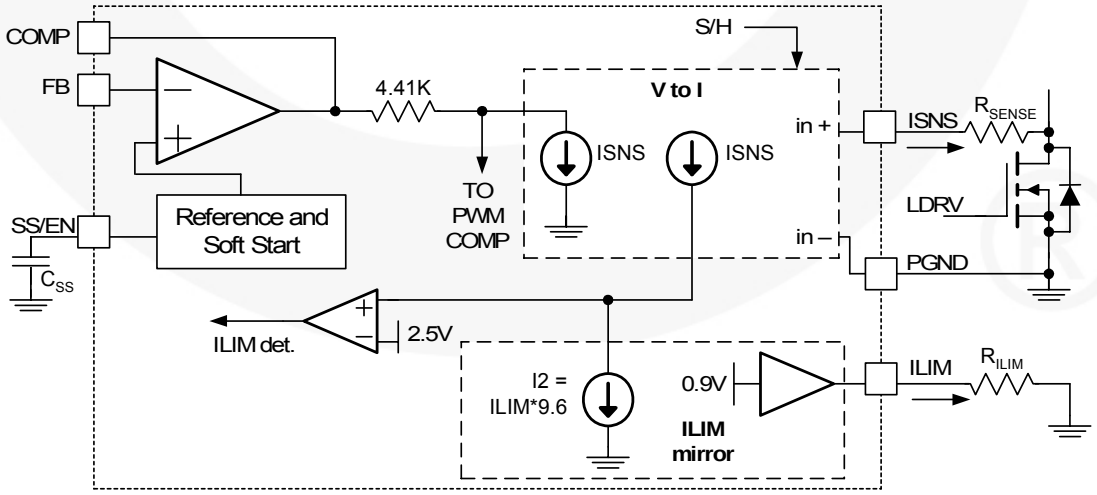


Figure 11. Current Limit / Summing Circuits

Setting the Current Limit

I_{SNS} is compared to the current established when a 0.9V internal reference drives the ILIM pin. R_{ILIM}, the $R_{DS(ON)}$ of Q2, and R_{SENSE} determine the current limit:

$$R_{ILIM} = \frac{9.6}{I_{LIMIT}} X \frac{(100 + R_{SENSE})}{R_{DS(ON)}} \quad (7)$$

where I_{LIMIT} is the peak inductor current. Since the tolerance on the current limit is largely dependent on the ratio of the external resistors, it is fairly accurate if the voltage drop on the switching node side of R_{SENSE} is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the I_{SNS}. This value not only varies from device to device, but also has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), so the actual current limit set point decreases proportional to increasing MOSFET die temperature. A factor of 1.6 in the current limit set point should compensate for MOSFET $R_{DS(ON)}$ variations, assuming the MOSFET heat sinking keeps its operating die temperature below 125°C.

Current limit (I_{LIMIT}) should be set sufficiently high as to allow the inductor current to rise in response to an output load transient. Typically, a factor of 1.3 is sufficient. In addition, since I_{LIMIT} is a peak current cut-off value, multiply $I_{LOAD(MAX)}$ by the inductor ripple current (i.e. 20%). To account all of these variations, set I_{LIMIT} as:

$$I_{LIMIT} > I_{LOAD(MAX)} \times 1.6 \times 1.3 \times 1.2 \quad (8)$$

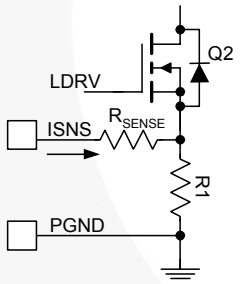


Figure 12. Improving Current Sensing Accuracy

More accurate sensing can be achieved using a resistor (R1) instead of the $R_{DS(ON)}$ of the FET, shown in Figure 12. This approach causes higher losses, but greater accuracy.

Gate Drive

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals, providing necessary amplification, level shifting, and shoot-through protection. It also has functions to help optimize the IC performance over a wide range of operating conditions.

Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than ~1V. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than ~1V. This allows a wide variety of upper and lower MOSFETs to be used without concern for simultaneous conduction or shoot-through.

There must be a low-resistance, low-inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path subtracts from the delay generated by the adaptive dead-time circuit and shoot-through may occur.

Frequency Loop Compensation

The loop is compensated using a feedback network around the error amplifier.

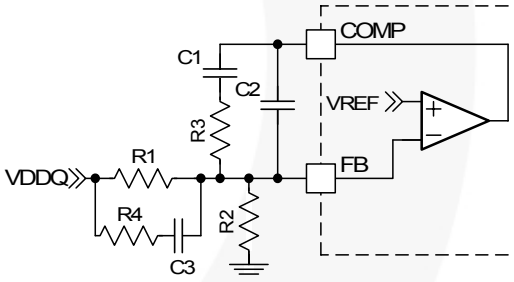


Figure 13. Compensation Network

Figure 13 shows a complete Type-3 compensation network. A Type-2 compensation configuration eliminates R4 and C3 and is shown in Figure 1. Since the FAN5078D3 architecture employs summing current mode, Type-2 compensation can be used for most applications. For critical applications that require wide loop bandwidth and use very low ESR output capacitors, Type-3 compensation may be required. The PSPICE model and spreadsheet calculator of AN-6006 can be used to calculate these component values.

Transient response during a rapid decrease in I_{LOAD} can be improved by adding a pull-down resistor (>5K) from the COMP pin to GND.

PGOOD Signal

PGOOD monitors the status of the PWM output and VTT. PGOOD remains LOW unless all these conditions are met:

- SS is above 3.5V
- Fault latch is cleared
- FB is between 90% and 110% of V_{REF}
- VTT is in regulation.

Protection

The converter output is monitored and protected against extreme overload, short-circuit, over-voltage, and under-voltage conditions.

An internal fault latch is set for any fault intended to shut down the IC. When the fault latch is set, the IC discharges its output by driving LDRV HIGH until VDDQ IN < 0.5V. LDRV goes LOW until VDDQ IN > 0.8V. This discharges VDDQ without causing undershoot (negative output voltage).

To discharge the output capacitors, a 40Ω load resistor is switched from VDDQ IN to PGND whenever the IC is in fault condition or when EN is LOW. After a latched fault, operation can be restored by recycling power or toggling the EN pin.

Under-Voltage Shutdown

If FB stays below the under-voltage threshold for 2μs, the fault latch is set. This fault is prevented from setting the fault latch during PWM soft-start (SS < 1.3V).

Over-Current Sensing

If the circuit's current limit signal (ILIM det shown in Figure 11) is high at the beginning of a clock cycle, a pulse-skipping circuit is activated and HDRV is inhibited. The circuit continues to pulse skip in this manner for the next 8 clock cycles. If, at any time from the 9th to the 16th clock cycle, the ILIM det is again reached, the fault latch is set. If ILIM det does not occur between cycle 9 and 16, normal operation is restored and the over-current circuit resets itself.

This fault is prevented from setting the fault latch during soft-start (SS < 1.3V).

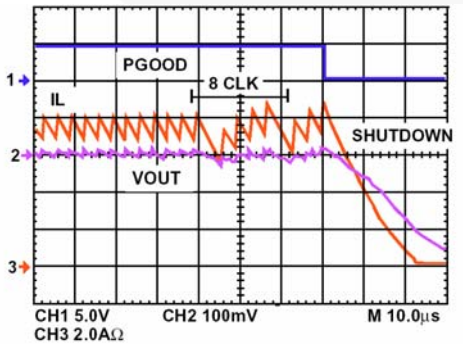


Figure 14. Over-Current Protection Waveforms

OVP / HS Fault / FB Short to GND Detection

A HS fault is detected when there is more than 0.5V from SW to PGND 350ns after LDRV reaches 4V (same as the current sampling time).

OVP fault detection occurs if FB>115% V_{REF} for 16 clock cycles.

During soft-start, the output voltage could potentially "run away" if either the FB pin is shorted to GND or R1 is open. This fault is detected if the following condition persists for more than 14μs during soft-start:

- VDDQ IN (PWM output voltage) > 1V
- FB < 100mV

Any of these faults sets the fault latch, even during the SS time (SS < 1.2V).

To ensure that FB pin open does not cause a destructive condition, a 1.3μA current source ensures that the FB pin is HIGH if open. This causes the regulator to keep the output LOW and eventually results in an under-voltage fault shutdown (after PWM SS completes).

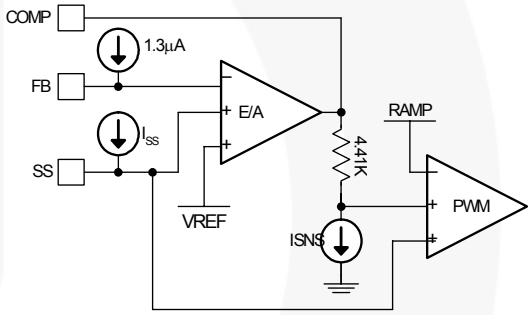


Figure 15. SS Clamp and FB Open Protection

Over-Temperature Protection

The chip incorporates an over-temperature protection circuit that shuts the chip down when a die temperature of ~150°C is reached. Normal operation is restored when the die temperature falls below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle. To accomplish this, the over-temperature comparator discharges the SS pin.

VTT Regulator Section *(see Figure 3)*

The VTT regulator includes an internal resistor divider (50K for each resistor) from the output of the PWM regulator. If the REF IN pin is left open, the divider produces a voltage 50% of VDDQ IN. Using a low-impedance external precision voltage divider produces greater accuracy.

The VTT regulator is enabled when S3#I is HIGH and the PWM regulator's internal PGOOD signal is true. The VTT regulator also includes its own PGOOD signal, which is HIGH when VTT SNS > 90% of REF IN.

Design Tools

AN-6006 provides a PSPICE model and spreadsheet calculator for the PWM regulator, simplifying external component selections and verifying loop stability.

The spreadsheet calculator can be used to calculate external component values for the FAN5078D3. The spreadsheet calculates compensation components that can be verified in the PSPICE model to ensure stability.

The PSPICE model in AN-6006 simulates both loop stability (Bode Plot) and transient analysis, and can be customized for a wide variety of applications and external component configurations.

As an initial step, define:

- Output voltage
- Maximum PWM output load current
- Maximum load transient current and maximum allowable output drop during load transient
- $R_{DS(ON)}$ of the low-side MOSFET (Q2)
- Maximum allowable output ripple.

Power MOSFET Selection

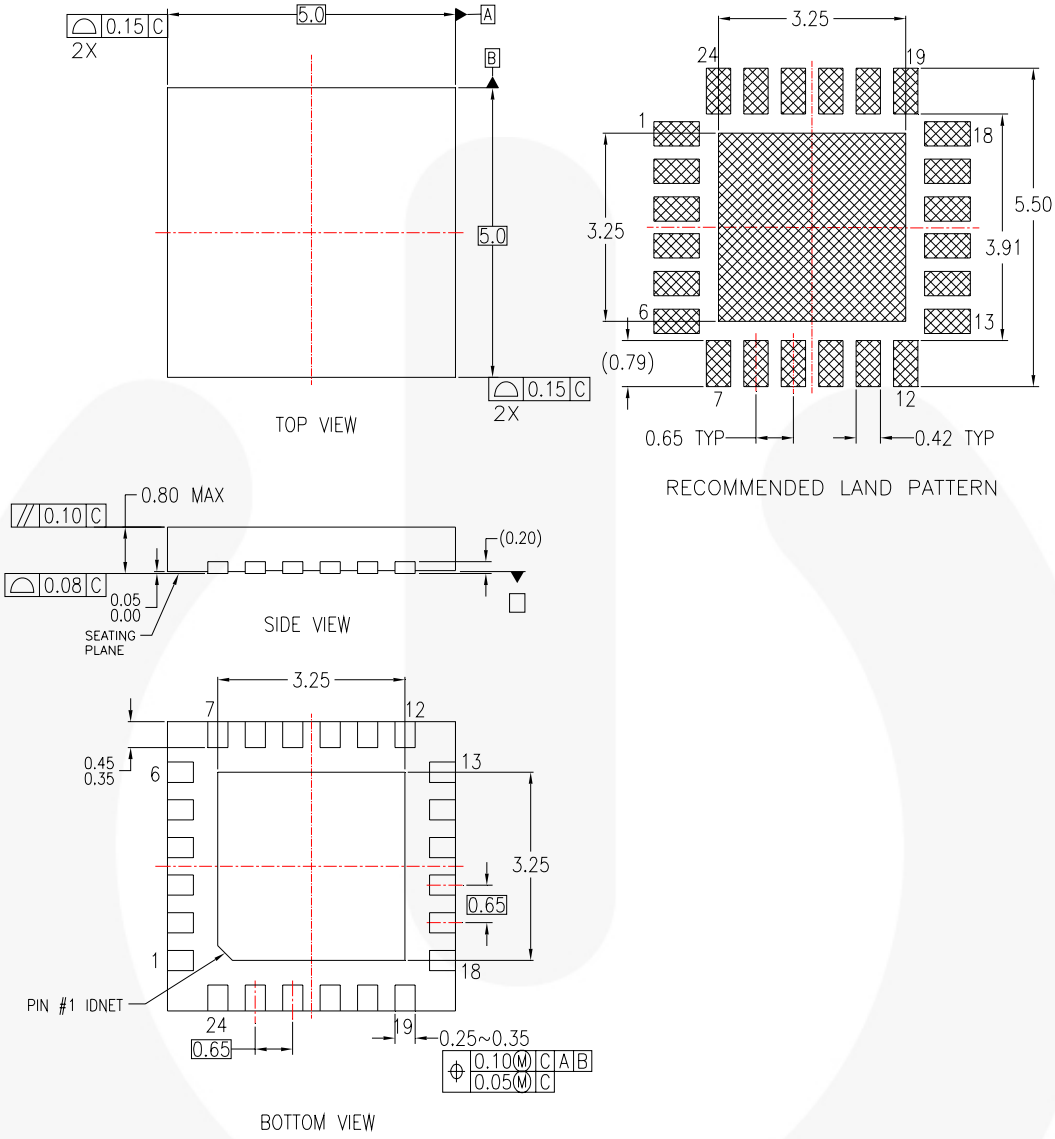
For a complete analysis of MOSFET selection and efficiency calculations, see Application Note *AN-6005: Synchronous Buck MOSFET Loss Calculations with Excel Model*.

3.3V and VTT LDO Output Capacitors

For stability, use at least 100µF for 3.3V-ALW bypass capacitor with a minimum ESR of 20mΩ.

The VTT output is typically bypassed with 820µF with at least 30mΩ ESR.

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHC, DATED AUG/2002
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP24ArevA

Figure 15. 24-Lead, 5x5mm, Molded Leadless Package (MLP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
EZSWITCH™ *
™
®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FlashWriter®*
FPS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
SYSTEM GENERAL ®
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™

* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33