FAIRCHILD SEMICONDUCTOR®

January 2007

FAN5336
1.5MHz Boost Regulator with 33V Integrated FET Switch

Features

- 1.5MHz Switching Frequency
- Low Noise
- Adjustable Output Voltage
- Up to 1.5A Peak Switch Current
- Low Shutdown Current: <1µA
- Cycle-by-Cycle Current Limit
- Over-Voltage Protection at the Feedback Pin
- Fixed-Frequency PWM Operation
- Soft-Start Capability
- Internal Compensation
- Thermal Shutdown
- Excellent Load Regulation: 0.2%
- Low Ripple
- 6-Lead 3x3mm MLP

Applications

- Portable Displays
- Mobile Phone / Smart Phone LED Backlights
- Display Bias
- PDA, DVD, Camcorder Backlights
- Pager and Cordless Phone Displays
- Portable Medical Diagnostic Equipment
- Remote Controls
- MP3 or PMP or DSC Players
- Serial Flash LED Drivers

Description

The FAN5336 is a high-efficiency, low-noise, fixed-frequency PWM, current-mode, DC-DC boost regulator. It is designed for small LCD bias supply and white LED backlight supply applications. Depending on the application, a FAN5336 regulator can output up to 33V at up to 50mA output current. With output voltage up to 21V, the output current can be up to 100mA. FAN5336 can be used for power conversion as low as 9V output voltage.

A current-mode control loop has a fast transient response that provides excellent load regulation within 0.2% of output voltage. The FAN5336 switches at fixed 1.5MHz frequency, allowing the use of small, low-cost external components. Constant frequency switching results in low input noise and small output capacitors. FAN5336 provides cycle-by-cycle current limiting up to 1.5A peak current.

The FAN5336 may be used to drive a serial flash LED with up to 100mA current at 21V for a maximum of 400ms on-time and 10% duty cycle.

A low-EMI mode reduces interference and radiated electromagnetic energy caused by the ringing of the inductor.

Additional features include thermal shutdown, over-voltage protection, cycle-by-cycle current limit, low ripple, and soft-start support.

The device is available in a 3x3mm 6-lead MLP, 0.8mm thickness package.

Application Diagram

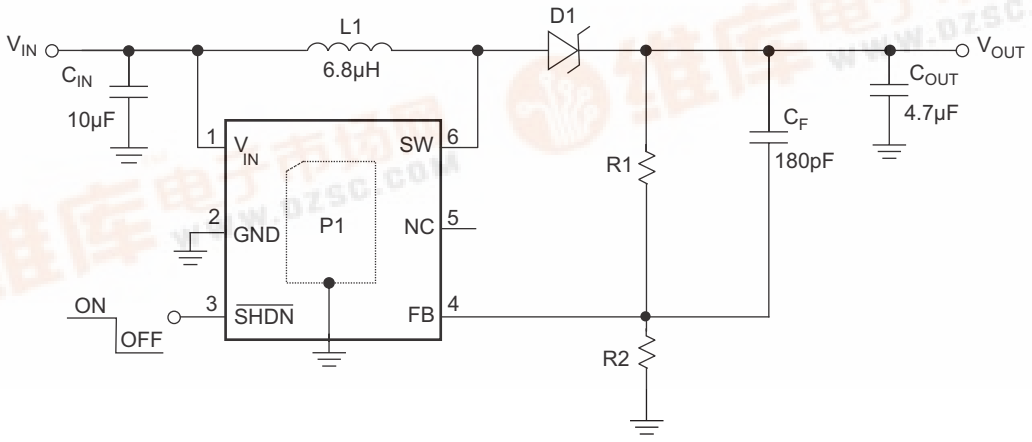


Figure 1. Typical Application Diagram

Ordering Information

Part Number	Package	Temperature Range	Pb-Free	Packing Method
FAN5336MPX	6-Lead 3x3mm MLP	-40°C to +85°C	Yes	Tape and Reel

Pin Assignments

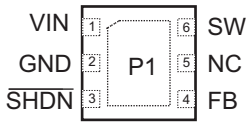


Figure 2. 6-Lead, 3x3mm MLP (Top View)

Pin Descriptions

Pin #	Name	Description
P1	GND	**Analog and Power Ground.** P1 must be soldered to the PCB ground.
1	V_{IN}	Input Voltage Pin.
2	GND	Ground.
3	$\overline{SHDN}$	**Shutdown Control Pin.** Logic HIGH enables, logic LOW disables the device.
4	FB	**Feedback Pin.** Feedback node that connects to an external voltage divider.
5	NC	No Connect.
6	SW	Switching Node.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbols	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN} to GND			6.0	V
	FB, $\overline{SHDN}$ to GND		-0.3	V_{IN} + 0.3	V
	SW to GND		-0.3	35	V
T_L	Lead Soldering Temperature (10 seconds)			300	°C
T_J	Junction Temperature			150	°C
T_{STG}	Storage Temperature		-55	150	°C
Θ_{JA}	Thermal Resistance			265	°C/W
ESD	Electrostatic Discharge Protection Level[1]	HBM	2		kV
		CDM	1		

Note:

1. Using EIA/JESD22A114B (Human Body Model) and EIA/JESD22C101-A (Charge Device Model).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbols	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Input Voltage	2.7		5.5	V
V_{OUT}	Output Voltage	9		33	V
T_A	Ambient Operating Temperature	-40	25	85	°C
C_{OUT}	Output Capacitance	2.2[2]		10	µF

Note:

2. This load capacitance value is required for loop stability. Tolerance, temperature variation, and voltage dependency of the capacitance must be considered. Typically a 4.7µF ceramic capacitor is required to achieve the specified value at V_{OUT} = 33V.

Electrical Characteristics

V_{IN} = 2.7 to 5.5V, $V_{\overline{SHDN}} = V_{IN}$, and T_A = -40°C to +85°C. Typical values are at T_A = 25°C and V_{IN} = 3.6V unless otherwise noted.

Parameter	Conditions Refer to the Test Circuit in Figure 3.	Min.	Typ.	Max.	Units
Output Voltage Accuracy	V_{IN} = 3.6V	-3		+3	%
Switch Current Limit	V_{IN} = 3.2V	1.1	1.5	1.8	A
Load Current	V_{OUT} = 21V ±5%, $V_{IN} \geq$ 3.0V	75			mA
	V_{OUT} = 21V ±5%, $V_{IN} \geq$ 3.2V, T_{ON} < 0.4s, T_{OFF} > 3.6s	100			
Switch On-Resistance	V_{IN} = 3.6V		0.4		Ω
Quiescent Current	No Switching, $V_{FB} \geq$ 1.27V		0.7		mA
	Switching		6.5		
OFF Mode Current	$V_{\overline{SHDN}}$ = 0V		0.1	3.0	µA
Shutdown Threshold	Device ON	1.5			V
	Device OFF			0.5	
Shutdown Pin Bias Current	$V_{\overline{SHDN}}$ = 0V or $V_{\overline{SHDN}}$ = 5.5V		1	10	nA
Feedback Voltage (V_{REF})	I_{Load} = 0mA, V_{IN} = 3.6V at 25°C	1.205	1.230	1.255	V
Feedback Pin Bias Current			1	10	nA
Feedback Voltage Line Regulation(3)	3.0V < V_{IN} < 5.5V, I_{LOAD} = 0mA		0.4	1.5	%/V
Switching Frequency		1.15	1.50	1.85	MHz
Maximum Duty Cycle		87	93		%
Start-up Turn-on Time	V_{IN} = 3.0V, I_{OUT} = 75mA		3.0	5.0	ms
Load Regulation	V_{IN} = 3.6V, 1mA < I_{Load} <100mA		0.2		%
Switch Leakage Current	No Switching, V_{IN} = 5.5V			1	µA

Note:
3.The line regulation is calculated based on $\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{1}{V_{OUT}}$.

Test Circuit

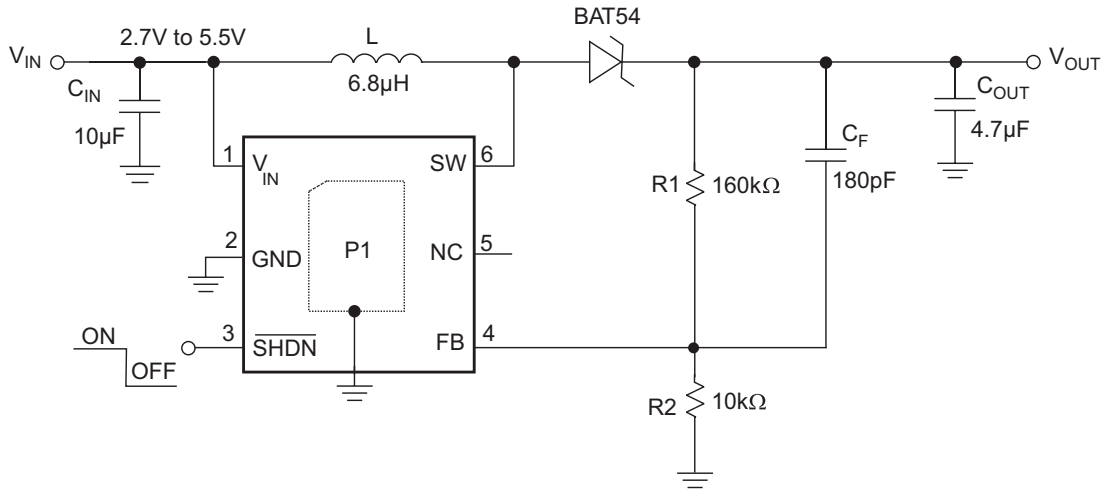


Figure 3. Test Circuit

Typical Performance Characteristics

V_{IN}=3.6V, V_{OUT}=21V, T_A=25°C, C_{IN}=10µF, C_{OUT}=4.7µF, L=6.8µH, C_F=180pF, R_1=160kΩ, R_2=10kΩ unless otherwise noted.

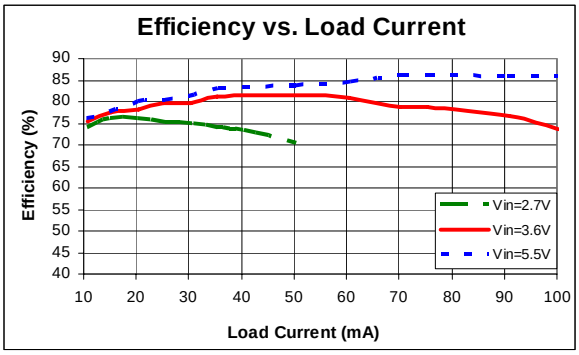


Figure 4. Efficiency vs. Load Current

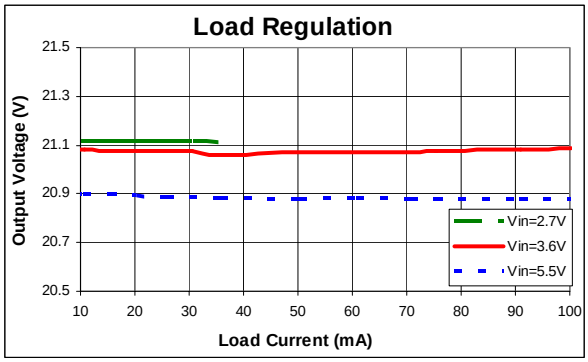


Figure 5. Load Regulation

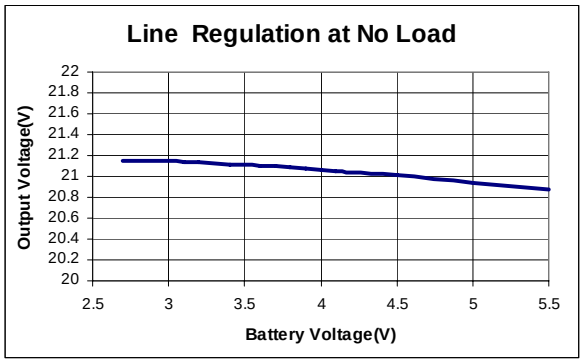


Figure 6. Line Regulation at No Load

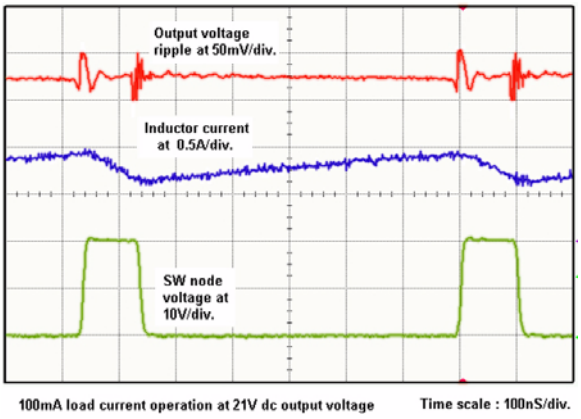


Figure 7. 100mA Load Current Operation

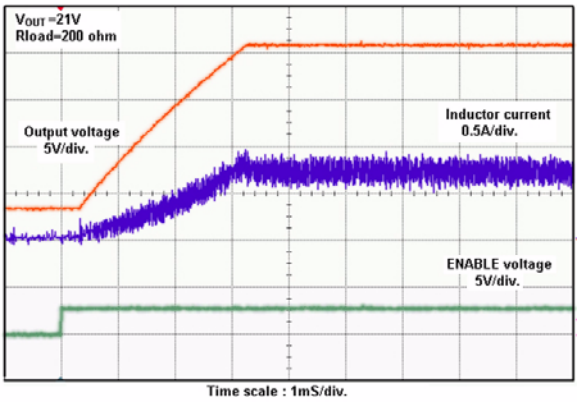


Figure 8. Start-up Response

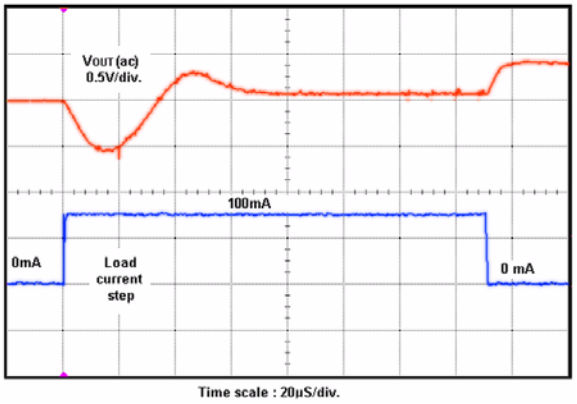


Figure 9. Load Transient Response

Block Diagram

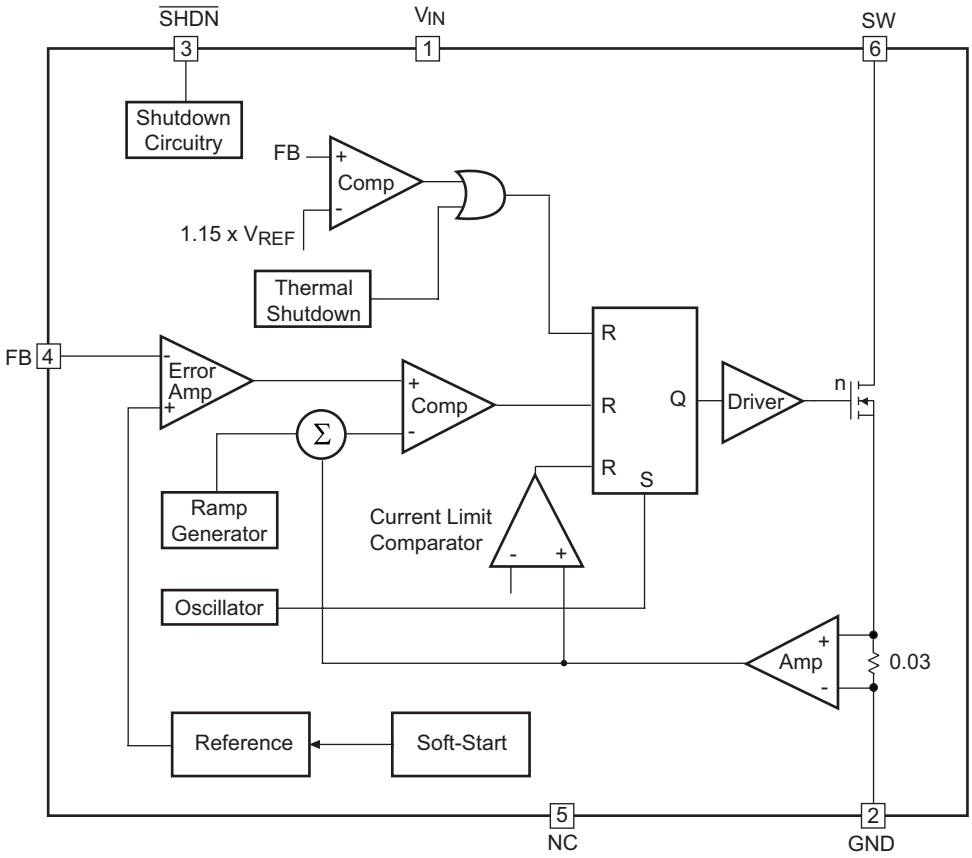


Figure 10. Block Diagram

Circuit Description

The FAN5336 is a pulse-width modulated (PWM) current-mode boost converter. The FAN5336 improves the performance of battery-powered equipment by significantly minimizing the spectral distribution of noise at the input caused by the switching action of the regulator. To facilitate effective noise filtering, the switching frequency was chosen to be high, 1.5MHz. An internal soft-start circuit minimizes in-rush currents. The timing of the soft-start circuit was chosen to reach 95% of the nominal output voltage within 5ms following an enable command when V_{IN} = 2.7V, V_{OUT} = 21V, I_{LOAD} = 35mA and $C_{OUT\ (EFFECTIVE)}$ = 4.7µF.

The device architecture is a current-mode controller with an internal sense resistor connected in series with the N-channel switch. The voltage at the feedback pin tracks the output voltage at the cathode of the external Schottky diode (shown in the test circuit in Figure 3). The error amplifier amplifies the difference between the feedback voltage and the internal bandgap reference. The amplified error voltage serves as a reference voltage to the PWM comparator. The inverting input of the PWM comparator consists of the sum of two components: the amplified control signal received from the 30mΩ current sense resistor and the ramp generator voltage derived from the oscillator. The oscillator sets the latch and the latch turns on the FET switch. Under normal operating conditions, the PWM comparator resets the latch and turns off the FET, terminating the pulse. Since the comparator input contains information about the output voltage and the control loop is arranged to form a negative feedback loop, the value of the peak inductor current is adjusted to maintain regulation.

Every time the latch is reset, the FET is turned off and the current flow through the switch is terminated. The latch can be reset by other events as well, such as over-current and over-voltage conditions. Over-current condition is monitored by the current-limit comparator, which resets the latch and turns off the switch within each clock cycle. An over-voltage condition at the feedback (FB) pin is detected by a fast comparator limiting the duty cycle in a similar manner to over-current monitoring.

Applications Information

Setting the Output Voltage

The internal feedback voltage reference (V_{REF}) is 1.23V (typical). The output voltage is divided by a resistor divider, R_1 and R_2 to the FB pin. The output voltage is calculated by:

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \quad \text{EQ 1}$$

The maximum output current depends on the output voltage settings. Table 1 provides the recommended voltage for several steady-state configurations:

Table 1: Recommended Voltages

V_{OUT} (V)	I_{LOAD} Max. (mA)	R_1 (kΩ) for R_2 = 10kΩ	V_{IN} Range (V)
9	50	63.2	2.7 to 5.5
9	170	63.2	2.9 to 4.7
12	125	87.5	2.7 to 5.5
21	75	160	3.6 to 5.5
33	50	258	4.0 to 5.5
33	10	258	2.7 to 5.5

Inductor Selection

The inductor parameters directly related to device performance are saturation current and DC resistance. The FAN5336 operates with a typical inductor value of 6.8µH. The lower the DC resistance, the higher the efficiency. Balancing inductor size, cost, and overall efficiency allows optimum choice.

The inductor saturation current should be rated around 1.5A, which is the threshold of the internal current limit circuit. This limit is reached only during the start-up and with heavy load conditions. When this occurs, the converter can shift into discontinuous conduction mode due to the automatic turn-off of the switching transistor, resulting in higher ripple and reduced efficiency.

Table 2: Recommended Inductors

Inductor Value	Vendor	Part Number	Comment
6.8µH	TDK	SLF7028T6R8M1R3	Lower Profile
6.8µH	Murata	LQS66C6R8M04	Higher Efficiency

Capacitors Selection

For best performance, low-ESR input and output capacitors are required. Ceramic capacitors of C_{IN} = 10µF and C_{OUT} = 4.7µF, placed as close as possible to the IC pins, are recommended for the lower input and output ripple. The output capacitor voltage rating should be selected according to the V_{OUT} setting.

Table 3: Recommended Capacitors

Cap. Value	Vendor	Part Number
10µF	Murata	GRM31CR70J106KA01B
4.7µF	Murata	GRM32RR61E475KC31B

A feedforward capacitor (C_F) is required for stability. The recommended value is around 180pF.

Diode Selection

The external diode used for rectification is usually a Schottky diode. Its average forward current should exceed the load current and its reverse voltage maximum ratings should exceed the voltage at the output of the converter. A barrier Schottky diode, such as BAT54, is preferred due to its low reverse current over the temperature range.

Care should be taken to avoid any short circuit of V_{OUT} to GND, even with the IC disabled, since the diode can be instantly damaged by the excessive current.

Flash LED Driver

The FAN5336 may be used to drive a serial flash LED with up to 100mA current at 21V for a maximum of 400ms on-time and 10% duty cycle.

Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and remains in effect until the die cools to 130°C, when the circuit is allowed to restart.

PCB Layout Recommendations

The inherently high peak currents and switching frequency of power supplies require careful PCB layout design. For best results, use wide traces for high-current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. The resistor divider that sets the output voltage should be routed away from the inductor to avoid RF coupling. A four-layer PCB, with at least one ground plane connected to Pin 2 of the IC, is recommended. The ground plane acts as an electromagnetic shield to reduce EMI and parasitic coupling between components.

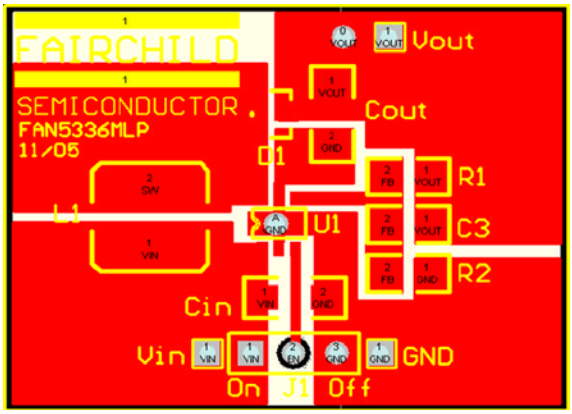
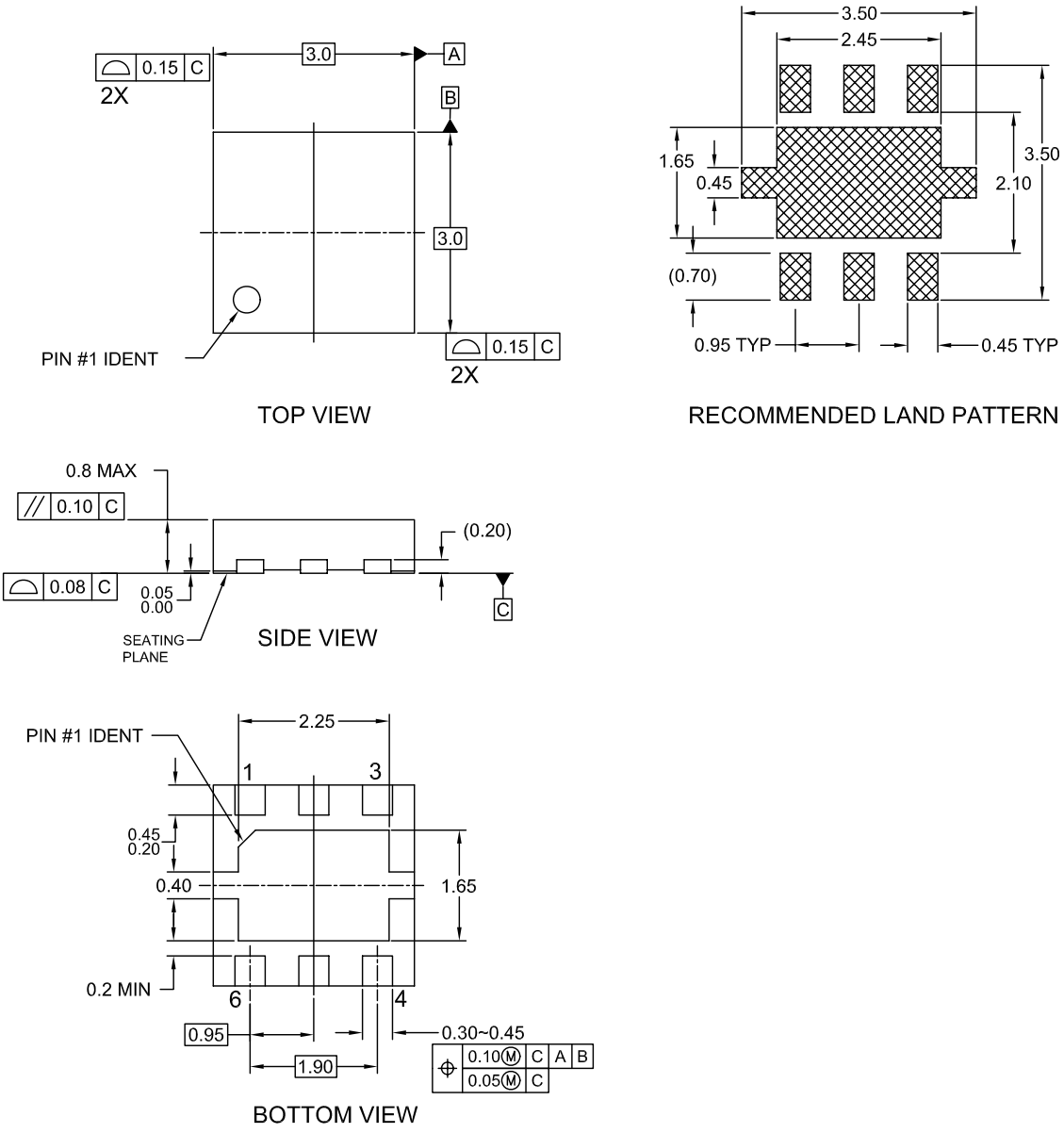


Figure 11. Recommended PCB Layout

Mechanical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229,
VARIATION WEEA, DATED 11/2001
EXCEPT FOR DAP EXTENSION TABS

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 1994

MLP06FrevA

Figure 12. 6-Lead 3x3 MLP

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EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
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Definition of Terms

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