QLogic Corporation

FAS209 Fast Architecture SCSI

Data Sheet

Features

- Compliance with ANSI SCSI-2 standard X3.131-1994 and SCSI-1
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Synchronous data transfers up to 10 Mbytes/sec fast SCSI and 5 Mbytes/sec normal SCSI
- Asynchronous data transfers up to 7 Mbytes/sec
- Up to 12 Mbytes/sec DMA burst transfer rate
- Clock rates up to 40 MHz
- Supports hot plugging
- Programmable active negation
- Low-input capacitance
- Programmable split-bus architecture
- DMA interface options
- Two bus configurations
- On-chip, 48-mA, single-ended drivers and receivers
- Parity pass-through on FIFO data
- Initiator and target roles
- SCSI sequences implemented without microprocessor intervention
- Part-unique ID code
- Eight-bit, single-ended SCSI operations

Product Description

The FAS209 is a high-performance SCSI interface chip designed to maximize transfer rates over the SCSI bus. It is the enhanced SCSI follow-on to QLogic's FAS216 SCSI processor chip, adding active negation and SCAM to the FAS216 design. The FAS209 supports bidirectional, single-ended SCSI operations. The block diagram of the FAS209 is illustrated in figure 1.

The FAS209 maximizes transfer rates by sustaining asynchronous data rates of up to 7 Mbytes/sec and fast, synchronous data transfer rates of 10 Mbytes/sec. The normal 5 Mbytes/sec synchronous transfer rate is also supported. With its on-chip, 48-mA, single-ended drivers and receivers, the FAS209 can connect directly to the SCSI bus, minimizing board space requirements. The FAS209's highly integrated structure provides users with numerous benefits.

Initiator and target roles are supported; therefore, the FAS209 can be used in both host adapter and peripheral applications. The FAS209 performs such functions as bus arbitration, selection of a target, or reselection of an initiator. It handles message, command, status, and data transfer between the SCSI bus and the chip's 16-byte internal FIFO or a buffer memory. The above functions are internal processes performed by the FAS209 chip without microprocessor intervention.

SCAM Implementation

The FAS209 supports levels 1 and 2 of the SCAM protocol. (Refer to the latest revision of X3T10/855D, Annex B.) The SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

Bus Configuration

The FAS209 split-bus architecture separates the two high-traffic information buses of the system, providing maximum efficiency and throughput. The versatile bus architecture supports various microprocessor and DMA bus configurations, including those listed below:

- Microprocessor interface via the PAD bus or the DB bus
- Concurrent microprocessor and DMA accesses
- PAD bus selectable as a data-only bus

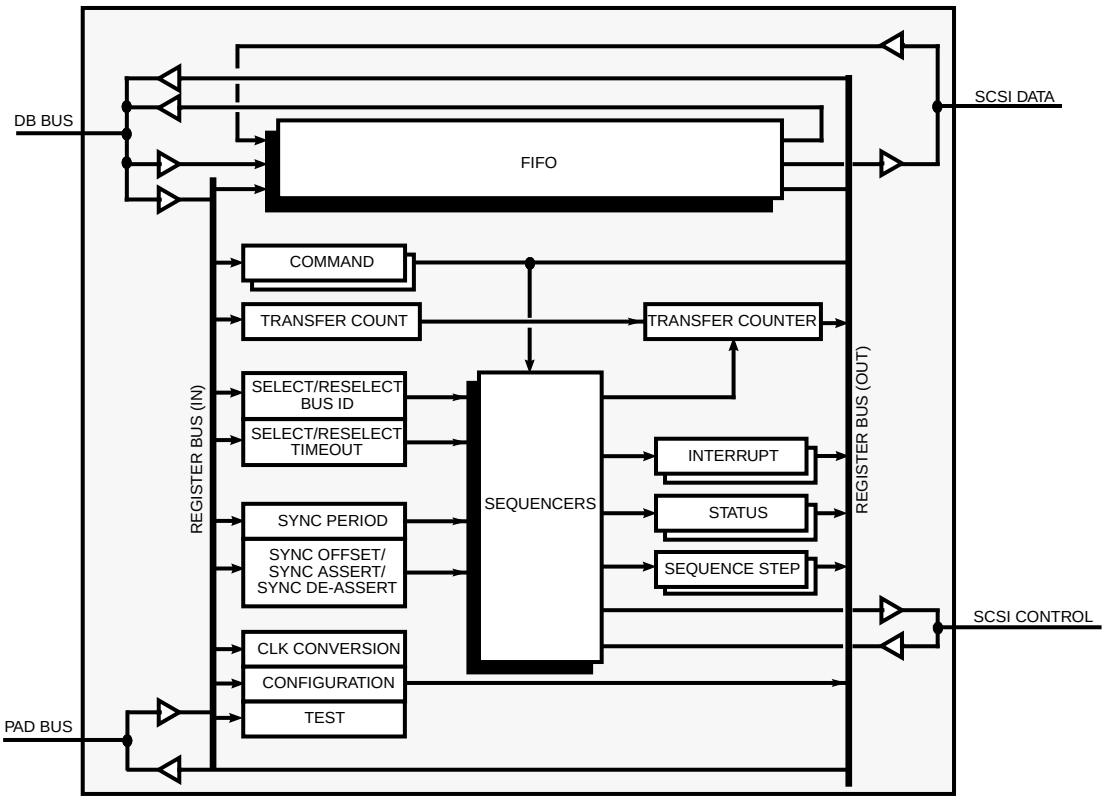


Figure 1. FAS209 Block Diagram

FAS209 bus configuration is selected by pulling the MODE pin up or down, as shown in table 1.

Table 1. Bus Modes

Mode No.	MODE Pin	Register Data	DMA Data	Configuration
0	0	DB bus	DB bus	Single bus, 8-bit DMA
1	1	PAD bus	DB bus	Split bus, 8-bit DMA

Microprocessor Interface

Microprocessor interface to the FAS209 occurs over the PAD bus or the DB bus. Both interfaces allow the microprocessor to read and write to all the internal chip registers, including the FIFO.

In single-bus mode (bus configuration mode 0), the PAD bus is not used and the microprocessor must arbitrate with other controllers for use of the DB bus. In split-bus mode (bus configuration mode 1), the PAD bus is dedicated to the microprocessor interface.

Pins that support the microprocessor and DMA interfaces and other chip operations are shown in figure 2.

DMA Interface

All FAS209 DMA activity occurs over the DB bus. The path is eight bits wide. The DB bus consists of the data parity pin DBP0 and data pins DB7-0. Data is transferred on DB7-0 on writes to and reads from the SCSI bus.

$\overline{\text{DACK}}$ must be active during DMA accesses. The transfer direction is determined by the type of command executed by the chip. $\overline{\text{DBWR}}$ strobes data into the chip. DMA read data is driven by the chip when $\overline{\text{DACK}}$ is true.

Packaging

The FAS209 is available in a 64-pin plastic quad flat pack (PQFP), part number 2405055; and a thin quad flat pack (TQPF), part number 2405095. The pin diagrams are shown in figures 2 and 4. Package dimensions are shown in figures 3 and 5. The FAS209 pins that support microprocessor interfaces and other chip operations are shown in figure 6.

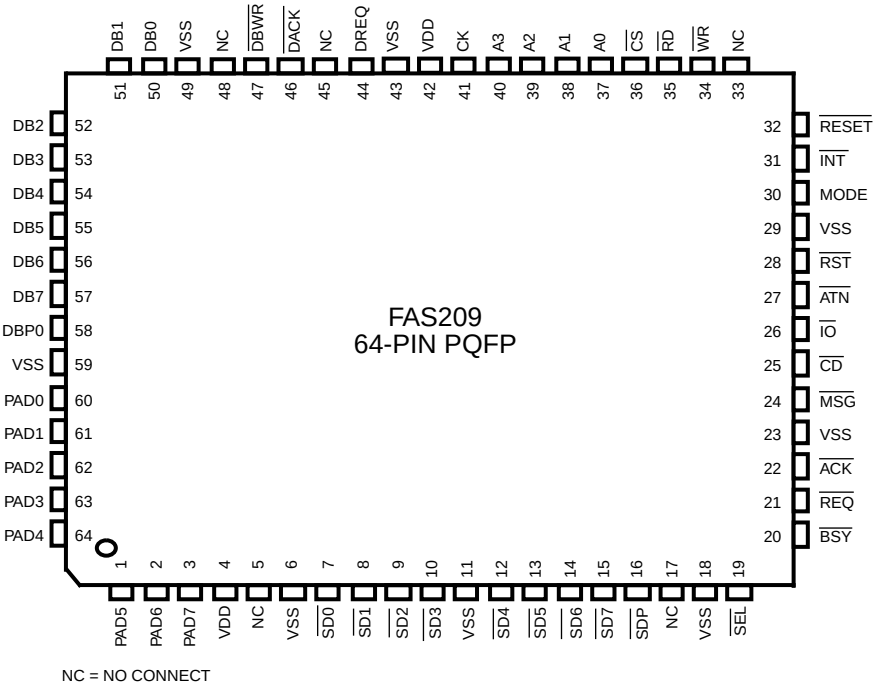
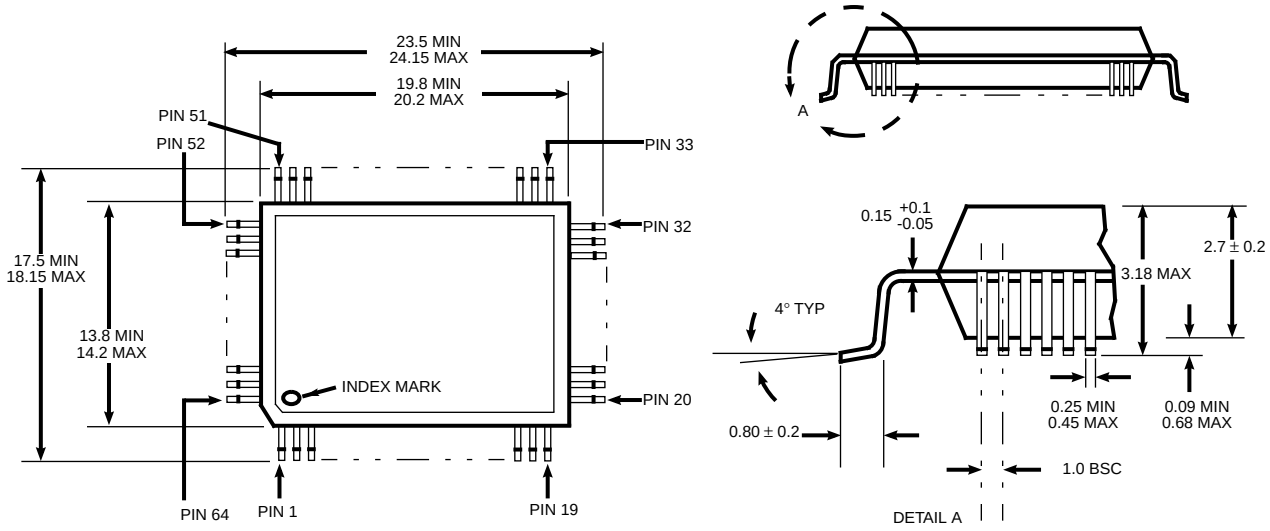
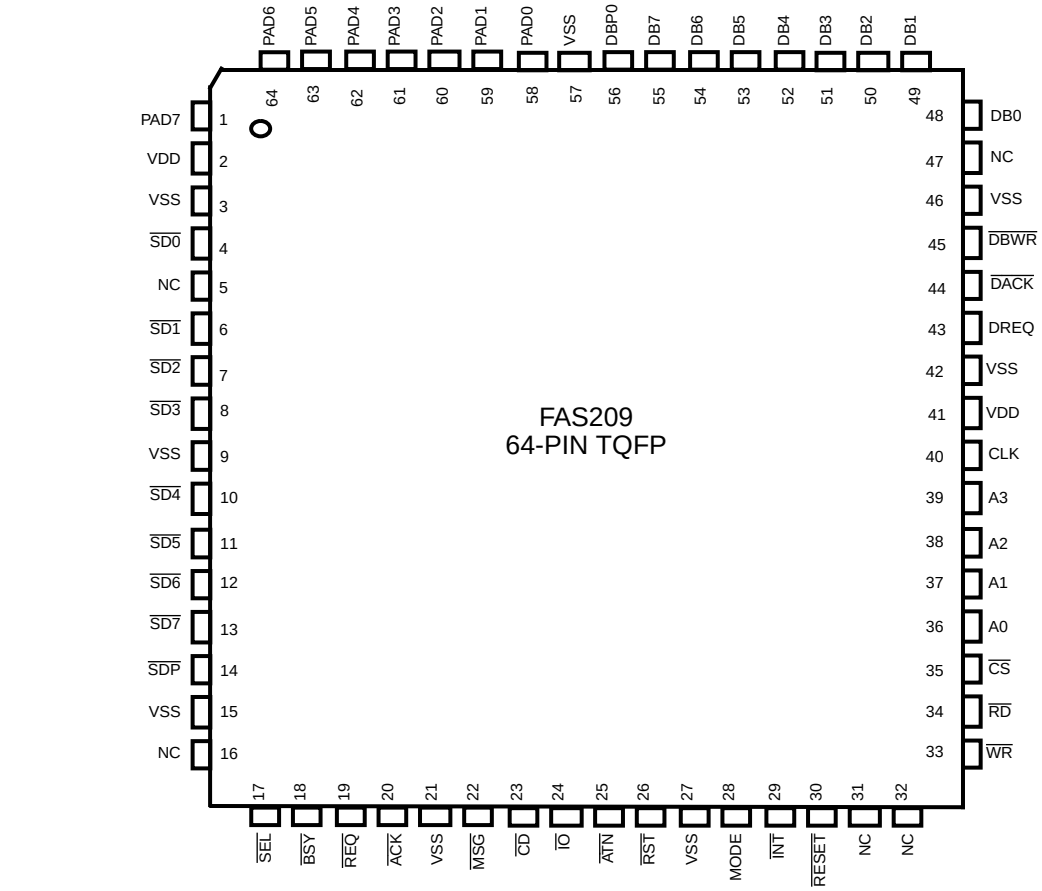


Figure 2. FAS209 PQFP Pin Diagram



NOTE: ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 3. 64-Pin PQFP Mechanical Drawings



NC = NO CONNECT

Figure 4. FAS209 64-Pin TQFP Pin Diagram

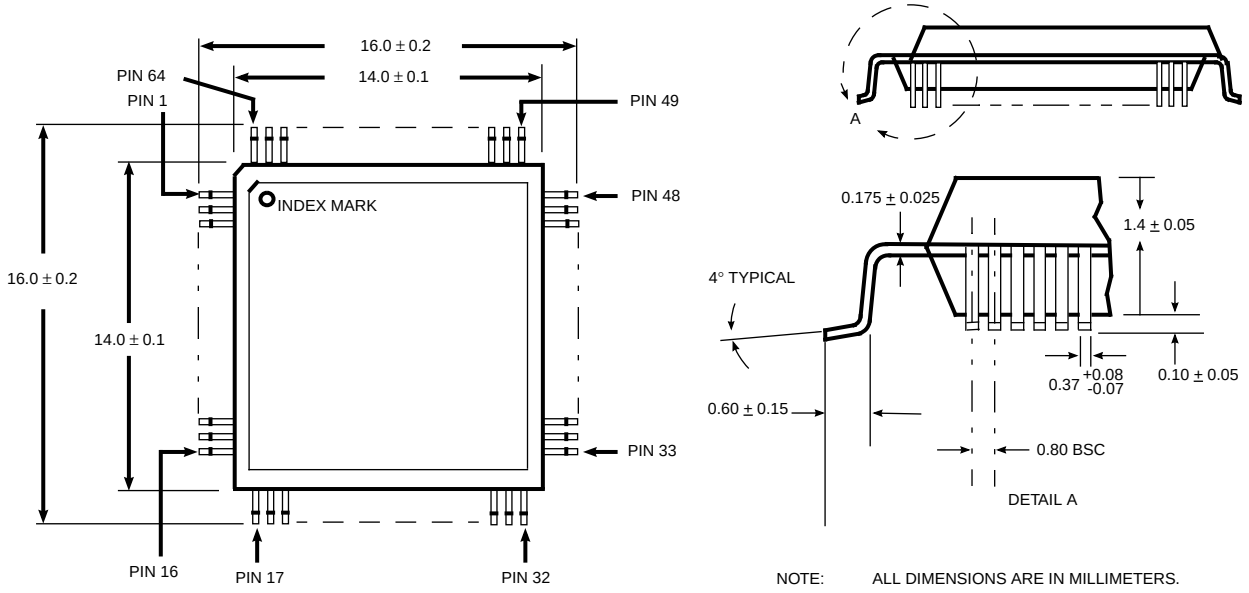


Figure 5. FAS209 TQFP Mechanical Drawings

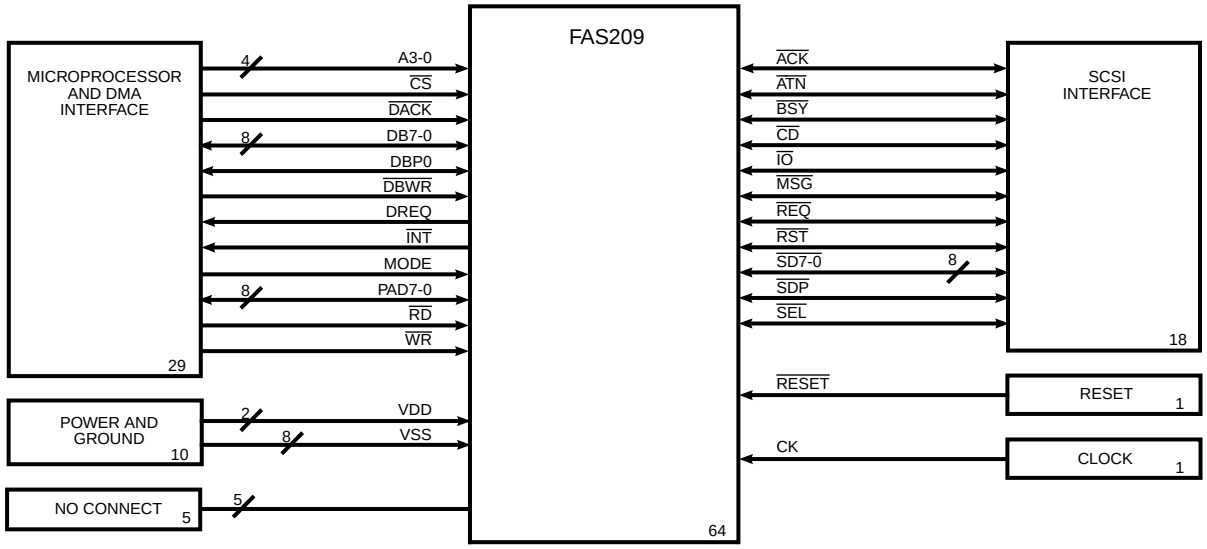


Figure 6. FAS209 Functional Signal Grouping

Electrical Characteristics

Table 2. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
VDD	Supply voltage	4.75	5.25	V
IDD[a]	Supply current (static IDD)		TBD	mA
IDD	Supply current (dynamic IDD)		TBD	mA
TA	Ambient temperature	0	70	°C

Table Notes

Conditions that exceed the operating conditions but are within the absolute maximum stress ratings may cause the chip to malfunction.

Capacitance in and out (CIN, COUT) is 10 pF maximum for all pins, except SCSI pins.

[a]Static IDD refers to all inputs at VDD, all outputs open circuit, and all bidirectional pins configured as inputs.

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