



December 2006

# FDD8750

## N-Channel PowerTrench<sup>®</sup> MOSFET

25V, 2.7A, 40mΩ

### Features

- Max  $r_{DS(on)}$  = 40mΩ at  $V_{GS} = 10V, I_D = 2.7A$
- Max  $r_{DS(on)}$  = 60mΩ at  $V_{GS} = 4.5V, I_D = 2.7A$
- Low gate charge:  $Q_{g(10)} = 6nC(Typ)$
- Low gate resistance
- Avalanche rated and 100% tested
- RoHS Compliant

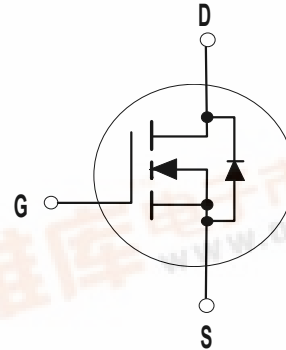
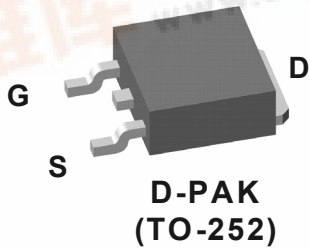


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$  and fast switching speed.

### Application

- Low current DC-DC switching
- Linear regulation



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous(Package Limited)	$T_C = 25^\circ C$	2.7
	-Continuous(Silicon Limited)	$T_C = 25^\circ C$ (Note 1)	16
	-Continuous	$T_A = 25^\circ C$ (Note 1a)	6.5
	-Pulsed		14
$E_{AS}$	Drain-Source Avalanche Energy (Note 3)	19	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ C$	18
	Power Dissipation (Note 1a)		3.7
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	8	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8750	FDD8750	D-PAK(TO-252)	13"	12mm	2500 units

FDD8750 N-Channel PowerTrench<sup>®</sup> MOSFET

### Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		18		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$ $T_J = 150^\circ\text{C}$			1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

#### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	2.0	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.7\text{A}$		28	40	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 2.7\text{A}$		39	60	
		$V_{GS} = 10\text{V}, I_D = 2.7\text{A}, T_J = 150^\circ\text{C}$		44	63	

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 13\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		320	425	pF
$C_{oss}$	Output Capacitance			80	110	pF
$C_{rss}$	Reverse Transfer Capacitance			50	75	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		1.8	

#### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{V}, I_D = 2.7\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		3	10	ns
$t_r$	Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			8	16	ns
$t_f$	Fall Time			5	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V to } 10\text{V}$	$V_{DD} = 13\text{V}$ $I_D = 2.7\text{A}$	6	9	nC
$Q_{g(5)}$	Total Gate Charge	$V_{GS} = 0\text{V to } 5\text{V}$		3.4	5	nC
$Q_{gs}$	Gate to Source Gate Charge			1.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.2		nC

#### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.7\text{A}$ (Note 2)		0.8	1.6	V
$t_{rr}$	Reverse Recovery Time	$I_F = 2.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$		16	24	ns
$Q_{rr}$	Reverse Recovery Charge			7	11	nC

#### Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
  - 40°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper;
  - 96°C/W when mounted on a minimum pad.
- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25^\circ\text{C}$ , L = 3mH,  $I_{AS} = 3.6\text{A}$ ,  $V_{DD} = 25\text{V}$ ,  $V_{GS} = 10\text{V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

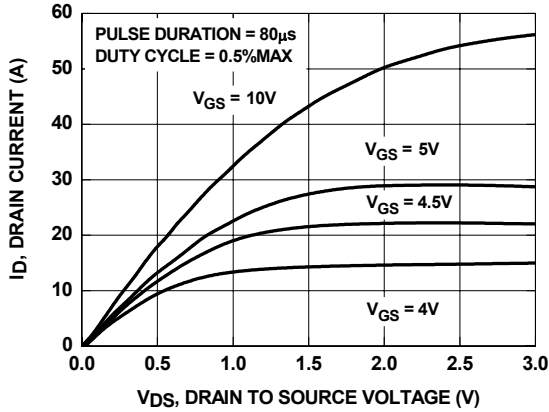


Figure 1. On Region Characteristics

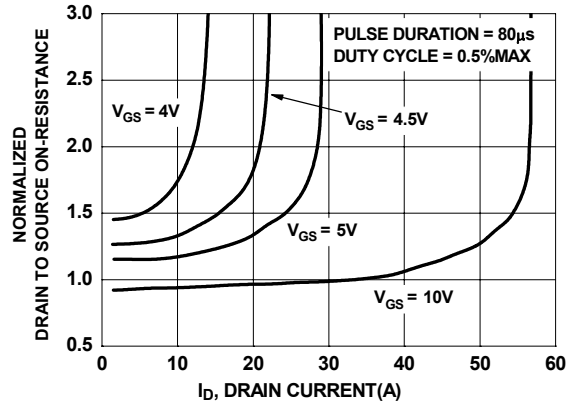


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

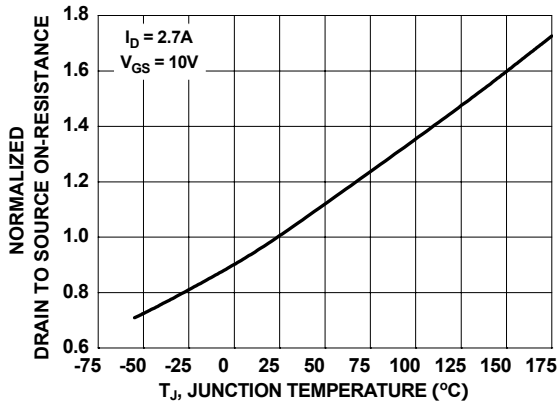


Figure 3. Normalized On Resistance vs Junction Temperature

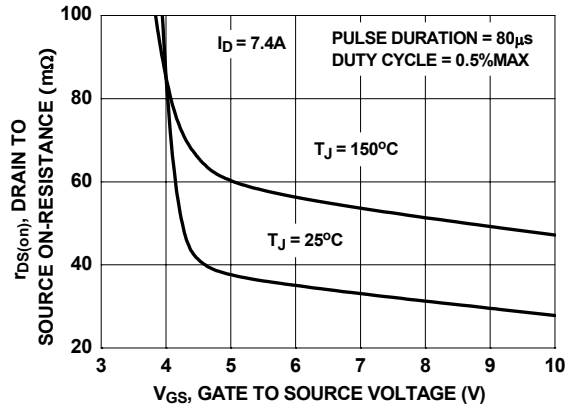


Figure 4. On-Resistance vs Gate to Source Voltage

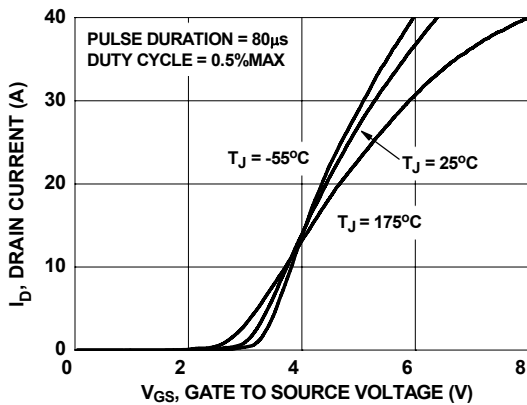


Figure 5. Transfer Characteristics

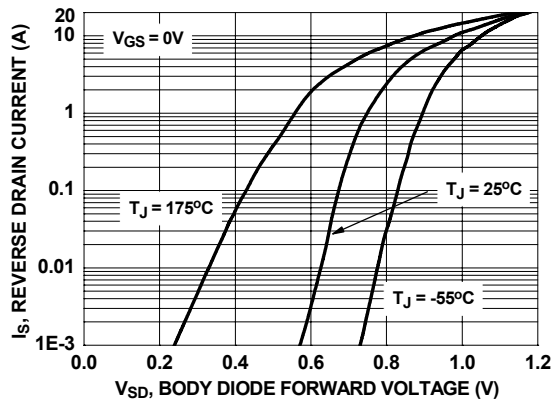
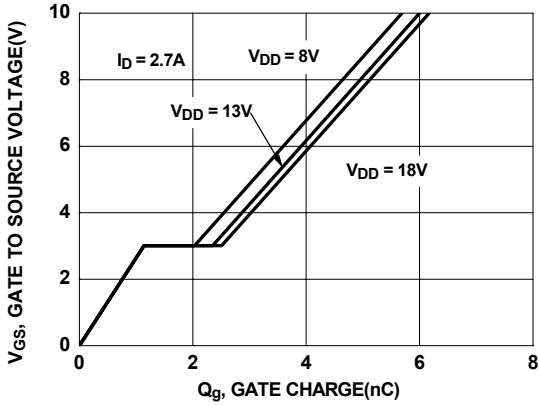
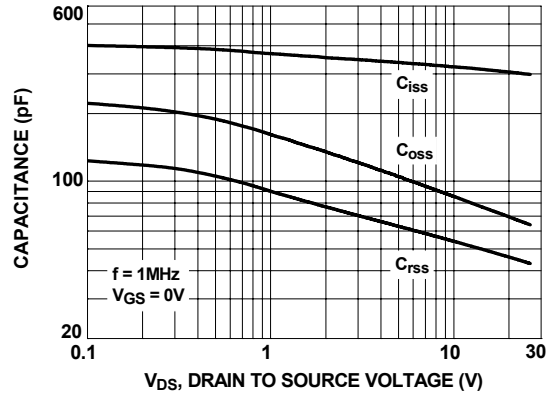


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

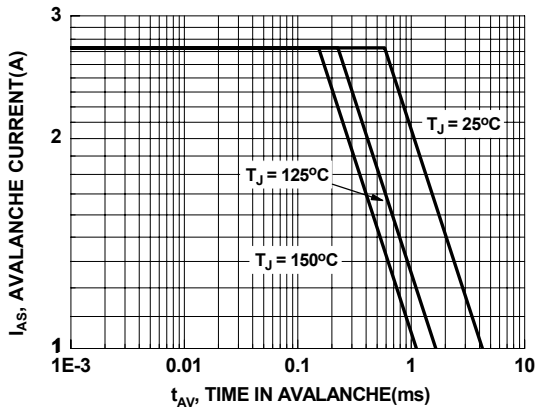
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



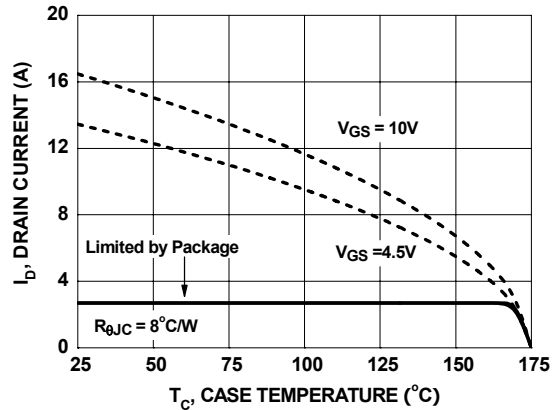
**Figure 7. Gate Charge Characteristics**



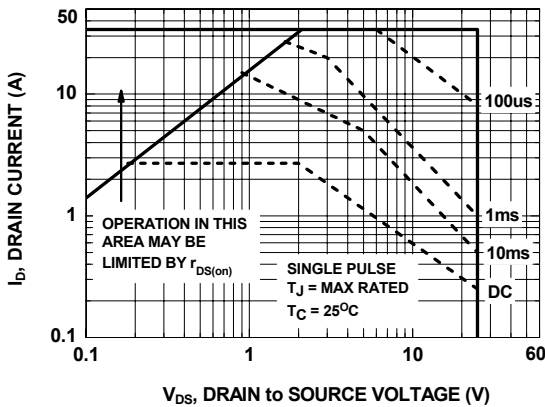
**Figure 8. Capacitance vs Drain to Source Voltage**



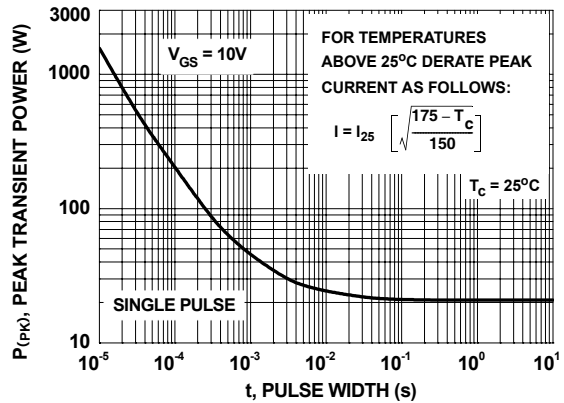
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

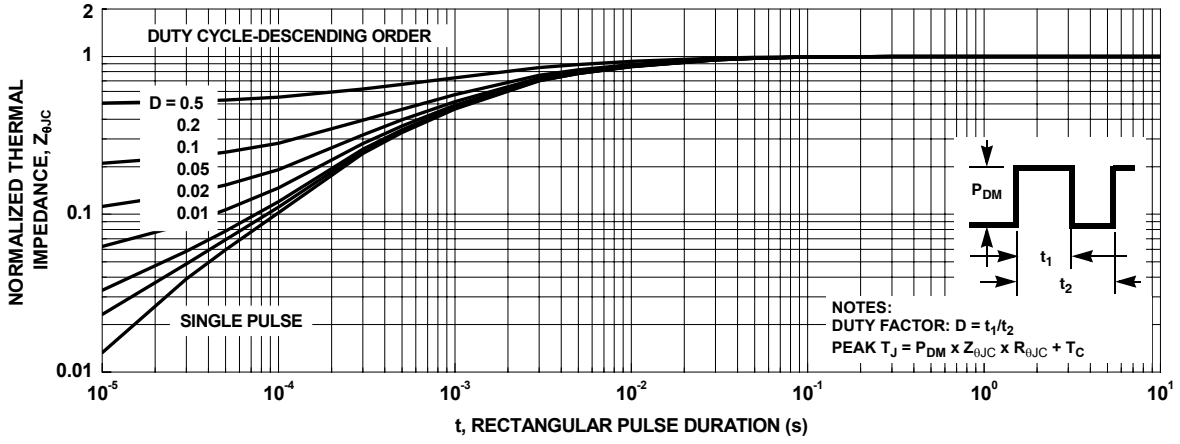


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

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