



January 2007

# FDMC5614P

## P-Channel PowerTrench<sup>®</sup> MOSFET

-60V, -13.5A, 100mΩ

### Features

- Max  $r_{DS(on)}$  = 100mΩ at  $V_{GS} = -10V$ ,  $I_D = -5.7A$
- Max  $r_{DS(on)}$  = 135mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -4.4A$
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability
- RoHS Compliant

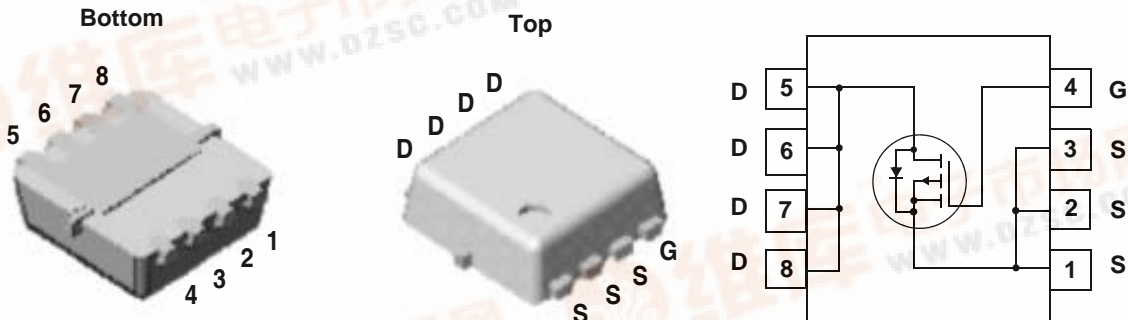


### General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V-20V).

### Application

- Power management
- Load switch
- Battery protection



Power 33

### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-60	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ C$	-13.5	A
	-Continuous (Silicon limited) $T_C = 25^\circ C$	-14	
	-Continuous $T_A = 25^\circ C$ (Note 1a)	-5.7	
	-Pulsed	-23	
$P_D$	Power Dissipation $T_C = 25^\circ C$	42	W
	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	2.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
5614P	FDMC5614P	Power 33	7"	8mm	3000 units

FDMC5614P P-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-54		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -48\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-1.95	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		4.7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -5.7\text{A}$		84	100	m $\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -4.4\text{A}$		108	135	
		$V_{GS} = -10\text{V}, I_D = -5.7\text{A}, T_J = 125^\circ\text{C}$		140	168	
$g_{FS}$	Forward Transconductance	$V_{DS} = -15\text{V}, I_D = -5.7\text{A}$		11		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		795	1055	pF
$C_{oss}$	Output Capacitance			140	185	pF
$C_{rss}$	Reverse Transfer Capacitance			60	90	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{V}, I_D = -1\text{A}$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		10	21	ns	
$t_r$	Rise Time			11	23	ns	
$t_{d(off)}$	Turn-Off Delay Time			32	65	ns	
$t_f$	Fall Time			11	22	ns	
$Q_{g(TOT)}$	Total Gate Charge at 10V		$V_{GS} = -10\text{V}$		15	20	nC
$Q_{gs}$	Gate to Source Gate Charge		$V_{DD} = -30\text{V}$ $I_D = -5.7\text{A}$		1.6	2.1	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.7	3.5	nC	

### Drain-Source Diode Characteristics

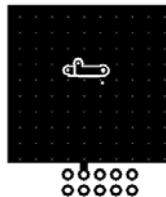
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -3.2\text{A}$		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -3.2\text{A}, di/dt = 100\text{A}/\mu\text{s}$			36	ns
$Q_{rr}$	Reverse Recovery Charge				29	nC

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

(a)  $R_{\theta JA} = 60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5'x1.5'x0.062' thick PCB.

(b)  $R_{\theta JA} = 135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.



a.  $60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty cycle < 2.0%.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

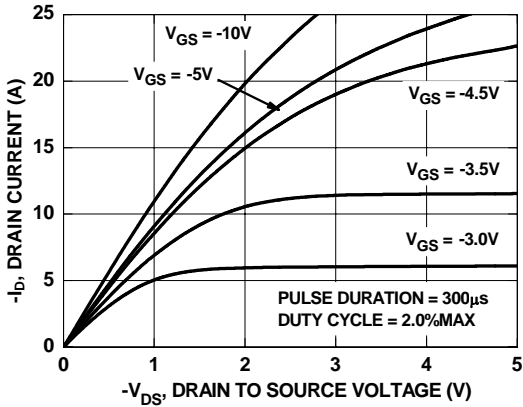


Figure 1. On-Region Characteristics

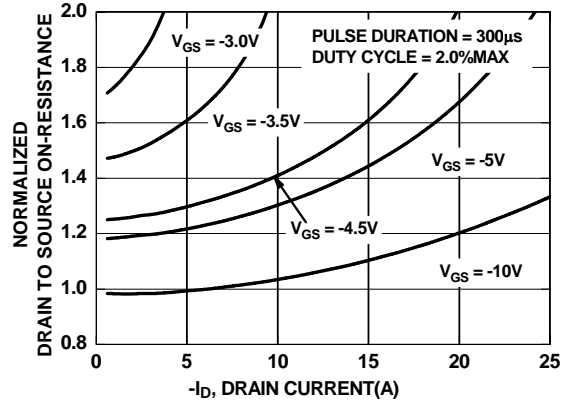


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

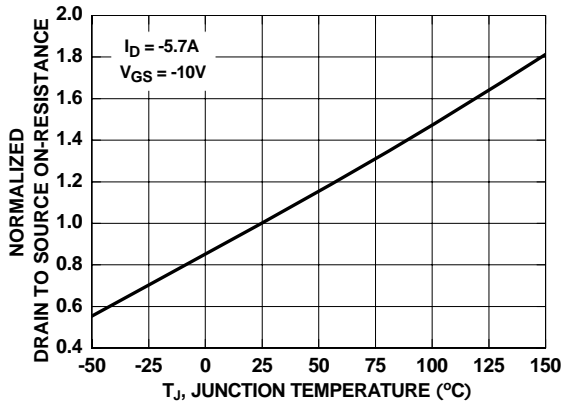


Figure 3. Normalized On-Resistance vs Junction Temperature

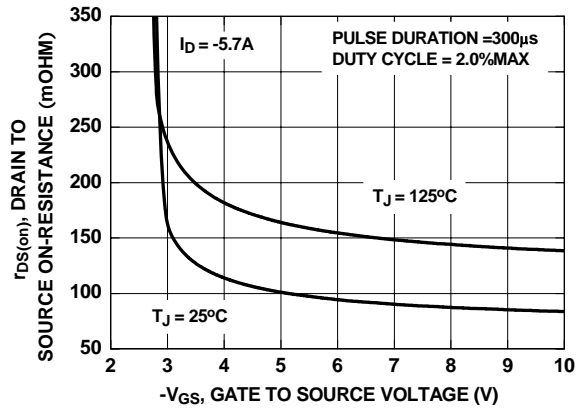


Figure 4. On-Resistance vs Gate to Source Voltage

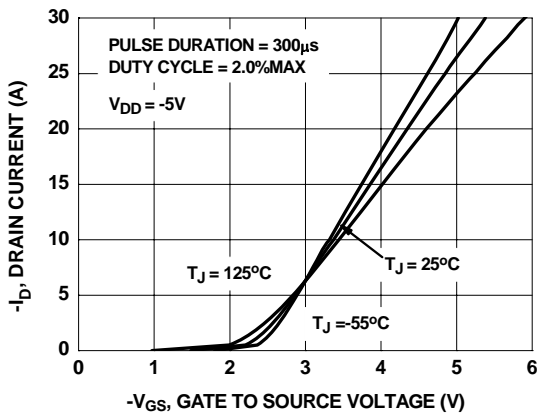


Figure 5. Transfer Characteristics

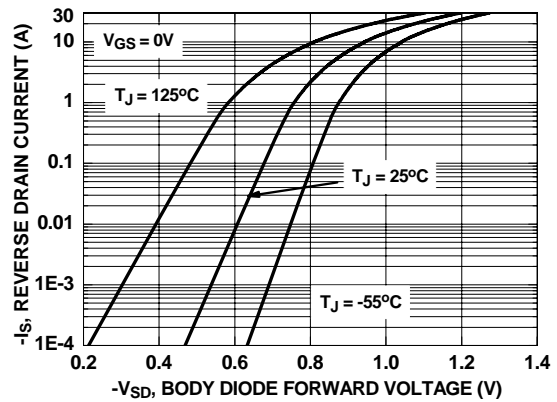


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

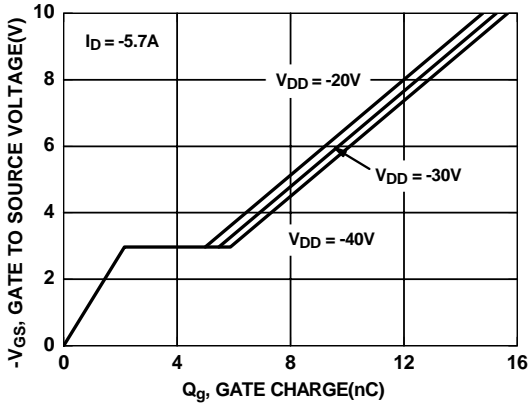


Figure 7. Gate Charge Characteristics

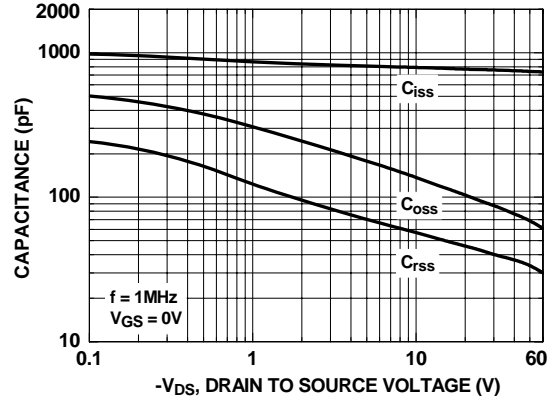


Figure 8. Capacitance vs Drain to Source Voltage

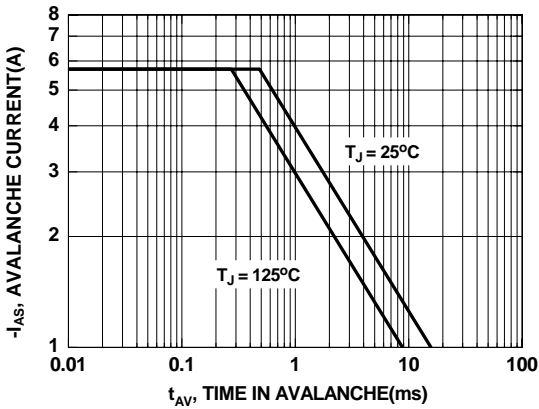


Figure 9. Unclamped Inductive Switching Capability

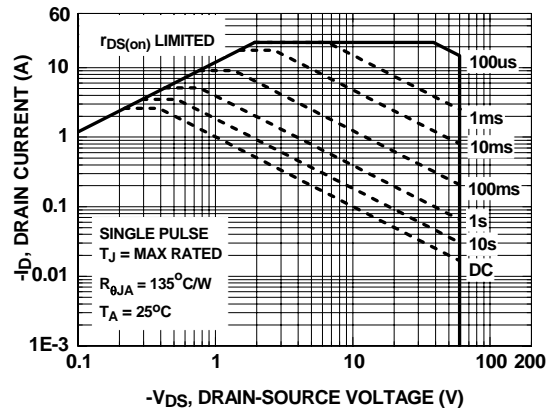


Figure 10. Forward Bias Safe Operating Area

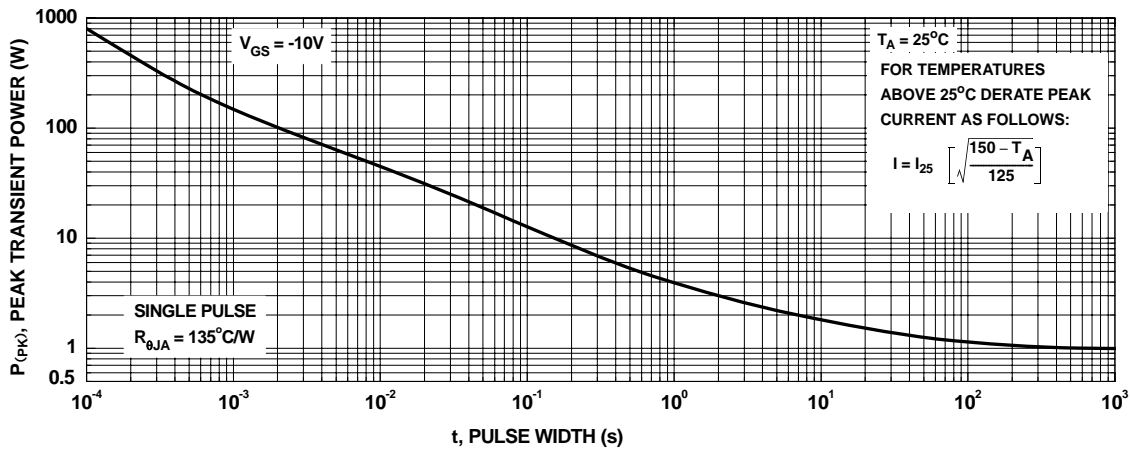
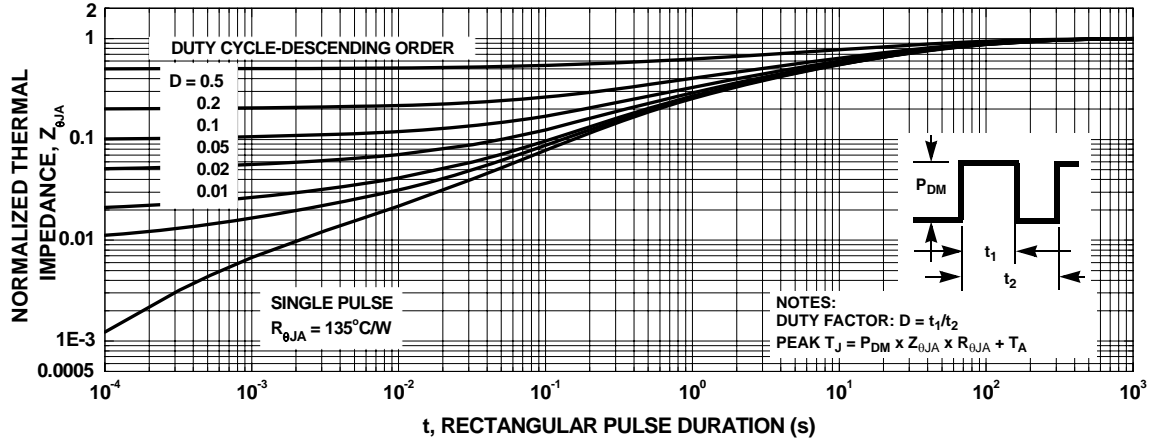
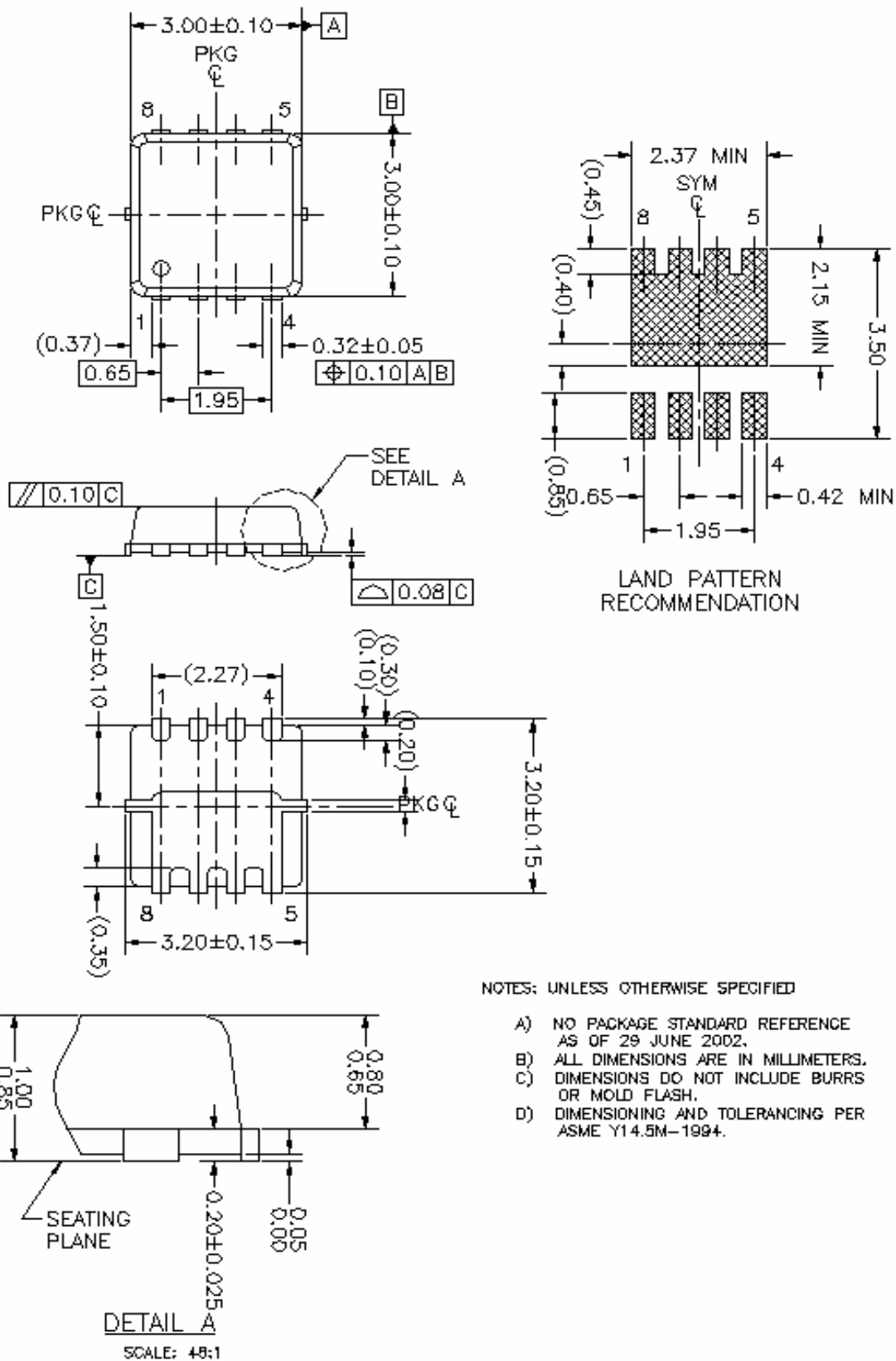


Figure 11. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 12. Transient Thermal Response Curve**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO PACKAGE STANDARD REFERENCE AS OF 29 JUNE 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

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