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FAIRCHILD SEMICONDUCTOR®

December 2007

FDMC8678S

N-Channel Power Trench® SyncFET™

30V, 18A, 5.2mΩ

Features

- Max $r_{DS(on)}$ = 5.2mΩ at V_{GS} = 10V, I_D = 15A
- Max $r_{DS(on)}$ = 8.7mΩ at V_{GS} = 4.5V, I_D = 12A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- SyncFET Schottky Body Diode
- MSL1 robust package design
- RoHS Compliant

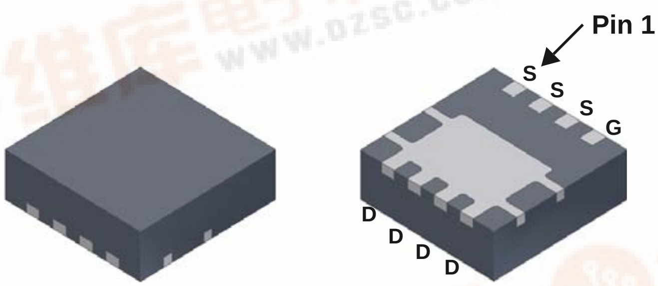
General Description

The FDMC8678S has been designed to minimize losses in power conversion applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

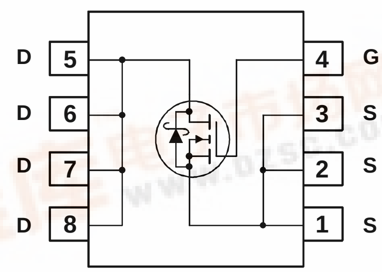
Synchronous Rectifier for DC/DC Converters

- Notebook Vcore/ GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification



Bottom   TOP

Power 33



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C	18	A
	-Continuous (Silicon limited) T_C = 25°C	66	
	-Continuous T_A = 25°C (Note 1a)	15	
	-Pulsed	60	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	181	mJ
P_D	Power Dissipation T_C = 25°C	41	W
	Power Dissipation T_A = 25°C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8678S	FDMC8678S	Power 33	13''	12 mm	3000 units

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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1mA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1mA, referenced to 25°C		38		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0V, V_{DS} = 24V,			500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1mA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 1mA, referenced to 25°C		-3.7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 15A		4.3	5.2	mΩ
		V_{GS} = 4.5V, I_D = 12A		6.3	8.7	
		V_{GS} = 10V, I_D = 15A, T_J = 125°C		6	10	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 15A		55		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		1560	2075	pF
C_{oss}	Output Capacitance			810	1080	pF
C_{rss}	Reverse Transfer Capacitance			90	135	pF
R_g	Gate Resistance	f = 1MHz		0.8		Ω

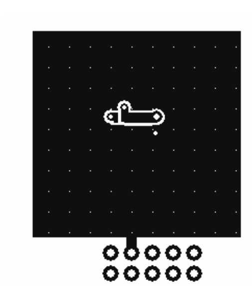
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 15A, V_{GS} = 10V, R_{GEN} = 6Ω		11	20	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			24	39	ns
t_f	Fall Time			2	10	ns
Q_g	Total Gate Charge	V_{GS}=0V to 10V; V_{DD} = 15V, I_D = 15A		24	34	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 4.5V; V_{DD} = 15V, I_D = 15A		11	16	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15V, I_D = 15A		4.7		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.8		nC

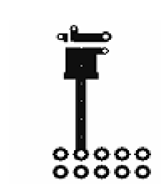
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 3A (Note 2)		0.5	0.7	V
t_{rr}	Reverse Recovery Time	I_F = 15A, di/dt = 300A/μs		31	51	ns
Q_{rr}	Reverse Recovery Charge			33	51	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting T_J = 25^{o}C; N-ch: L = 3mH, I_{AS} = 11A, V_{DD} = 30V, V_{GS} = 10V

Typical Characteristics T_J = 25°C unless otherwise noted

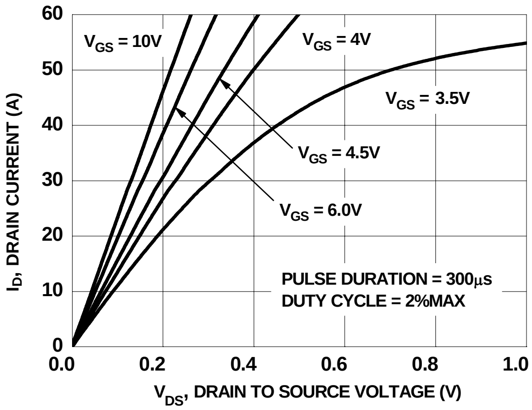


Figure 1. On-Region Characteristics

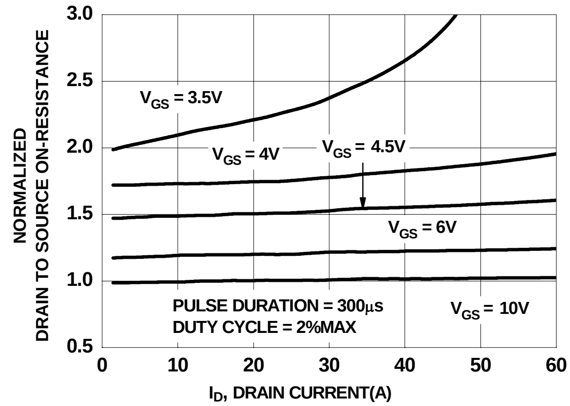


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

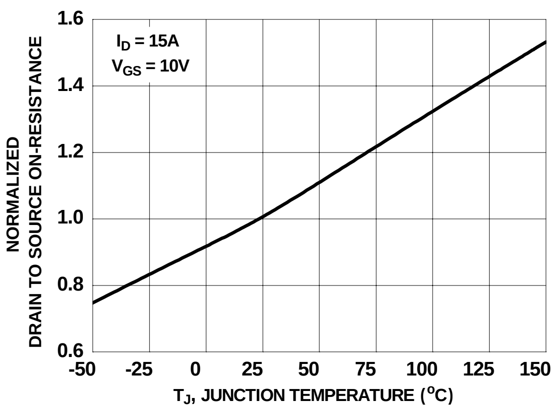


Figure 3. Normalized On-Resistance vs Junction Temperature

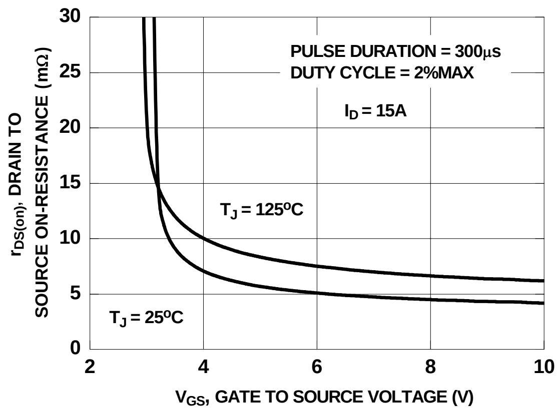


Figure 4. On-Resistance vs Gate to Source Voltage

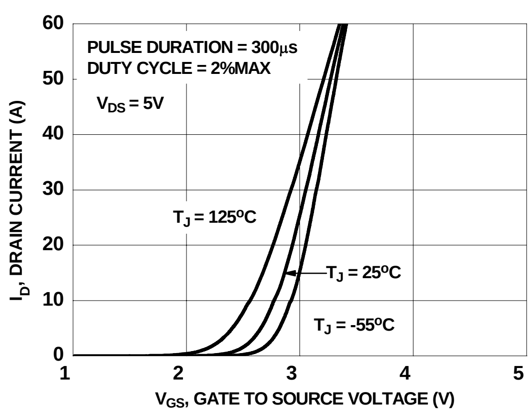


Figure 5. Transfer Characteristics

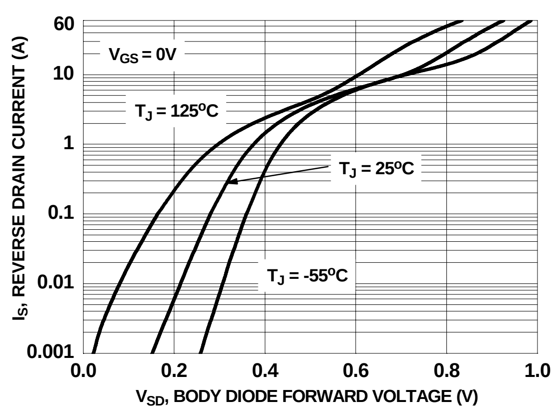


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

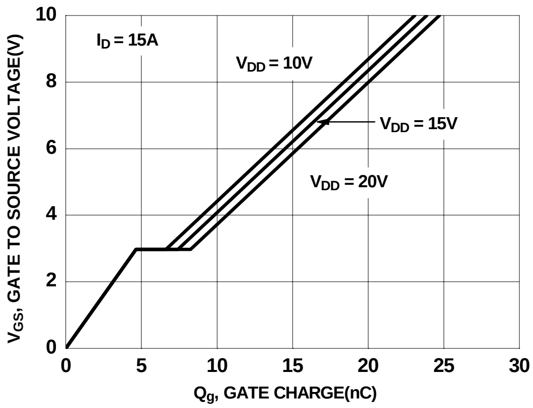


Figure 7. Gate Charge Characteristics

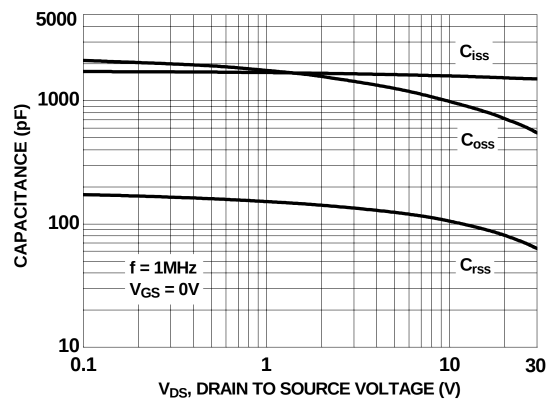


Figure 8. Capacitance vs Drain to Source Voltage

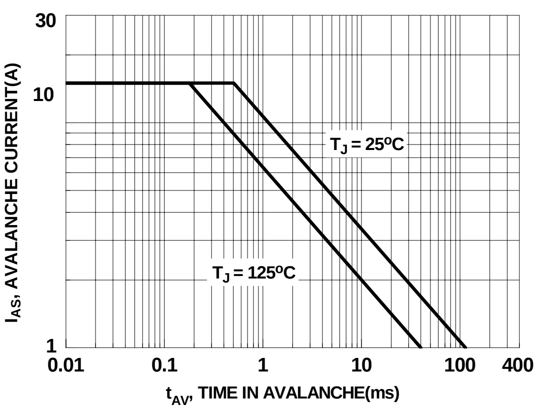


Figure 9. Unclamped Inductive Switching Capability

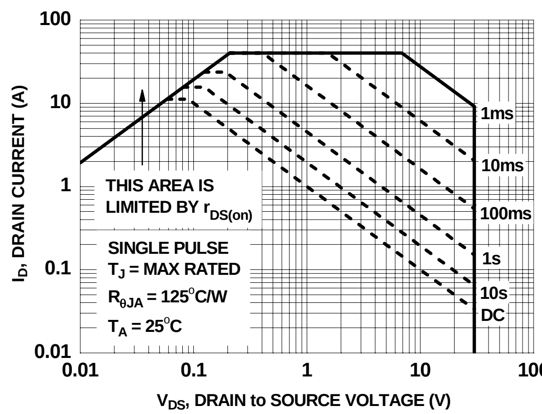


Figure 10. Forward Bias Safe Operating Area

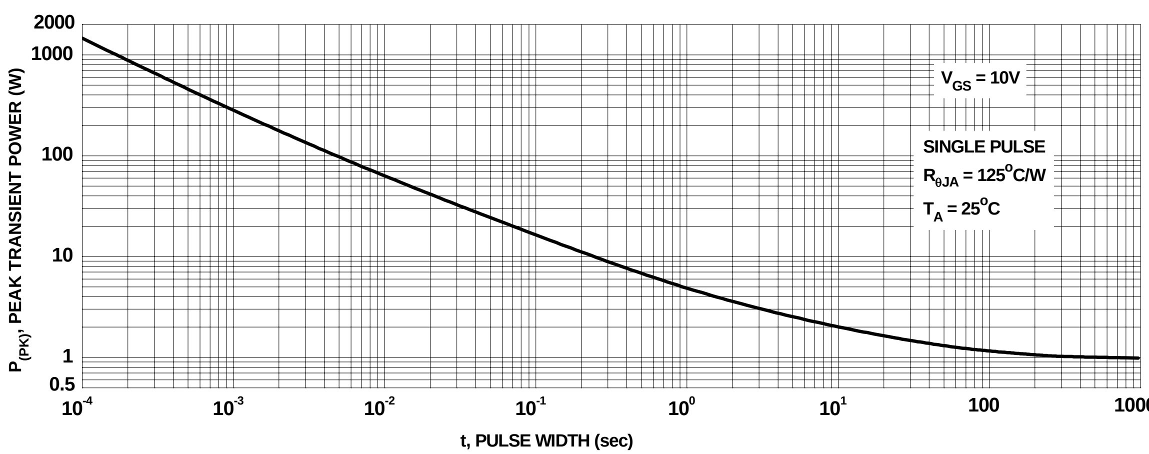


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

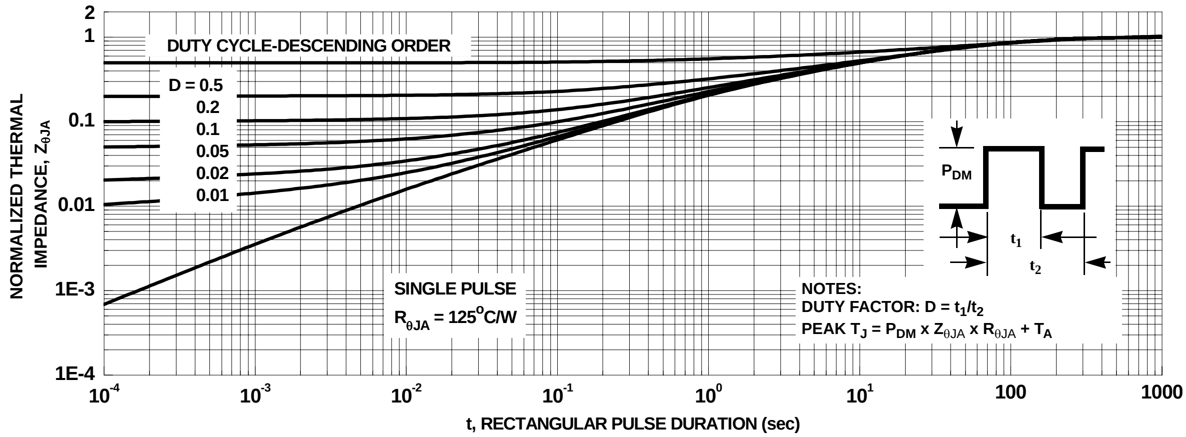


Figure 12. Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MoSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverses recovery characteristic of the FDMC8678S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

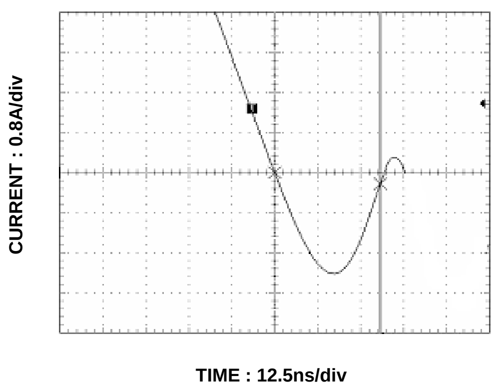


Figure 13. SyncFET body diode reverse recovery characteristic

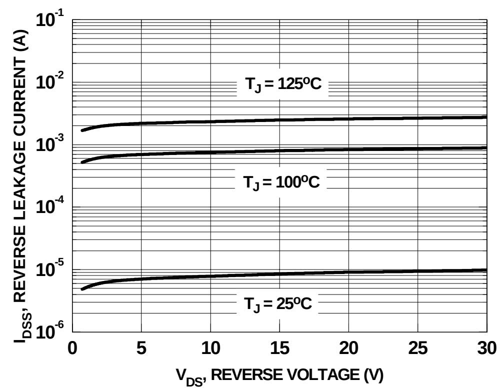
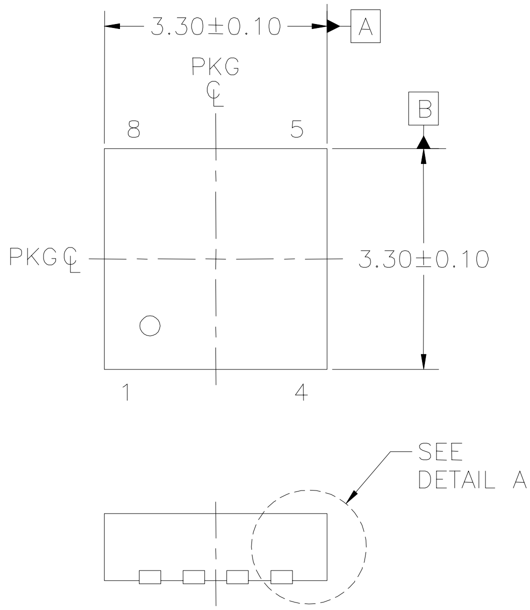
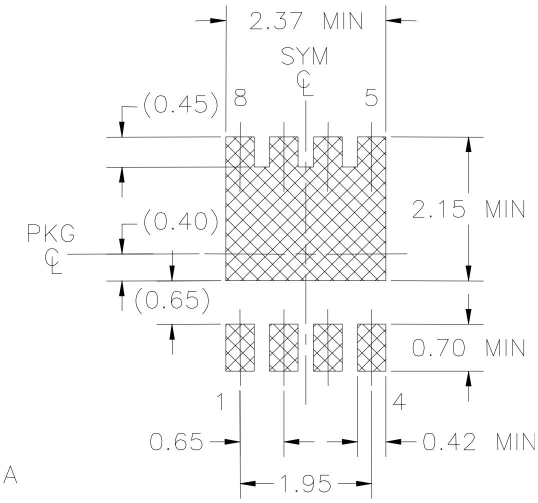


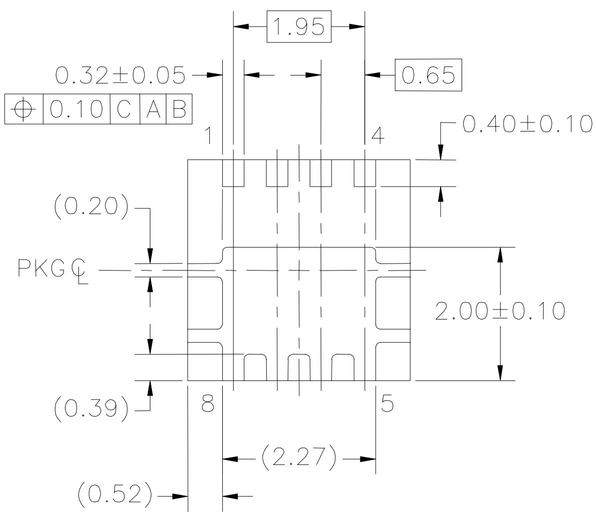
Figure 14. SyncFET body diode reverses leakage versus drain-source voltage

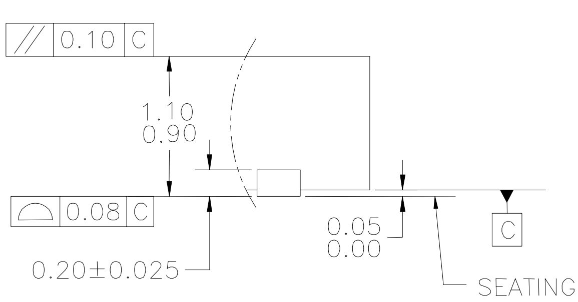
Dimensional Outline and Pad Layout





LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE:
JEDEC MO-240, ISSUE A, VAR. BA,
DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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