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FAIRCHILD
SEMICONDUCTOR®

June 2003

FDS6612A

Single N-Channel, Logic-Level, PowerTrench® MOSFET

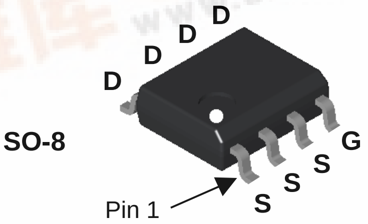
General Description

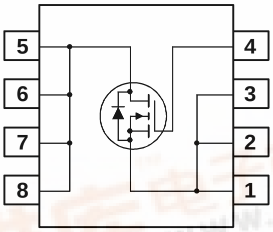
This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 8.4 A, 30 V. $R_{DS(ON)}$ = 22 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 30 mΩ @ V_{GS} = 4.5 V
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	8.4	A
	– Pulsed		40	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6612A	FDS6612A	13''	12mm	2500 units

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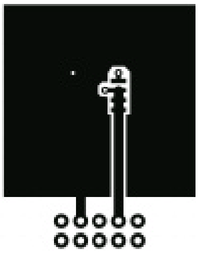
Electrical Characteristics

T_A = 25°C unless otherwise noted

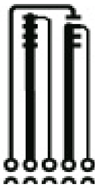
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		26		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J=55°C			10	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–4.4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 8.4 A V_{GS} = 4.5 V, I_D = 7.2 A V_{GS}= 10 V, I_D = 8.4 A, T_J=125°C		19 24 25	22 30 37	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 8.4 A		30		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		560		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			55		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		2.5		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		7	14	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			22	35	ns
t_f	Turn–Off Fall Time			3	6	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 8.4 A, V_{GS} = 5 V		5.4	7.6	nC
Q_{gs}	Gate–Source Charge			1.7		nC
Q_{gd}	Gate–Drain Charge			1.9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.77	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 8.4 A, d_{iF}/d_t = 100 A/µs		19		nS
Q_{rr}	Diode Reverse Recovery Charge			9		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2 Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

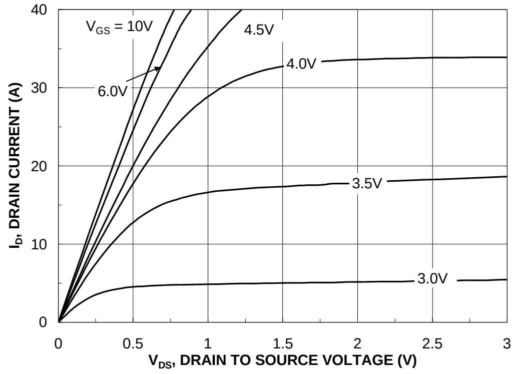


Figure 1. On-Region Characteristics.

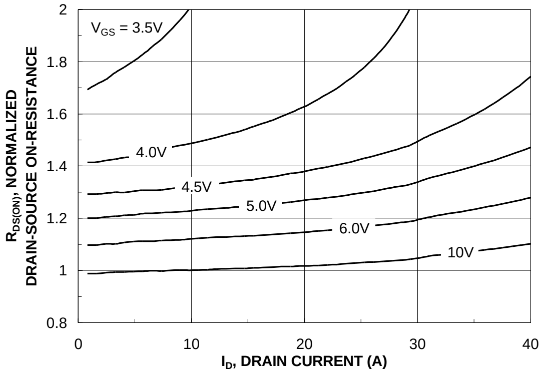


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

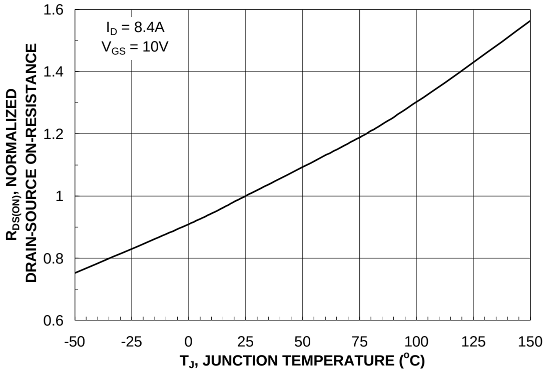


Figure 3. On-Resistance Variation with Temperature.

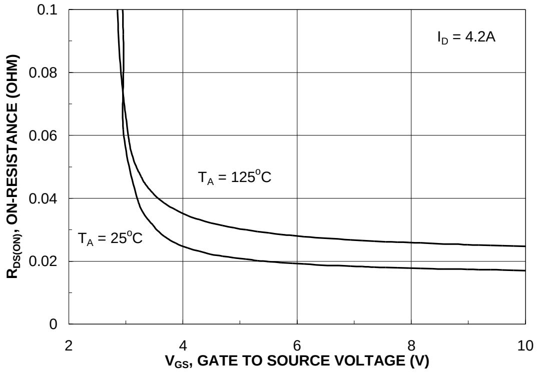


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

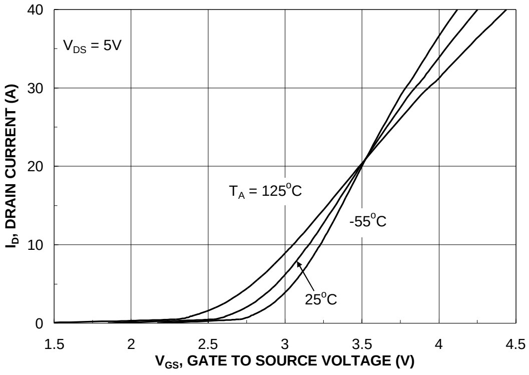


Figure 5. Transfer Characteristics.

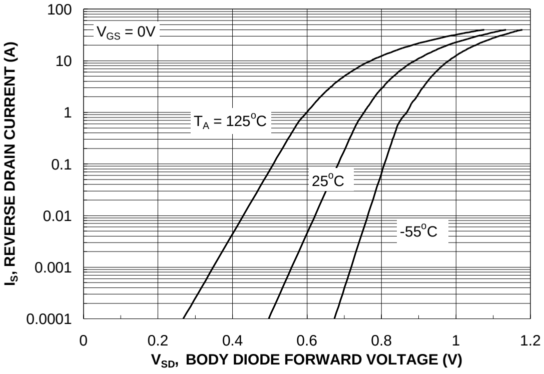


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

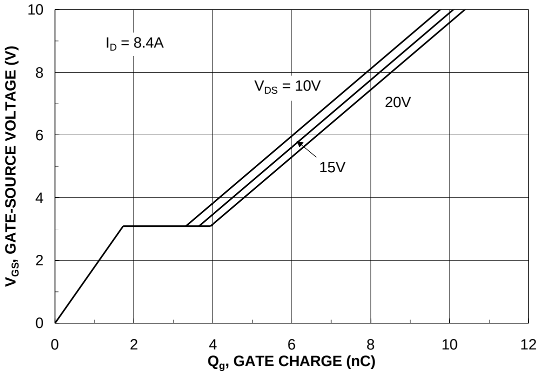


Figure 7. Gate Charge Characteristics.

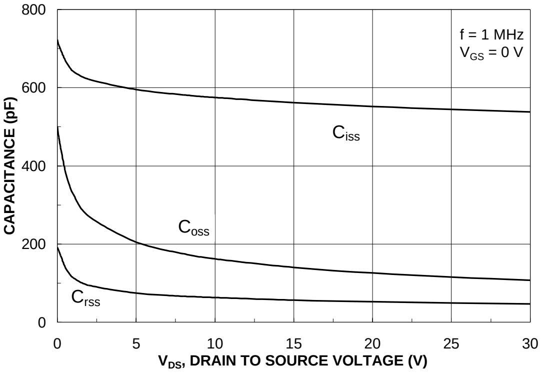


Figure 8. Capacitance Characteristics.

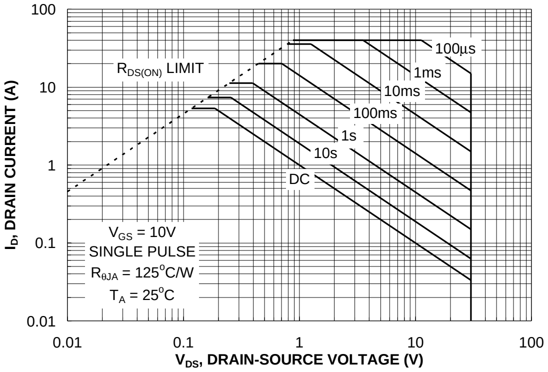


Figure 9. Maximum Safe Operating Area.

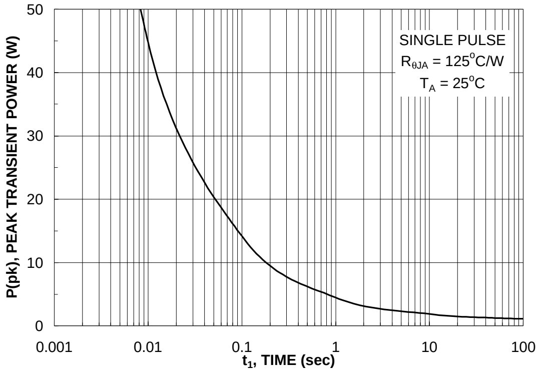


Figure 10. Single Pulse Maximum Power Dissipation.

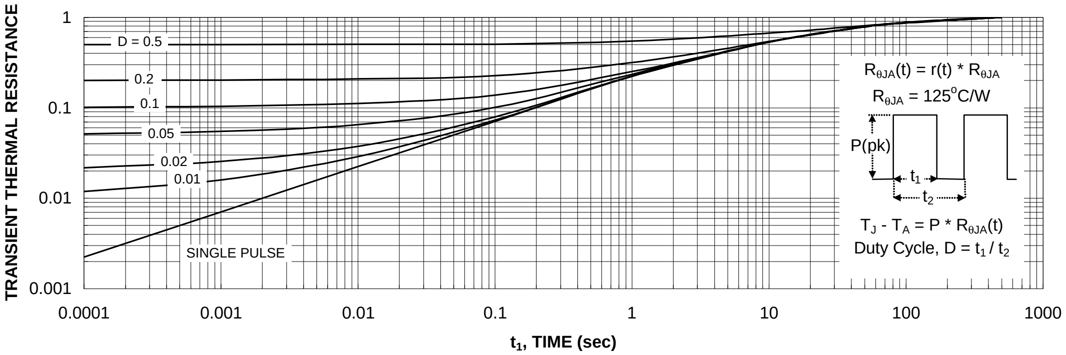
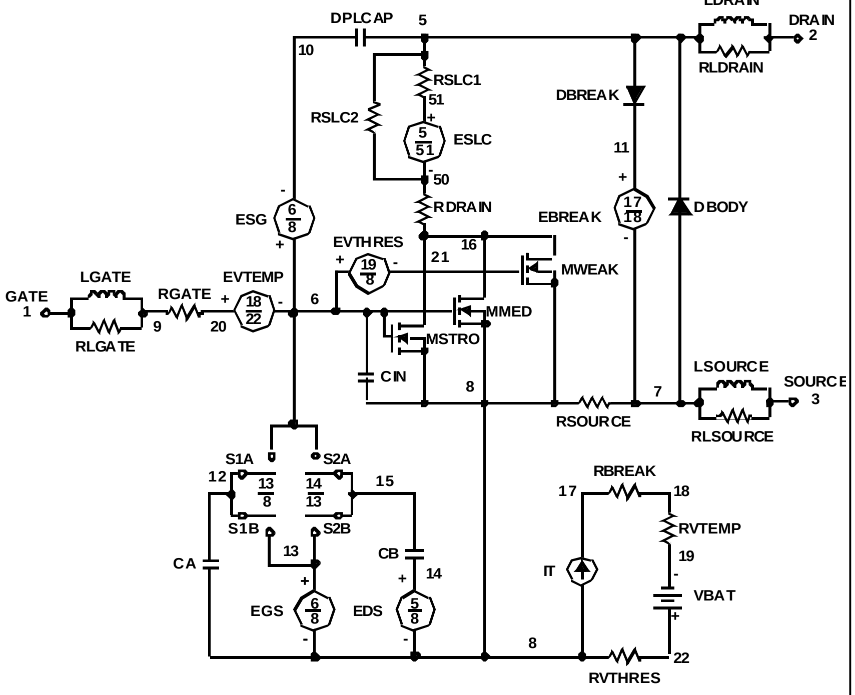


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

PSPICE Electrical Model N-Channel


DPLCAP
5
10
LDRAIN
DRAIN
2
RLDRAIN
RSLC1
51
RSLC2
5/51
ESLC
50
DBREAK
11
17/18
EBREAK
DBODY
RDRAIN
ESG
6/8
EVTHRES
19/8
16
21
MWEAK
GATE
1
LGATE
RLGATE
RGATE
9
20
EVTEMP
18/22
6
MMED
MSTRO
CIN
8
7
RSOURCE
LSOURCE
RLSOURCE
SOURCE
3
S1A
S2A
12
13/8
14/13
15
S1B
S2B
13
CA
CB
14
EGS
6/8
EDS
5/8
RBREAK
17
18
RVTEMP
19
IT
VBAT
22
RVTHRES

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.SUBCKT FDS6612A  2 1 3
*NOM TEMP=25 DEG C
*REV A - JULY 2003

CA 12 8 1E-9
CB 15 14 4.0E-10
CIN 6 8 5.1E-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 34.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LGATE 1 9 3.84E-9
LDRAIN 2 5 1.00E-9
LSOURCE 3 7 4E-9

RLGATE 1 9 38.4
RLDRAIN 2 5 10
RLSOURCE 3 7 40

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 8E-3
RGATE 9 20 4.2

RSLC1 5 51 RSLCMOD 1E-6
RSLC2 5 50 1E3
RSOURCE 8 7 RSOURCEMOD 7.5E-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1E-6*105),3))}

.MODEL DBODYMOD D (IS=7E-15 RS=6.1E-3 N=0.84 TRS1=1.7E-3 TRS2=1.0E-6
+ CJO=3.2E-10 TT=10E-9 M=0.5 IKF=0.3 XTI=3.0)
.MODEL DBREAKMOD D (RS=1E-1 TRS1=1.12E-3 TRS2=1.25E-6)
.MODEL DPLCAPMOD D (CJO=14E-11 IS=1E-30 N=10 M=0.34)
.MODEL MWEAKMOD NMOS (VTO=1.82 KP=0.05 IS=1E-30 N=10 TOX=1 L=1U W=1U RG=42 RS=.1)
.MODEL MMEDMOD NMOS (VTO=2.1 KP=6 IS=1E-30 N=10 TOX=1 L=1U W=1U RG=4.2)
.MODEL MSTROMOD NMOS (VTO=2.55 KP=50 IS=1E-30 N=10 TOX=1 L=1U W=1U)
.MODEL RBREAKMOD RES (TC1=0.83E-3 TC2=1E-7)
.MODEL RDRAINMOD RES (TC1=6E-3 TC2=5E-6)
.MODEL RSLCMOD RES (TC1=2.5E-3 TC2=4.5E-6)
.MODEL RSOURCEMOD RES (TC1=1.0E-3 TC2=1E-6)
.MODEL RVTHRESMOD RES (TC1=-2.013E-3 TC2=-7E-6)
.MODEL RVTEMPMOD RES (TC1=-1.5E-3 TC2=1E-6)

.MODEL S1AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-4 VOFF=-3)
.MODEL S1BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-3 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-1.3 VOFF=-0.5)
.MODEL S2BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-0.5 VOFF=-1.3)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SPICE Thermal Model

```
.SUBCKT FDS6612A_THERM TH TL
*THERMAL MODEL SUBCIRCUIT
*REV A - JULY 2003
*MIN PAD RJA

CTHERM1     TH     8      0.005
CTHERM2     8      7      0.05
CTHERM3     7      6      0.10
CTHERM4     6      5      0.35
CTHERM5     5      4      0.45
CTHERM6     4      3      0.50
CTHERM7     3      2      0.55
CTHERM8     2      TL     3.00

RTHERM1     TH     8      5.000
RTHERM2     8      7      6.250
RTHERM3     7      6      7.500
RTHERM4     6      5      8.750
RTHERM5     5      4      10.625
RTHERM6     4      3      11.875
RTHERM7     3      2      31.250
RTHERM8     2      TL     43.750

.ENDS
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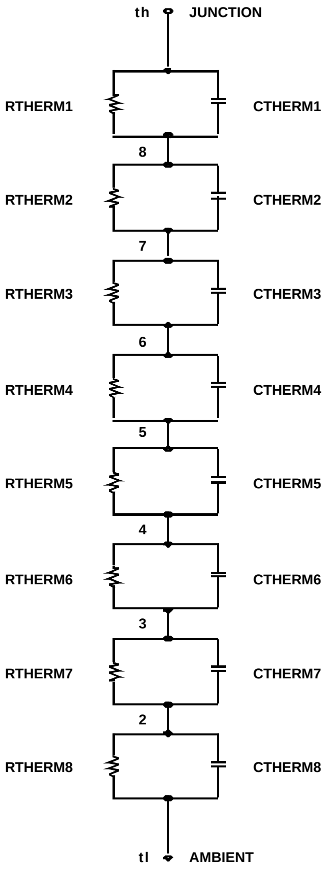
th
JUNCTION
RTHERM1
CTHERM1
8
RTHERM2
CTHERM2
7
RTHERM3
CTHERM3
6
RTHERM4
CTHERM4
5
RTHERM5
CTHERM5
4
RTHERM6
CTHERM6
3
RTHERM7
CTHERM7
2
RTHERM8
CTHERM8
tl
AMBIENT

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SyncFET™
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VCX™

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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