



September 2005

# FDU6676AS

## N-Channel PowerTrench<sup>®</sup> SyncFET<sup>™</sup>

### 30V, 90A, 5.8mΩ

#### General Description

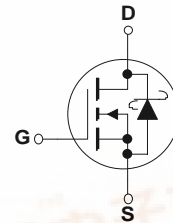
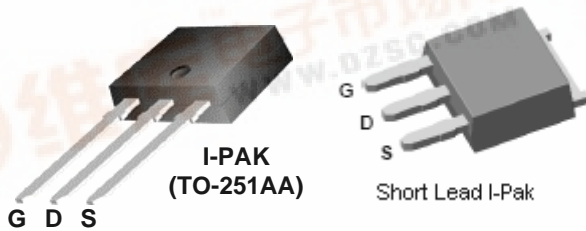
The FDU6676AS is designed to replace a single MOSFET and Schottky diode in synchronous DC/DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low  $R_{DS(ON)}$  and low gate charge. The FDU6676AS includes a patented combination of a MOSFET monolithically integrated with a Schottky diode using Fairchild's monolithic SyncFET technology.

#### Applications

- DC/DC converter

#### Features

- $R_{DS(ON)} = 5.8m\Omega$  Max,  $V_{GS} = 10V$
- $R_{DS(ON)} = 7.3m\Omega$  Max,  $V_{GS} = 4.5V$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Low Gate Charge
- High power and current handling capability
- Includes SyncFET Schottky diode



#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current	-Continuous (Note 1a)	90
		-Pulsed	100
$P_D$	Power Dissipation for Single Operation (Note 1)	(Note 1a)	3.1
		(Note 1b)	1.3
			70
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance junction to Case (Note 1)	1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance junction to Ambient (Note 1a)	45	
$R_{\theta JA}$	Thermal Resistance junction to Ambient (Note 1b)	96	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDU6676AS	FDU6676AS	I-PAK (TO-251)	Tube	N/A	75
FDU6676AS	FDU6676AS_NL (Note 4)	I-PAK (TO-251)	Tube	N/A	75
FDU6676AS	FDU6676AS_F071 (Note 5)	I-PAK (TO-251)	Tube	N/A	75



### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Drain-Source Avalanche Ratings (Note 2)

$W_{DSS}$	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15\text{V}, I_D = 16\text{A}$		108	250	mJ
$I_{AR}$	Drain-Source Avalanche Current				16	A

#### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		29		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$			500	$\mu\text{A}$
		$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$		13		$\text{mA}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

#### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 16\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 10\text{A}$ $V_{GS} = 10\text{V}, I_D = 16\text{A}, T_J = 125^\circ\text{C}$		4.8 5.8 7.7	5.8 7.3 9.6	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 16\text{A}$		67		S

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$		2470		pF
$C_{oss}$	Output Capacitance			710		pF
$C_{rss}$	Reverse Transfer Capacitance			260		pF
$R_G$	Gate Resistance	$V_{GS} = 100\text{mV}, f = 1.0\text{MHz}$		1.8		$\Omega$

#### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 1\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\ \Omega$		12	22	ns
$t_r$	Turn-On Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			50	80	ns
$t_f$	Turn-Off Fall Time			25	40	ns
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}, I_D = 1\text{A},$ $V_{GS} = 4.5\text{V}, R_{GEN} = 6\ \Omega$		20	32	ns
$t_r$	Turn-On Rise Time			24	38	ns
$t_{d(off)}$	Turn-Off Delay Time			34	54	ns
$t_f$	Turn-Off Fall Time			26	42	ns
$Q_g$	Total Gate Charge, $V_{GS} = 10\text{V}$	$V_{DS} = 15\text{V}, I_D = 16\text{A}$		46	64	nC
$Q_g$	Total Gate Charge, $V_{GS} = 5\text{V}$			25	35	nC
$Q_{gs}$	Gate-Source Charge			6		nC
$Q_{gd}$	Gate-Drain Charge			7		nC

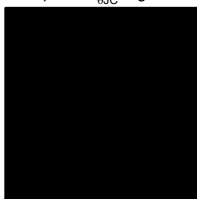
## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.3	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2)		0.4	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 16\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$		28		ns
$Q_{rr}$	Diode Reverse Recovery Charge			19		nC

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $R_{\theta JA} = 45^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $R_{\theta JA} = 96^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

- Maximum current is calculated as: 
$$\sqrt{\frac{P_D}{R_{DS(on)}}}$$

where  $P_D$  is maximum power dissipation at  $T_C = 25^\circ\text{C}$  and  $R_{DS(on)}$  is at  $T_{J(max)}$  and  $V_{GS} = 10\text{V}$ . Package current limitation is 21A

- FDU6676AS\_NL is a lead free product. The FDU6676AS\_NL marking will appear on the reel label.
- FDU6676AS\_F071 is a lead free product. The FDU6676AS\_F071 marking will appear on the reel label.

### Typical Characteristics

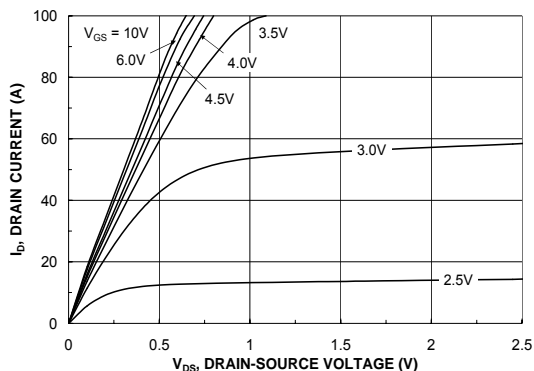


Figure 1. On-Region Characteristics

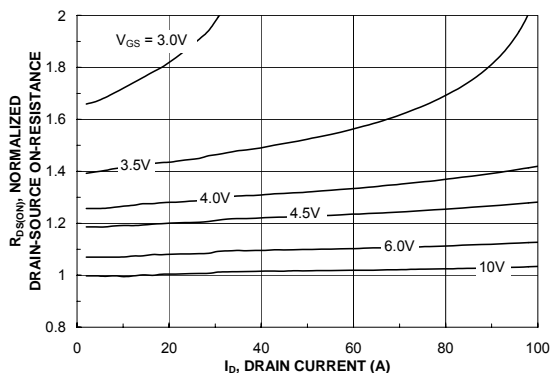


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

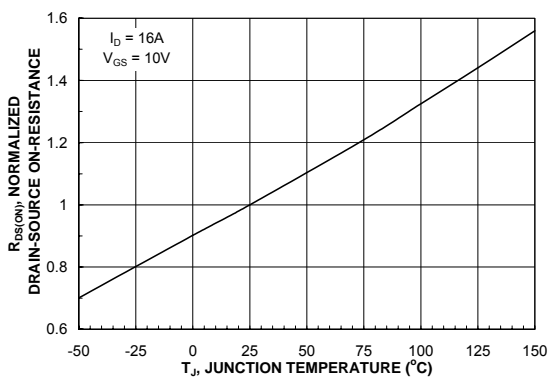


Figure 3. On-Resistance Variation with Temperature

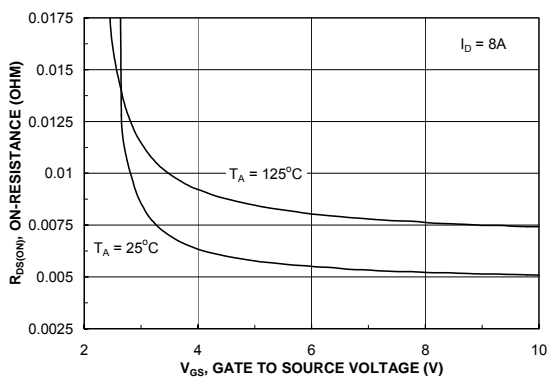


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

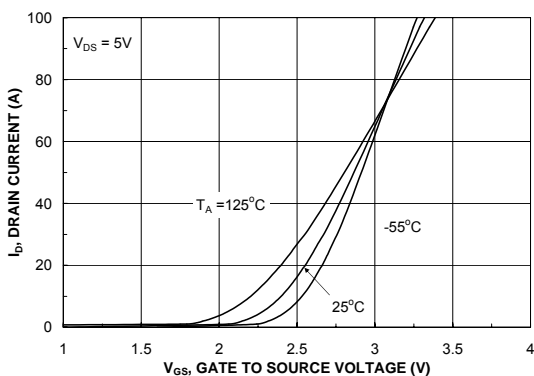


Figure 5. Transfer Characteristics

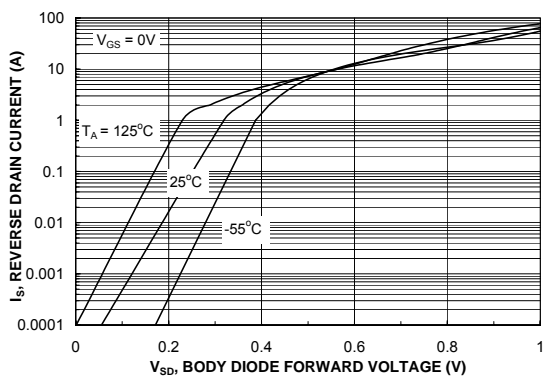
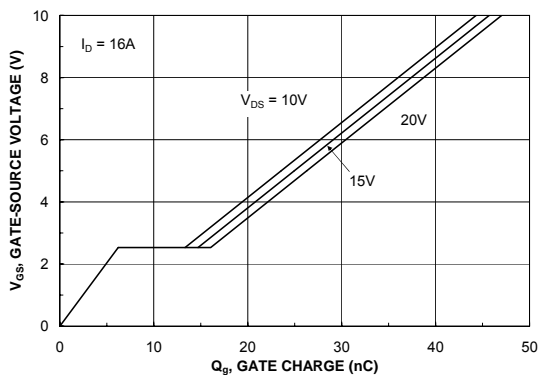
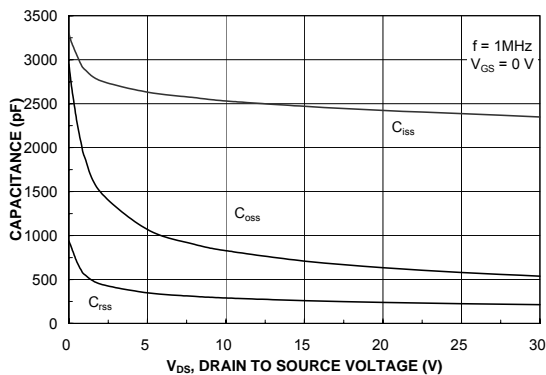


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

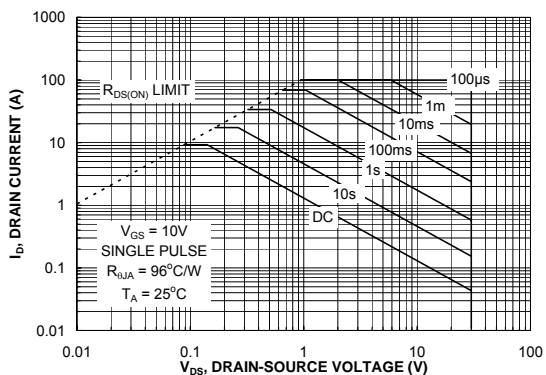
## Typical Characteristics



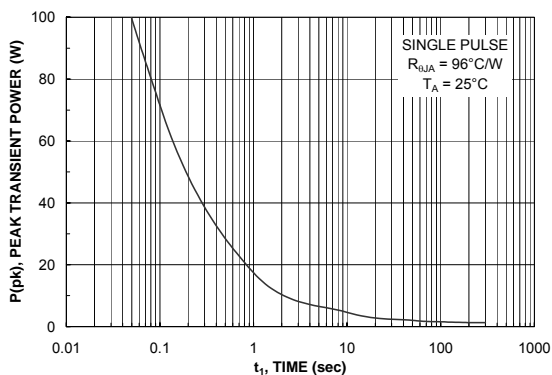
**Figure 7. Gate Charge Characteristics**



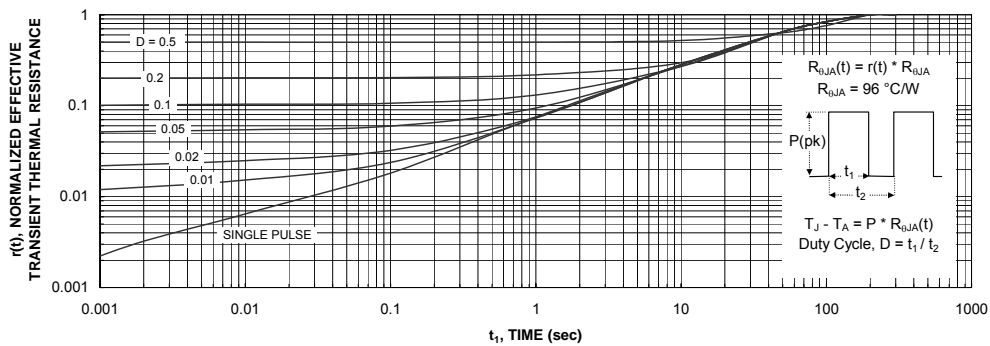
**Figure 8. Capacitance Characteristics**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Single Pulse Maximum Power Dissipation**



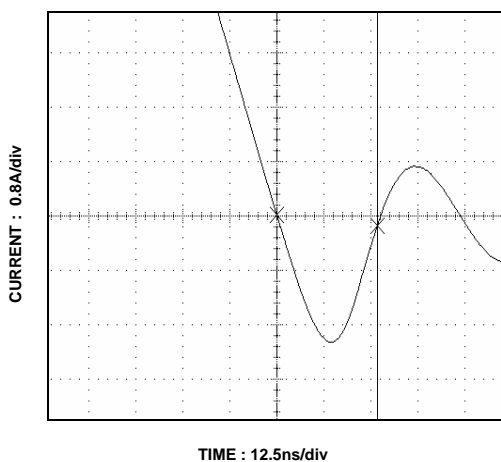
**Figure 11. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

## Typical Characteristics (continued)

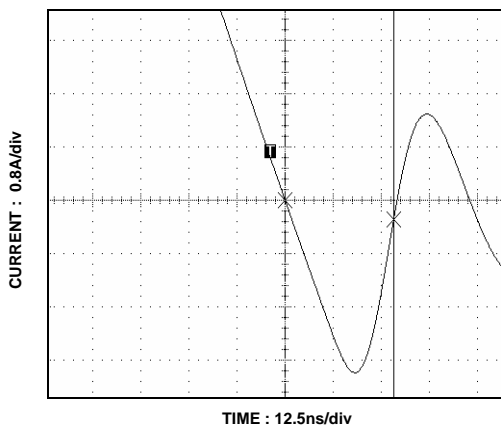
### SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDU6676AS.



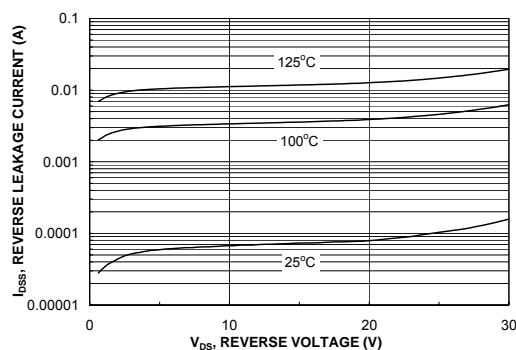
**Figure 12. FDU6676AS SyncFET Body Diode Reverse Recovery Characteristic.**

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDU6676A).



**Figure 13. Non-SyncFET (FDU6676A) Body Diode Reverse Recovery Characteristic.**

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.



**Figure 14. SyncFET Body Diode Reverse Leakage Versus Drain-Source Voltage and Temperature.**

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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