FAIRCHILD SEMICONDUCTOR®

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FMS6403

Triple Video Drivers with Selectable HD/PS/SD/ Bypass Filters for RGB and YPbPr Signals

Features

- Three video anti-aliasing or reconstruction filters
- 2:1 Mux inputs for YPbPr and RGB inputs
- Supports D1, D2, D3 and D4 video D-connector (EIAJ CP-4120)
- Selectable 8MHz/15MHz/30MHz 6th order filters plus bypass
- Works with SD (480i), Progressive (480p) and HD (1080i/ 720p)
- AC-coupled inputs include DC restore /bias circuitry
- All outputs can drive AC or DC coupled 75Ω loads and provide either 0dB or 6dB of gain
- 0.40% differential gain, 0.25° differential phase
- Lead (Pb)-free TSSOP-20 packaging

Applications

- Progressive scan
- Cable set top boxes
- Home theaters
- Satellite set top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

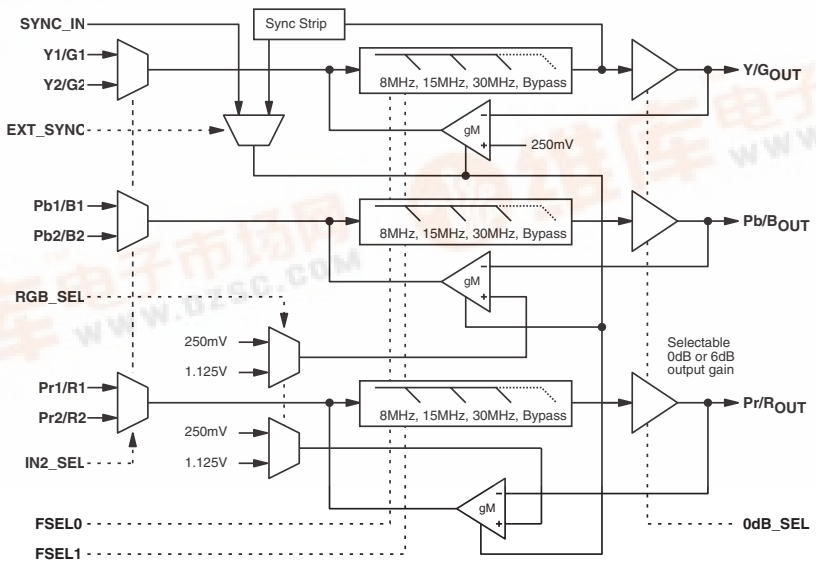
Description

The FMS6403 offers comprehensive filtering for TV, set top box or DVD applications. This part consists of a triple 6th order filter with selectable 30MHz, 15MHz, or 8MHz cutoff frequencies. The filters may also be bypassed so that the bandwidth is limited only by the output amplifiers.

A 2 to 1 multiplexer is provided on each filter channel. The triple filters are intended for YPbPr and RGB signals. The DC clamp levels are set according to the RGB_SEL control input. YPbPr sync tips are clamped to 250mV, 1.125V and 1.125V respectively while RGB sync tips are all clamped to 250mV. Sync clamp timing can be derived from the Y/G inputs or from the external SYNC_IN pin. The 8MHz and 15MHz filter settings support bi-level sync while the 30MHz filter setting and bypass mode support tri-level sync.

All channels nominally accept AC coupled 1Vpp signals. Selectable 0dB or 6dB gain allows the outputs to drive 1Vpp or 2Vpp signals into AC or DC coupled terminated loads with a 1Vpp input. Input signals cannot exceed 1.5Vpp and outputs cannot exceed 2.5Vpp.

Functional Block Diagram



DC Electrical Specifications

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current[1]	V_{CC} no load		90	130	mA
V_i	Input Voltage Max			1.5		V_{pp}
V_{il}	Digital Input Low[1]	F_{SEL0}, F_{SEL1}, RGB_SEL, 0dB_SEL, EXT_SYNC, IN2_SEL, SYNC_IN	0		0.8	V
V_{ih}	Digital Input High[1]	F_{SEL0}, F_{SEL1}, RGB_SEL, 0dB_SEL, EXT_SYNC, IN2_SEL, SYNC_IN	2.4		V_{CC}	V
V_{CLAMP1}	Output Clamp Voltage	R,G,B,Y		250		mV
V_{CLAMP2}	Output Clamp Voltage	Pb and Pr		1.125		V
PSRR	Power Supply Rejection Ratio	DC (All Channels)		-40		dB

Standard Definition Electrical Specifications

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 0, F_{SEL1} = 0, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{SD}	SD Gain, 0dB_SEL = '0'[1]	All Channels SD Mode	5.6	6.0	6.4	dB
AV_{SD}	SD Gain, 0dB_SEL = '1'[1]	All Channels SD Mode	-0.4	0	0.4	dB
f_{1dBSD}	-1dB Bandwidth for SD[1]	All Channels	5.5	7.6		MHz
f_{CSD}	-3dB Bandwidth for SD	All Channels		8.5		MHz
f_{SBSD}	Attenuation: SD (Stopband Reject)[1]	All Channels at f = 27MHz	40	56		dB
dG	Differential Gain	All Channels		0.40		%
dϕ	Differential Phase	All Channels		0.25		°
THD	Output Distortion (All Channels)	V_{out} = 1.8V_{pp} at 1MHz		0.4		%
X_{TALK}	Crosstalk (Channel-to-Channel)	at 1.0MHz		-68		dB
IN_{MUXISO}	IN_{MUX} Isolation	at 1.0MHz		-70		dB
SNR	Signal-to-Noise Ratio	All Channels, NTC-7 Weighting, 4.2MHz lowpass, 100kHz Highpass		74		dB
t_{pdSD}	Propagation Delay for SD	Delay from Input to Output at 4.5MHz		80		ns
T1	SYNC to SYNC_IN Delay			10		ns
T2	SYNC_IN Min Pulse Width			4		µs

Progressive Scan (PS) Electrical Specifications

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 1, F_{SEL1} = 0, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{PS}	PS Gain, 0dB_SEL = '0'[1]	All Channels PS Mode	5.6	6.0	6.4	dB
AV_{PS}	PS Gain, 0dB_SEL = '1'[1]	All Channels PS Mode	-0.4	0	0.4	dB
f_{1dBPS}	-1dB Bandwidth for PS[1]	All Channels	10	15		MHz

Note:
1. 100% tested at 25°C.

Progressive Scan (PS) Electrical Specifications (Continued)

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 1, F_{SEL1} = 0, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPS}	-3dB Bandwidth for PS	All Channels		17		MHz
f_{SBPS}	Attenuation: PS (Stopband Reject)[1]	All Channels at f = 54MHz	40	48		dB
t_{pdPS}	Propagation Delay for PS	Delay from Input to Output at 10MHz		45		ns
T1	SYNC to SYNC_IN Delay			10		ns
T2	SYNC_IN Min Pulse Width			2		µs

High Definition Electrical Specifications

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 0, F_{SEL1} = 1, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{HD}	HD Gain, 0dB_SEL = '0'[1]	All Channels HD Mode	5.6	6.0	6.4	dB
AV_{HD}	HD Gain, 0dB_SEL = '1'[1]	All Channels HD Mode	-0.4	0	0.4	dB
f_{1dBHD}	-1dB Bandwidth for HD[1]	All Channels	20	29		MHz
f_{CHD}	-3dB Bandwidth for HD	All Channels		33		MHz
f_{SBHD}	Attenuation: HD (Stopband Reject)[1]	All Channels at f = 74.25MHz	30	40		dB
t_{pdHD}	Propagation Delay for HD	Delay from Input to Output at 20MHz		26		ns
T1	SYNC to SYNC_IN Delay			10		ns
T2	SYNC_IN Min Pulse Width			1.5		µs

Unfiltered 1080p Bypass (Wide Bandwidth) Electrical Specifications

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 1, F_{SEL1} = 1, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{WB}	Gain, 0dB_SEL = '0'[1]	All Channels Bypass Mode	5.6	6.0	6.4	dB
AV_{WB}	Gain, 0dB_SEL = '1'[1]	All Channels Bypass Mode	-0.4	0	0.4	dB
f_{1dBWB}	-1dB Bandwidth	All Channels		63		MHz
f_{CWB}	-3dB Bandwidth	All Channels		91		MHz
t_{pdWB}	Propagation Delay	Delay from Input to Output at 20MHz		10		ns

Note:
1. 100% tested at 25°C.

Absolute Maximum Ratings (beyond which the device may be damaged)

Parameter	Min	Max	Units
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
Output Current, Any One Channel (Do not exceed)		60	mA

Note:
Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.

Reliability Information

Parameter	Min	Typ	Max	Units
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance (θ_{JA}), JEDEC Standard Multi-layer Test Boards, Still Air		74		°C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temperature Range	0		70	°C
V_{CC} Range	4.75	5.0	5.25	V
Input Source Resistance (R_{source})			150	Ω

Standard Definition Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 0, F_{SEL1} = 0, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 1. SD Frequency Response

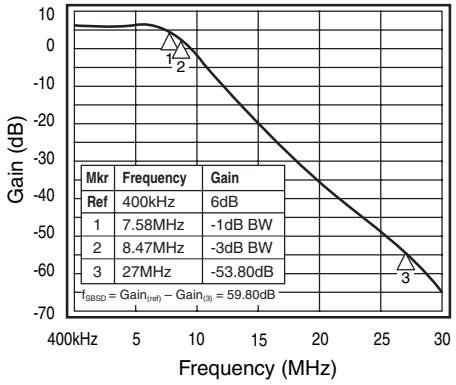


Figure 2. SD Group Delay vs. Frequency

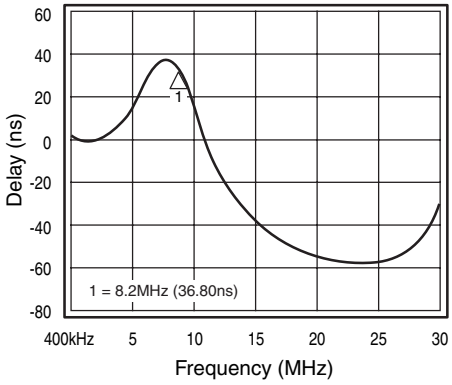


Figure 3. SD Noise vs. Frequency

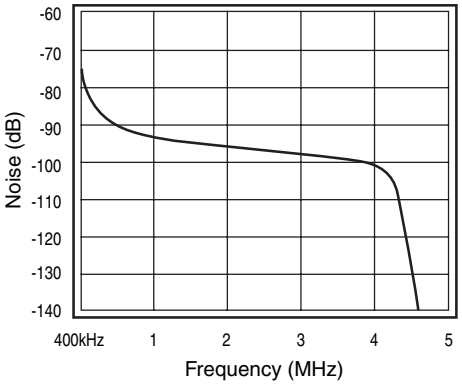


Figure 4. SD Differential Gain

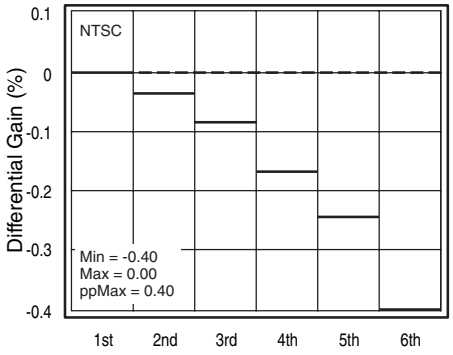
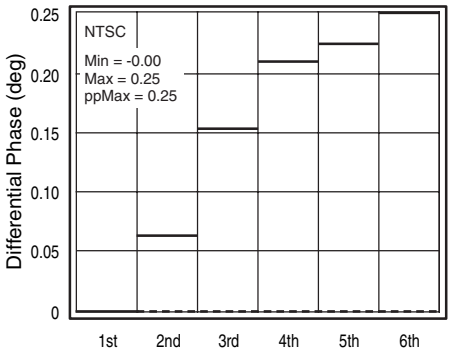


Figure 5. SD Differential Phase



Progressive Scan (PS) Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 1, F_{SEL1} = 0, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 6. PS Frequency Response

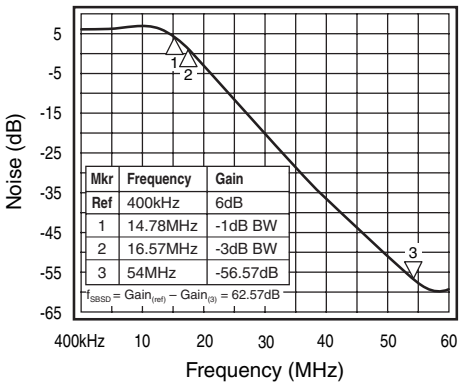
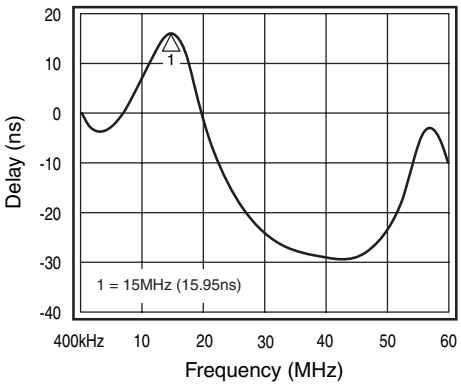


Figure 7. PS Group Delay vs. Frequency



High Definition Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 0, F_{SEL1} = 1, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 8. HD Frequency Response

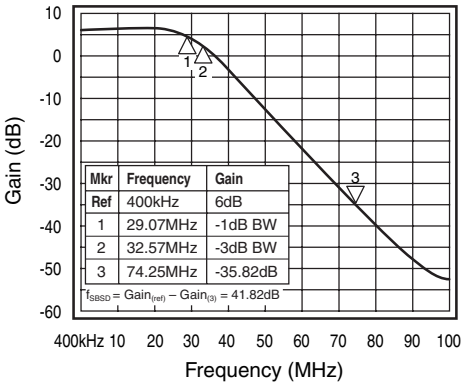
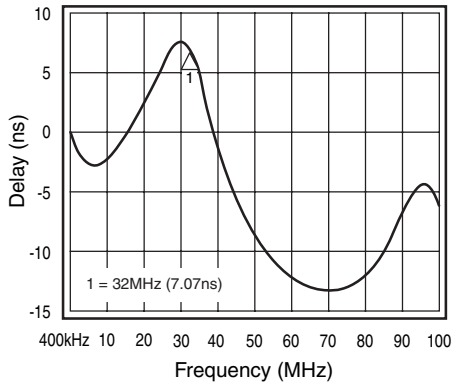


Figure 9. HD Group Delay vs. Frequency



Unfiltered 1080p Bypass (WB) Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{pp}, V_{CC} = 5.0V, F_{SEL0} = 1, F_{SEL1} = 1, 0dB_SEL = 0 (gain = 6dB), R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 10. Bypass Mode Frequency Response

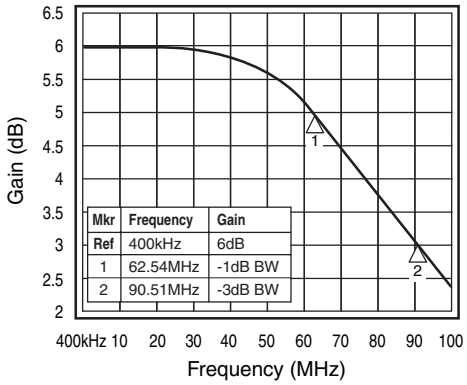
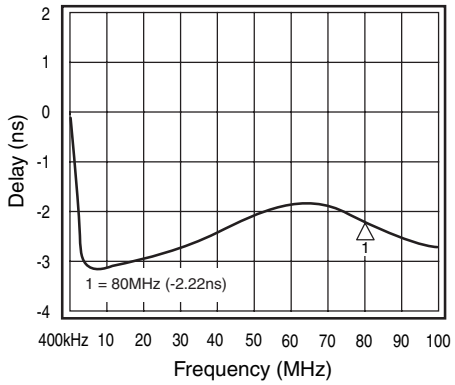
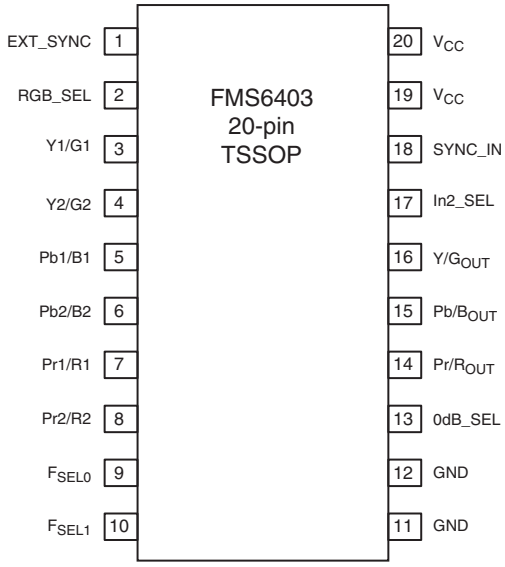


Figure 11. Bypass Mode Group Delay vs. Frequency



Pin Configuration



Pin#	Pin	Type	Description
1	EXT_SYNC	Input	Selects the external SYNC_IN signal when set to logic ‘1’, do not float
2	RGB_SEL	Input	Selects RGB clamp levels when set to logic ‘1’, YPbPr clamp levels when set to logic ‘0’, do not float
3	Y1/G1	Input	Y or G input 1 - may be connected to a signal which includes sync
4	Y2/G2	Input	Y or G input 2 - may be connected to a signal which includes sync
5	Pb1/B1	Input	Pb or B input 1
6	Pb2/B2	Input	Pb or B input 2
7	Pr1/R1	Input	Pr or R input 1
8	Pr2/R2	Input	Pr or R input 2
9	F_{SEL0}	Input	Selects filter corner frequency or bypass, see table, do not float
10	F_{SEL1}	Input	Selects filter corner frequency or bypass, see table, do not float
11	GND	Input	Must be tied to Ground, do not float
12	GND	Input	Must be tied to Ground, do not float
13	0dB_SEL	Input	Selects output gain of 0dB when set to logic ‘1’, 6dB when set to logic ‘0’, do not float
14	Pr/R_{OUT}	Output	Pr or R output
15	Pb/B_{OUT}	Output	Pb or B output
16	Y/G_{OUT}	Output	Y or G output
17	IN2_SEL	Input	Selects mux input 2 when set to logic ‘1’, mux input 1 when set to logic ‘0’, do not float
18	SYNC_IN	Input	External sync input signal, square wave crossing V_{il} and V_{ih} input thresholds, do not float
19	V_{CC}	Input	+5V supply, do not float
20	V_{CC}	Input	+5V supply, do not float

Gain Settings

0dB_SEL, Pin 13	Gain (dB)	V_{IN}*	V_{OUT}*
0	6	$1V_{pp}$	$2V_{pp}$
1	0	$1V_{pp}$	$1V_{pp}$

* Video level, does not include clamp voltage which will offset the input above ground.

Sync Settings

EXT_SYNC, Pin1	Sync Source
0	Y/G input, Pin 3/4
1	SYNC_IN input, Pin 2

Filter Settings

F_{SEL1}, Pin 10	F_{SEL0}, Pin 9	Filter -3dB Freq	Video Format	Sync Format
0	0	8MHz	SD, 480i	Bi-level, 4.7µs pulse width
0	1	15MHz	PS, 480p	Bi-level, 2.35µs pulse width
1	0	32MHz	HD, 1080i, 720p	Tri-level, 589ns pulse width
1	1	Filter Bypass	Unfiltered 1080p	Tri-level, 290ns, pulse width

Clamp Settings

RGB_SEL, Pin 2	Input	Output	Clamp Voltage
0	Y1, Pin 3	Y, Pin 16	250mV
	Pb1, Pin 5	Pb, Pin 15	1.125V
	Pr1, Pin 7	Pr, Pin 14	1.125V
1	G1, Pin 3	G, Pin 16	250mV
	B1, Pin 5	B, Pin 15	250mV
	R1, Pin 7	R, Pin 14	250mV

Functional Description

Introduction

The FMS6403 is a next generation filter solution from Fairchild Semiconductor addressing the expanding filtering needs for televisions, set top boxes, and DVD players including progressive scan capability. The product provides selectable filtering with cutoff frequencies of 30MHz, 15MHz, and 8.0MHz for all three channels. In addition, the filters can be bypassed for wider bandwidth applications. The FMS6403 allows consumer devices to support a variety of resolution standards with the same hardware.

Multiplexers on the channel inputs are controlled by the IN2_SEL pin. The RGB_SEL pin can be used to set the sync tip clamp voltages for YPbPr or RGB applications. All three channels are set for 250mV sync tips to reduce DC-coupled power dissipation for RGB inputs. The lower output bias voltage is not suitable for the PbPr outputs so for YPbPr inputs these signals are clamped to 1.125V while Y is still clamped to 250mV. Sync tip clamping voltages are set by forcing the desired DC bias level during the active sync period. For systems without sync on Y/G, an external sync input is provided. If sync exists on one input Y/G signal but not on the other Y/G input signal, the IN2_SEL and EXT_SYNC control inputs may be wired together on the PCB to switch the sync source with the input source. Both standard definition (bi-level) and high definition (tri-level) sync are supported at the Y/G inputs and SYNC_IN depending on the FSEL[1:0] inputs. See the *Sync Processing* section for further details.

Standard definition (480i) and progressive (480p) signals are clamped by forcing the signal to the desired voltage during the sync pulse. For signals with sync, the sync tip itself will be forced to the clamp voltage (typically 250mV). When high definition sync is present (tri-level sync) the sync tip duration is too short to allow this approach. In order to accurately clamp HD signals, the sync pulse starts a timer and the actual clamping is done at the blanking level right after the sync pulse. The sync tip will still typically be placed at 250mV if its amplitude is 300mV.

All three outputs are driven by amplifiers with selectable gains of 0dB or +6dB. The gain is set with the 0dB_SEL pin. These amplifiers can drive two terminated video loads (75Ω) to 2Vpp with a 1Vpp input when set to 6dB gain. The input range is limited to $1.5V_{pp}$ and the output range is limited to $2.5V_{pp}$.

All control inputs must be driven high or low. Do not leave them floating.

External SYNC Mode

The FMS6403 can properly recover sync timing from video signals that include sync. If the Y-input video signals does not include sync, the FMS6403 can be used in External SYNC Mode. When the FMS6403 is used in external sync mode, (EXT_SYNC pin is high), a pulsed input must be applied to the SYNC_IN pin. If there is no video signal present, therefore no sync signal present, there must still be an input applied to the SYNC_IN pin. When there is no video signal on the video inputs SYNC_IN can be a sync pulse every 60µs to mimic the slowest sync in a regular video signal. The following two sections discuss the sync processing and timing required in more detail.

SD and Progressive Scan Video Sync Processing

The FMS6403 must control the DC offset of AC-coupled input signals since the average DC level of video varies with image content. If the input offset is allowed to wander, the common mode input range of the amplifiers can be exceeded leading to signal distortion. DC offset adjustment is referred to as clamping or in some cases, biasing, and must be done at the correct time during each video line. The optimum time is during the sync pulse since it is the lowest input voltage. This approach works well for 480i and 480p signals since the sync tip duration is long enough to allow the DC-offset errors to be compensated from line to line. The DC-offset of the sync tip is adjusted as illustrated in Figure 12 by forcing a current on the input during the sync pulse. The sync tip will be clamped to approximately 250mV. Signals like Pb and Pr with a symmetric voltage range (±350mV) will be clamped to approximately 1.125V. Note that the following diagrams illustrate DC restore functionality and indicate output voltage levels for both 0dB and 6dB gain ($1V_{pp}$ and $2V_{pp}$ video signals at the FMS6403 output pin).

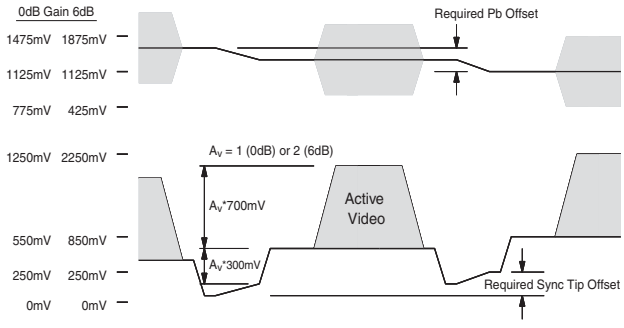


Figure 12. Bi-Level Sync Tip Clamping and Bias

In some cases, the sync voltage may be compressed to less than the nominal 300mV value. The FMS6403 can successfully recover SD and Progressive Scan sync which is greater than 100mV (compressed to 33% of nominal).

The FMS6403 can properly recover sync timing from luma and green which include sync. If none of the video signals

includes sync, the EXT_SYNC control input can be set high and an external sync signal must be input on the SYNC_IN pin. Refer to the External Sync section for more details. The timing required for this operating mode is shown in Figure 13. SYNC timings, T1 and T2, are defined in the SD Electrical Specifications table on page 2.

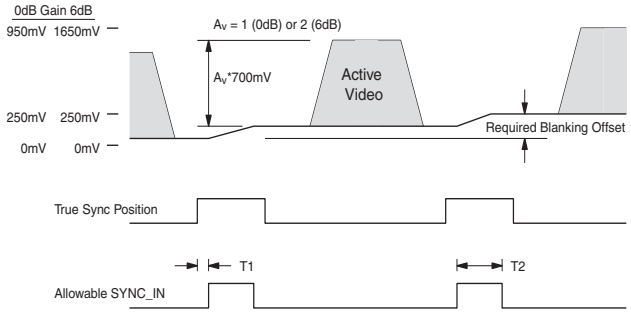


Figure 13. Bi-Level External Sync Clamping and Bias

HD and Bypass Mode Video Sync Processing

When the input signal is a high definition signal, the tri-level sync pulse is too short to allow proper clamp operation. Rather than clamp during the sync pulse, the sync pulse is located and the signal is clamped to the blanking level. This is done in such a way that the sync tip will still be set to approximately 250mV for signals with 300mV sync tip amplitude. The EXT_SYNC control input selects the sync stripper output or the SYNC_IN pin for use by the clamp circuit.

NOTE: The SYNC_IN timing for HD signals is different than the timing for SD or PS signals.

For HD signals, the SYNC_IN signal must be high when the clamp must be active. This is during the time immediately after the sync pulse while the signal is at the blanking level. This operation is shown in Figure 14. Note that the following diagrams illustrate DC restore functionality and indicate output voltage levels for both 0dB and 6dB gain ($1V_{pp}$ and $2V_{pp}$ video signals at the FMS6403 output pin). SYNC timings, T1 and T2, are defined in the HD Electrical Specifications table on page 3.

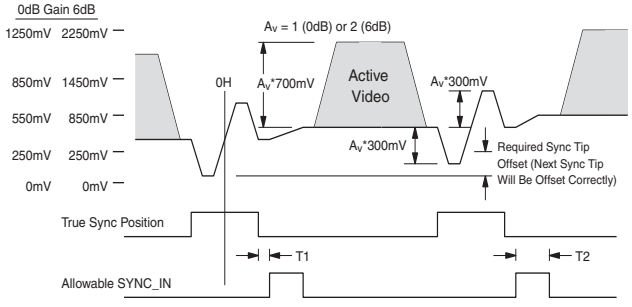


Figure 14. Tri-Level Blanking Clamp

NOTE: Tri-level sync may only be compressed 5%. If HD sync is compressed more than 5% it may not be properly located.

Sync Timing

Normally, the FMS6403 will respond to bi-level sync and clamp the sync tip during period 'B' in Figure 15(a). When the filters are switched to high definition mode (30MHz) or bypass mode the sync processing will respond to tri-level sync and clamp to the blanking level during period 'C' in Figure 15(b).

NOTE: The diagram indicates SYNC timings at the output pin.

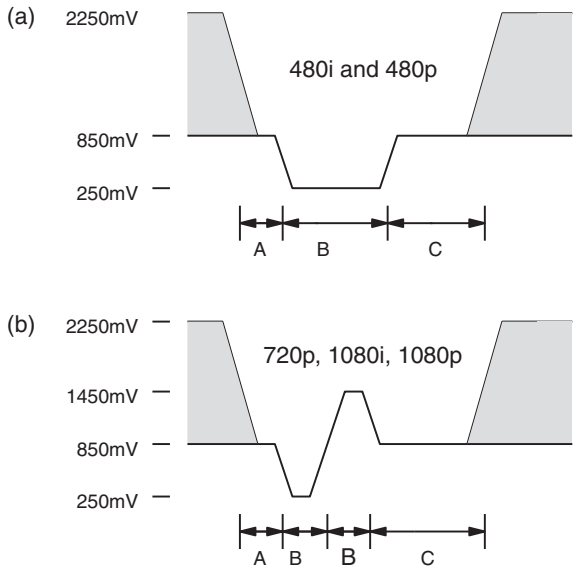


Figure 15. Sync Timing; Bi-Level (a), Tri-Level (b)

The tri-level sync pulse is located such that the broad pulses in the vertical interval do not trigger the clamp. In order to improve the system settling at turn-on, the broad pulses will be clamped to just above ground. Once the broad pulses (and tri-level sync tips) are above ground, the normal clamping process takes over and clamps to the blanking level during period 'C' in Figure 15(b).

The FMS6403 is designed to support the video standards and associated sync timings shown in Table 1, (additional standards such as 483p59.94 will also work correctly). The Filter Settings table from page 9 is repeated on page 12 for convenience..

Filter Settings

F_{SEL1}, Pin 10	F_{SEL0}, Pin 9	Filter -3dB Freq	Video Format	Sync Format
0	0	8MHz	SD, 480i	Bi-level, 4.7µs pulse width
0	1	15MHz	PS, 480p	Bi-level, 2.35µs pulse width
1	0	32MHz	HD, 1080i, 720p	Tri-level, 589ns pulse width
1	1	Filter Bypass	Unfiltered 1080p	Tri-level, 290ns, pulse width

Table I

Format	Refresh	Sample Rate	Period (T)	A	B	C	H-Rate
480i	30Hz	13.5MHz	74ns	20T = 1.5µs	64T = 4.7µs	61T = 4.5µs	15.75kHz
480p	60Hz	27MHz	37ns	20T = 750ns	64T = 2.35µs	61T = 2.25µs	31.5kHz
720p	60Hz	74.25MHz	13.4ns	70T = 938ns	40T = 536ns	220T = 2.95µs	45kHz
1080i	30Hz	74.25MHz	13.4ns	44T = 589ns	44T = 589ns	148T = 1.98µs	33.75kHz
1080p	60Hz	148.5MHz	6.7ns	44T = 296ns	44T = 296ns	148T = 996ns	67.5kHz

Note: Timing values are approximate for 30Hz/60Hz refresh rates.

Application Information

Input Circuitry

The DC restore circuit in the FMS6403 requires a source impedance ($R_{source} = R_S \parallel R_T$) of less than or equal to 150Ω for correct operation. Driving the FMS6403 with a high-impedance source (e.g. a DAC loaded with 330Ω) will not yield optimum results. Refer to the Typical Application Circuit diagram on page 13 for more details.

Output Drive

The FMS6403 is specified to operate with output currents typically less than 60mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to approximately 100mA and should withstand brief duration short circuit conditions, however this capability is not guaranteed.

The maximum specified input voltage of $1.5V_{pp}$ can be sustained for all inputs. When the input is clamped to 1.125V, this does not result in a meaningful output signal. With a gain of 6dB, the output should be 1.125V ±1.5V which is not possible since the output cannot drive below ground. This condition will not damage the part; however, the output will be clipped. For signals which are clamped to 250mV, this does not occur.

Signals that are at midscale during SYNC (Pb and Pr) must be clamped to 1.125V and signals that are at their lowest during SYNC (Y, R, G, B) must be clamped to 250mV for proper operation. Clamping a Pr signal to 250mV will result in clipping the bottom of the signal.

The 220uF capacitor coupled with the 150Ω termination, as shown in the Typical Application Circuit of Figure 5, forms a high pass filter that blocks the DC while passing the video frequencies and avoiding tilt. Any value lower than 220µF will create problems, such as video tilt. Higher values, such as 470µF - 1000µF are the most optimal output coupling capacitor. By AC coupling, the average DC level is zero. Thus, the output voltages of all channels will be centered around zero.

Sync Recovery

The FMS6403 will typically recover bi-level sync with amplitude greater than 100mV (33% compressed relative to the nominal 300mV amplitude). The FMS6403 looks for the lowest signal voltage and clamps this to approximately 250mV at the output.

Tri-level sync may not be compressed more than 5% (15mV) for correct operation. Tri-level sync is located by finding the edges of the tri-level pulse and running a timer to operate the clamp during the back porch interval.

The selection of the 8MHz or 15MHz filters enables bi-level sync recovery. Selection of the 30MHz filter or bypass mode enables tri-level sync recovery. Bi-level and tri-level sync recovery are not interchangeable. See the detailed sync processing section for more information.

Power Dissipation

TheFMS6403 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6403's power dissipation and internal temperature rise.

$T_j = T_A + P_d \bullet \Theta_{JA}$

where $P_d = P_{CH1} + P_{CH2} + P_{CH3}$

and $P_{CHx} = V_s \bullet I_{CH} - (V_O^2/R_L)$

where

$V_O = 2V_{in} + 0.280V$

$I_{CH} = (I_{CC} / 3) + \ (V_O/R_L)$

V_{in} = RMS value of input signal

$I_{CC} = 90mA$

$V_s = 5V$

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* Section for more information. The FMS6403 is specified to operate with output currents typically less than 60mA, more than sufficient for a single (150Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief duration short circuit conditions, however this capability is not guaranteed.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6403DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6403DEMO is a 4-layer board with a full power and ground plane. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 10µF and 0.1µF ceramic bypass capacitors
- Place the 10µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package
- Layout channel connections to reduce mutual trace inductance
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs.

If using multiple, low impedance DC coupled outputs, special layout techniques may be employed to help dissipate heat.

For dual-layer boards, place a 0.5" to 1" (1.27cm to 2.54cm) square ground plane directly under the device and on the bottom side of the board. Use multiple vias to connect the ground planes. For multi-layer boards, additional planes (connected with vias) can be used for additional thermal improvements.

Worse case additional die power due to DC loading can be estimated at $(V_{CC}^2/4R_{load})$ per output channel. This assumes a constant DC output voltage of V_{CC}^2. For 5V V_{CC} with a dual DC video load, add 25/(4*75) = 83mW, per channel.

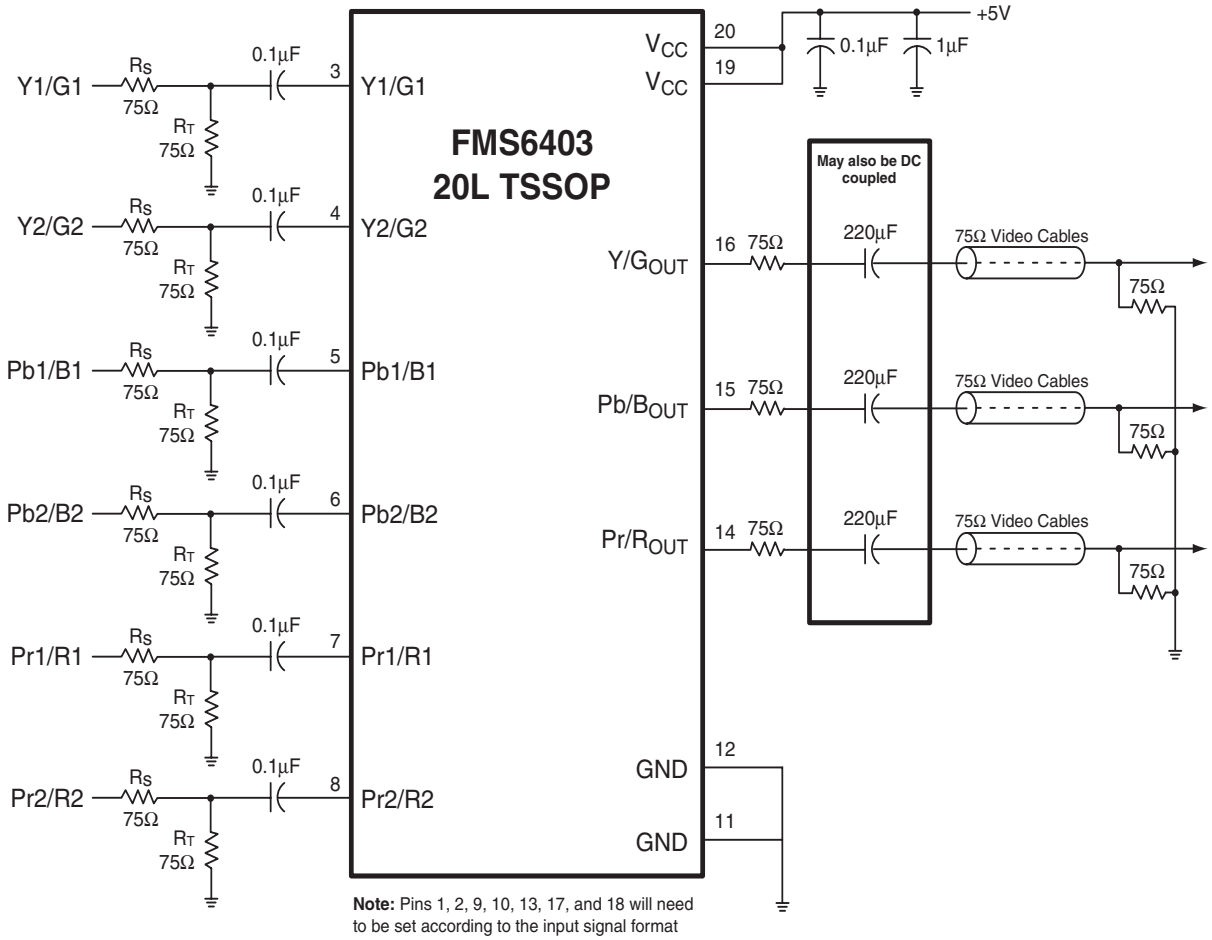
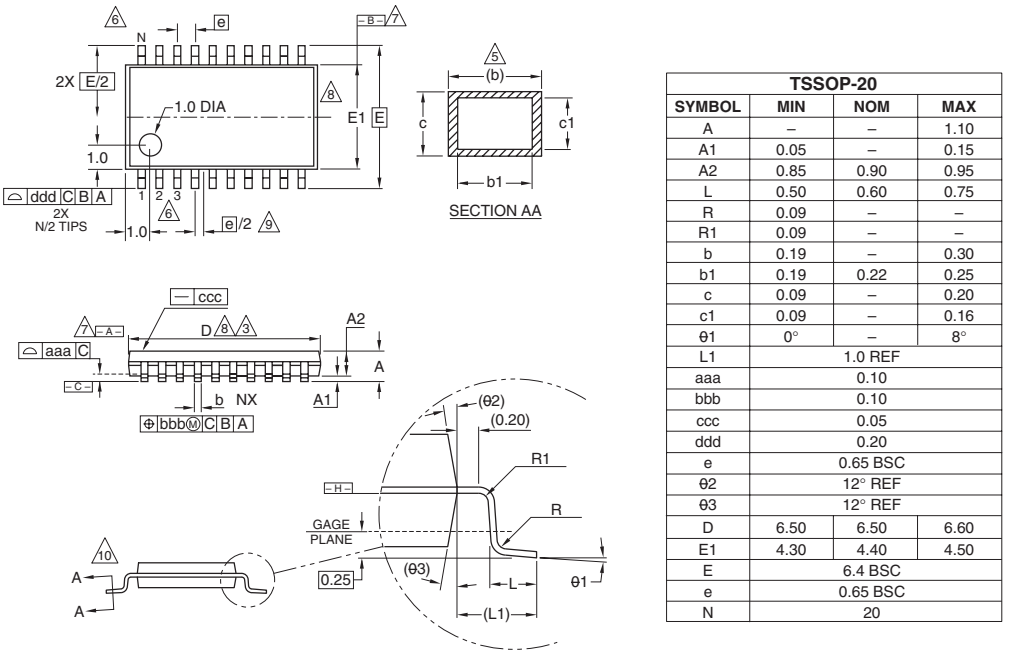


Figure 16. Typical Application Circuit

Package Dimensions

TSSOP-20



TSSOP-20			
SYMBOL	**MIN**	**NOM**	**MAX**
A	–	–	1.10
A1	0.05	–	0.15
A2	0.85	0.90	0.95
L	0.50	0.60	0.75
R	0.09	–	–
R1	0.09	–	–
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	–	0.16
θ1	0°	–	8°
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
θ2	12° REF		
θ3	12° REF		
D	6.50	6.50	6.60
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	20		

NOTES:

1 All dimensions are in millimeters (angle in degrees).

2 Dimensioning and tolerancing per ASME Y14.5–1994.

3 Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .

4 Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.

5 Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar connot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.

6 Terminal numbers are shown for reference only.

7 Datums – A – and – B – to be determined at datum plane – H –.

8 Dimensions "D" and "E1" to be determined at datum plane – H –.

9 This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.

10 Cross sections A – A to be determined at 0.10 to 0.25mm from the leadtip.

Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty
FMS6403	FMS6403MTC20_NL	Yes	TSSOP-20	Tube	94
FMS6403	FMS6403MTC20X_NL	Yes	TSSOP-20	Tape and Reel	2500

Temperature range for all parts: 0°C to +70°C.

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Bottomless™	FPS™	LittleFET™	PowerEdge™	SuperFET™
CoolFET™	FRFET™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CROSSVOLT™	GlobalOptoisolator™	MicroFET™	PowerTrench®	SuperSOT™-6
DOME™	GTO™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	HiSeC™	MICROWIRE™	QS™	SyncFET™
E²CMOS™	I²C™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	*i-Lo*™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
The Power Franchise®		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
Programmable Active Droop™		PACMAN™	SMART START™	VCX™

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