FM18L08

256Kb Bytewide FRAM Memory

Features

256K bit Ferroelectric Nonvolatile RAM

- Organized as 32,768 x 8 bits
- 45 year Data Retention
- Unlimited Read/Write Cycles
- NoDelay™ Writes
- Advanced High-Reliability Ferroelectric Process

Superior to Battery-Backed SRAM

- No Battery Concerns
- Monolithic Reliability
- True Surface Mount Solution, No Rework Steps
- Superior for Moisture, Shock, and Vibration
- Resistant to Negative Voltage Undershoots

SRAM & EEPROM Compatible

- JEDEC 32Kx8 SRAM & EEPROM pinout
- 70 ns Access Time
- 140 ns Cycle Time

Low Power Operation

- 3.0V to 3.65V Operation
- 15 mA Active Current
- 15 µA Standby Current

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 32-pin “Green” TSOP Package
- 28-pin SOIC or DIP Package
- “Green” Packaging Options

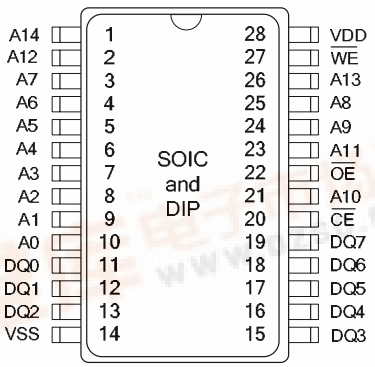
Description

The FM18L08 is a 256-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile and reads and writes like a RAM. It provides data retention for 45 years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make FRAM superior to other types of nonvolatile memory.

In-system operation of the FM18L08 is very similar to other RAM based devices. Read cycle and write cycle times are equal. The FRAM memory, however, is nonvolatile due to its unique ferroelectric memory process. Unlike BBSRAM, the FM18L08 is a truly monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the FM18L08 ideal for nonvolatile memory applications requiring frequent or rapid writes in a bytewide environment. The availability of a surface-mount package improves the manufacturability of new designs, while the DIP package facilitates simple design retrofits. Device specifications are guaranteed over a temperature range of -40°C to +85°C.

Pin Configurations



Ordering Information	
FM18L08-70-TG	70 ns access, 32-pin “Green” TSOP
FM18L08-70-S	70 ns access, 28-pin SOIC
FM18L08-70-P	70 ns access, 28-pin DIP
FM18L08-70-SG	70 ns access, 28-pin “Green” SOIC
FM18L08-70-PG	70 ns access, 28-pin “Green” DIP

This product conforms to specifications per the terms of the Ramtron standard warranty. The product has completed Ramtron’s internal qualification testing and has reached production status.

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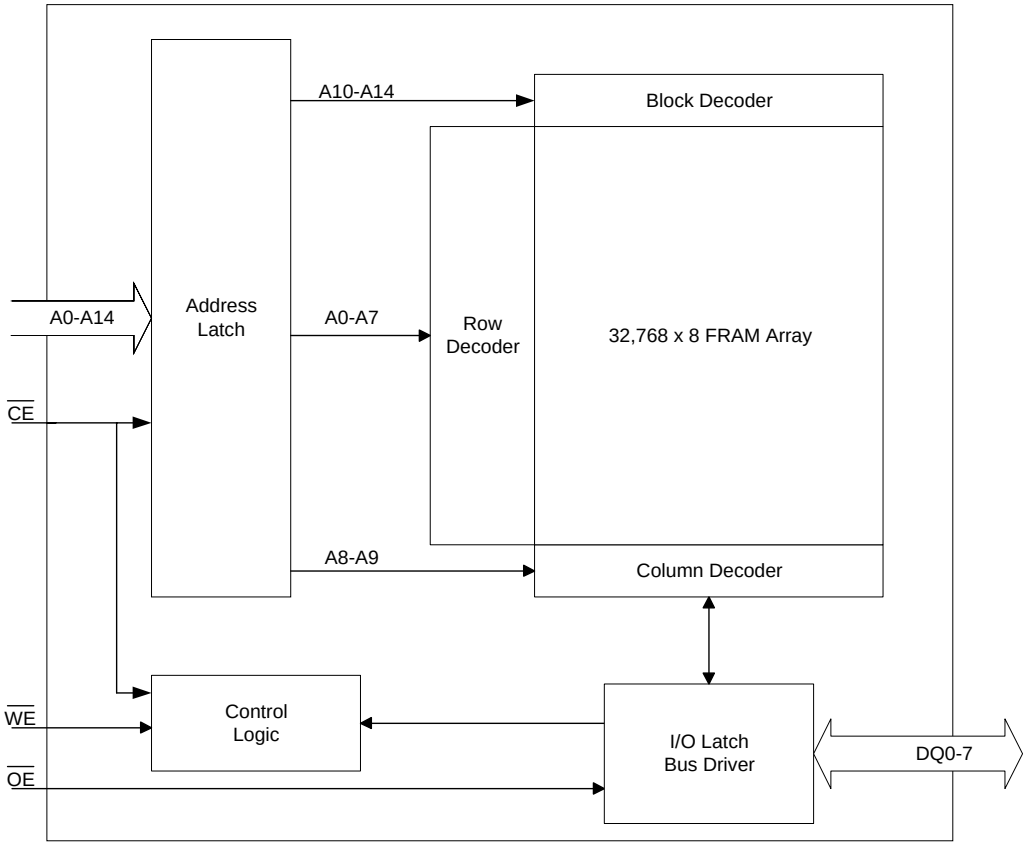


Figure 1. Block Diagram

Pin Description

Pin Name	Type	Pin Description
A0-A14	Input	Address: The 15 address lines select one of 32,768 bytes in the FRAM array. The address value is latched on the falling edge of /CE.
DQ0-7	I/O	Data: 8-bit bi-directional data bus for accessing the FRAM array.
/CE	Input	Chip Enable. /CE selects the device when low. Asserting /CE low causes the address to be latched internally. Address changes that occur after /CE goes low will be ignored until the next falling edge occurs.
/OE	Input	Output Enable: Asserting /OE low causes the FM18L08 to drive the data bus when valid data is available. Deasserting /OE high causes the DQ pins to be tri-stated.
/WE	Input	Write Enable: Asserting /WE low causes the FM18L08 to write the contents of the data bus to the address location latched by the falling edge of /CE.
VDD	Supply	Supply Voltage
VSS	Supply	Ground

Functional Truth Table

/CE	/WE	Function
H	X	Standby/Precharge
↓	X	Latch Address (and Begin Write if /WE=low)
L	H	Read
L	↓	Write

Note: The /OE pin controls only the DQ output buffers.

Overview

The FM18L08 is a bytewide FRAM memory. The memory array is logically organized as 32,768 x 8 and is accessed using an industry standard parallel interface. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is the same as SRAM type devices, except the FM18L08 requires a falling edge of /CE to start each memory cycle.

Memory Operation

Users access 32,768 memory locations each with 8 data bits through a parallel interface. The cycle time is the same for read and write memory operations. This simplifies memory controller logic and timing circuits. Likewise the access time is the same for read and write memory operations. When /CE is deasserted high, a precharge operation begins, and is required of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

Note that the FM18L08 contains a limited low voltage write protection circuit. This will prevent access when V_{DD} is much lower than the specified operating range. It is still the user's responsibility to ensure that V_{DD} is within data sheet tolerances to prevent incorrect operation.

The FM18L08 is designed to operate in a manner similar to other bytewide memory products. For users familiar with SRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write performance of FRAM technology including NoDelay writes and from unlimited write endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally regardless of the state of /CE. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM18L08 drives the data bus when /OE is asserted to a low state. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will be driven when valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven onto the bus. When /OE is inactive the data bus will remain tri-stated.

Write Operation

Writes operations require the same time as reads. The FM18L08 supports both /CE- and /WE-controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE-controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the device begins the memory cycle as a write. The FM18L08 will not drive the data bus regardless of the state of /OE.

In a /WE-controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE- and /WE-controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Precharge Operation

The precharge operation is an internal condition where the state of the memory is prepared for a new access. All memory cycles consist of a memory access and a precharge. The precharge is user initiated by taking the /CE signal high or inactive. It

must remain high for at least the minimum precharge timing specification.

The user dictates the beginning of this operation since a precharge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

FRAM Design Considerations

When designing with FRAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide FRAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of /CE, users cannot ground it as they might with SRAM.

Users who are modifying existing designs to use FRAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a low transition of /CE. In many cases, this is the only change required. An example of the signal relationships is shown in Figure 2 below. Also shown is a common SRAM signal relationship that will not work for the FM18L08.

The reason for /CE to strobe for each address is two-fold: it latches the new address and creates the necessary precharge period while /CE is high.

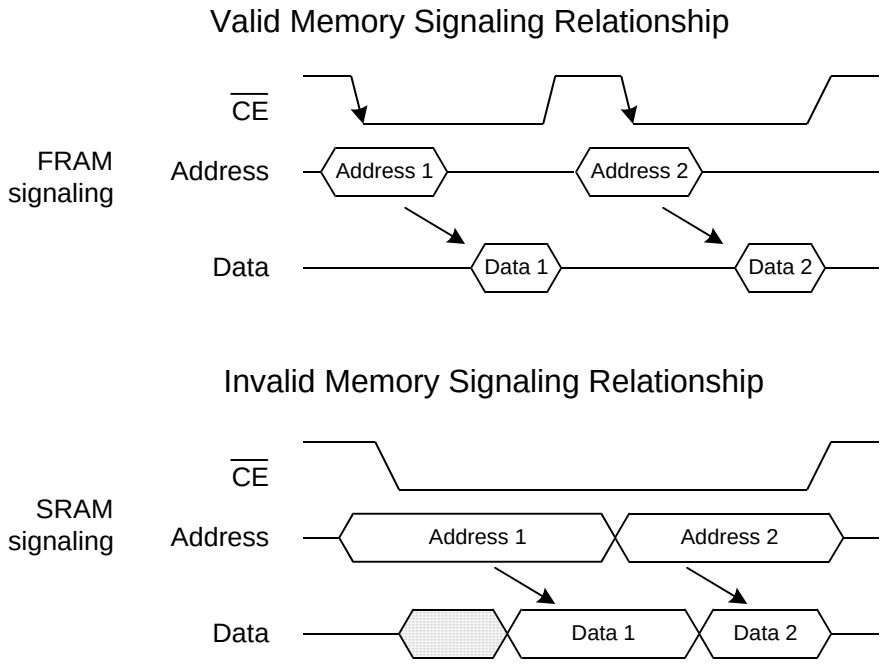


Figure 2. Memory Address Relationships

A second design consideration relates to the level of V_{DD} during operation. Battery-backed SRAMs are forced to monitor V_{DD} in order to switch to battery backup. They typically block user access below a certain V_{DD} level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the memory in a power down situation without warning.

FRAM memories do not need this system overhead. The memory will not block access at any V_{DD} level. The user, however, should prevent the processor from accessing memory when V_{DD} is out-of-tolerance. The common design practice of holding a processor in reset during powerdown may be sufficient. It is recommended that Chip Enable is pulled high and allowed to track V_{DD} during powerup and powerdown cycles. It is the user's responsibility to ensure that chip enable is high to prevent accesses below V_{DD} min. (3.0V). Figure 3 shows an external pullup resistor on /CE which will keep the pin high during power cycles assuming the MCU/MPU pin tri-states during the reset condition. The pullup resistor value should be chosen to ensure the /CE pin tracks V_{DD} yet a high enough value that the current drawn when /CE is low is not an issue.

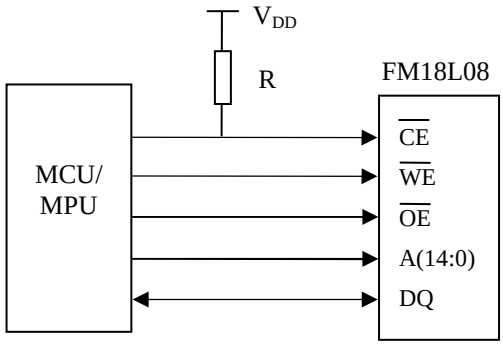


Figure 3. Use of Pullup Resistor on /CE

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +5.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +5.0V and V_{IN} < V_{DD}+1V
T_{STG}	Storage temperature	-55°C to +125°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Machine Model (JEDEC Std JESD22-A115-A)	 4kV 400V
	Package Moisture Sensitivity Level	MSL-1 (SOIC/DIP) MSL-2 (TSOP)

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 3.0V to 3.65V)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply	3.0		3.65	V	
I_{DD}	V_{DD} Supply Current – Active	-	7	15	mA	1
I_{SB1}	Standby Current – TTL			400	µA	2
I_{SB2}	Standby Current – CMOS		7	15	µA	3
I_{LI}	Input Leakage Current	-		10	µA	4
I_{LO}	Output Leakage Current	-		10	µA	4
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{OH}	Output High Voltage (I_{OH} = -1.0 mA)	2.4		-	V	
V_{OL}	Output Low Voltage (I_{OL} = 3.2 mA)	-		0.4	V	

Notes

1. V_{DD} = 3.65V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
2. V_{DD} = 3.65V, /CE at V_{IH}, All other pins at TTL levels.
3. V_{DD} = 3.65V, /CE at V_{DD}, All other pins at CMOS levels.
4. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.

Read Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 3.0V to 3.65V)

Symbol	Parameter	Min	Max	Units	Notes
t_{CE}	Chip Enable Access Time (to data valid)		70	ns	
t_{CA}	Chip Enable Active Time	70	2,000	ns	
t_{RC}	Read Cycle Time	140		ns	
t_{PC}	Precharge Time	70		ns	
t_{AS}	Address Setup Time	0		ns	
t_{AH}	Address Hold Time	15		ns	
t_{OE}	Output Enable Access Time		10	ns	
t_{HZ}	Chip Enable to Output High-Z		15	ns	1
t_{OHZ}	Output Enable to Output High-Z		15	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 3.0V to 3.65V)

Symbol	Parameter	Min	Max	Units	Notes
t_{CA}	Chip Enable Active Time	70	2,000	ns	
t_{CW}	Chip Enable to Write High	70		ns	
t_{WC}	Write Cycle Time	140		ns	
t_{PC}	Precharge Time	70		ns	
t_{AS}	Address Setup Time	0		ns	
t_{AH}	Address Hold Time	15		ns	
t_{WP}	Write Enable Pulse Width	40		ns	
t_{DS}	Data Setup	40		ns	
t_{DH}	Data Hold	0		ns	
t_{WZ}	Write Enable Low to Output High Z		15	ns	1
t_{WX}	Write Enable High to Output Driven	10		ns	1
t_{HZ}	Chip Enable to Output High-Z		15	ns	1
t_{WS}	Write Setup	0		ns	2
t_{WH}	Write Hold	0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Data Retention (V_{DD} = 3.0V to 3.65V)

Parameter	Min	Units	Notes
Data Retention	45	Years	1

Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 3.0V to 3.65V)

Symbol	Parameter	Min	Units	Notes
t_{PU}	V_{DD} (min.) to First Access Start	1	µS	
t_{PD}	Last Access Complete to V_{DD} (min.)	0	µS	

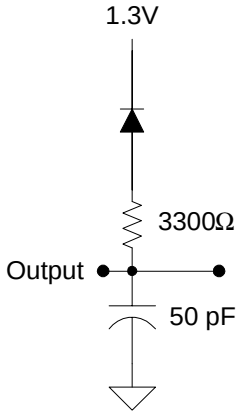
Capacitance (T_A = 25° C , f=1 MHz, V_{DD} = 3.3V)

Symbol	Parameter	Max	Units	Notes
$C_{I/O}$	Input/Output Capacitance (DQ)	8	pF	
C_{IN}	Input Capacitance	6	pF	

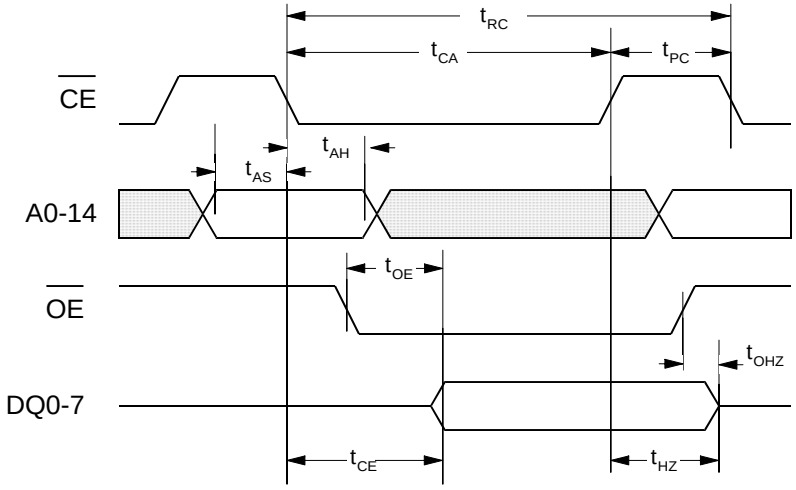
AC Test Conditions

Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input rise and fall times	5 ns
Input and output timing levels	1.5V

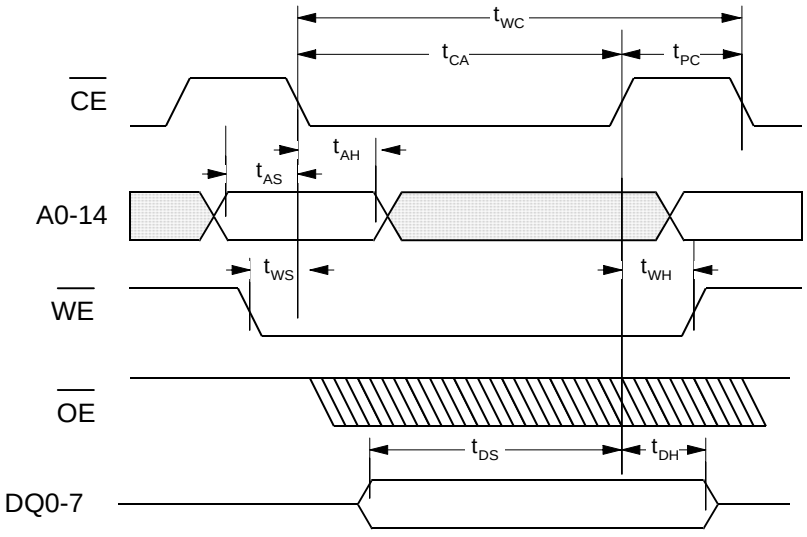
Equivalent AC Load Circuit



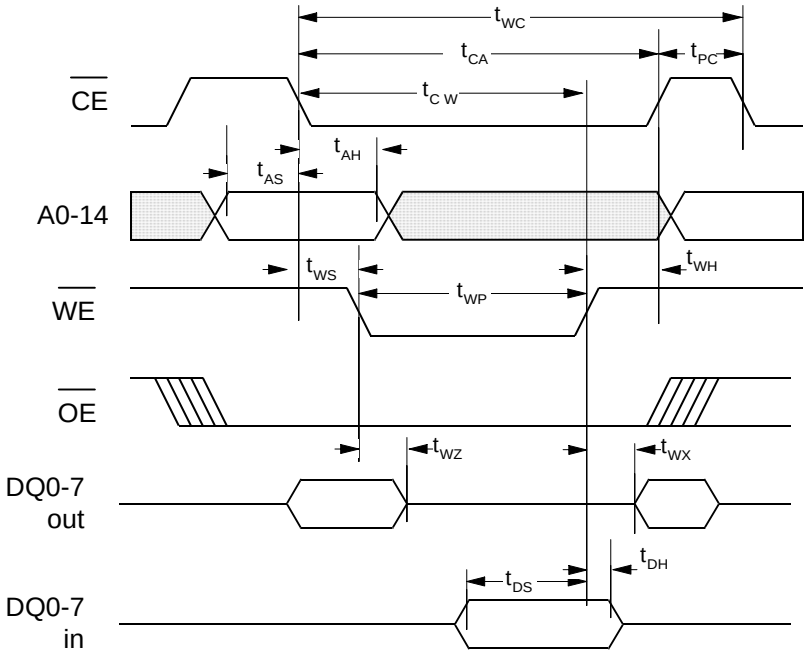
Read Cycle Timing



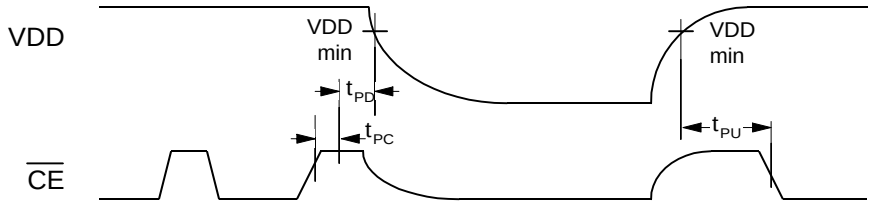
Write Cycle Timing - /CE Controlled Timing



Write Cycle Timing - /WE Controlled Timing

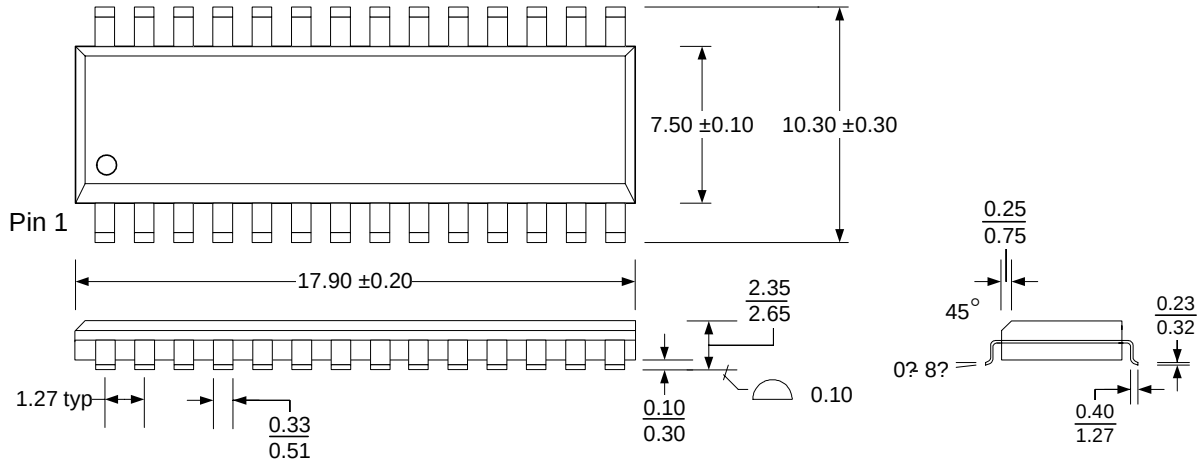


Power Cycle Timing

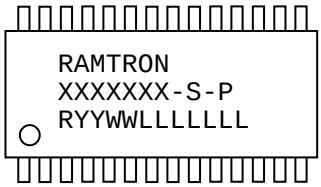


Mechanical Drawing

28-pin SOIC (JEDEC MS-013D Variation AE)
All dimensions in millimeters



SOIC Package Marking Scheme

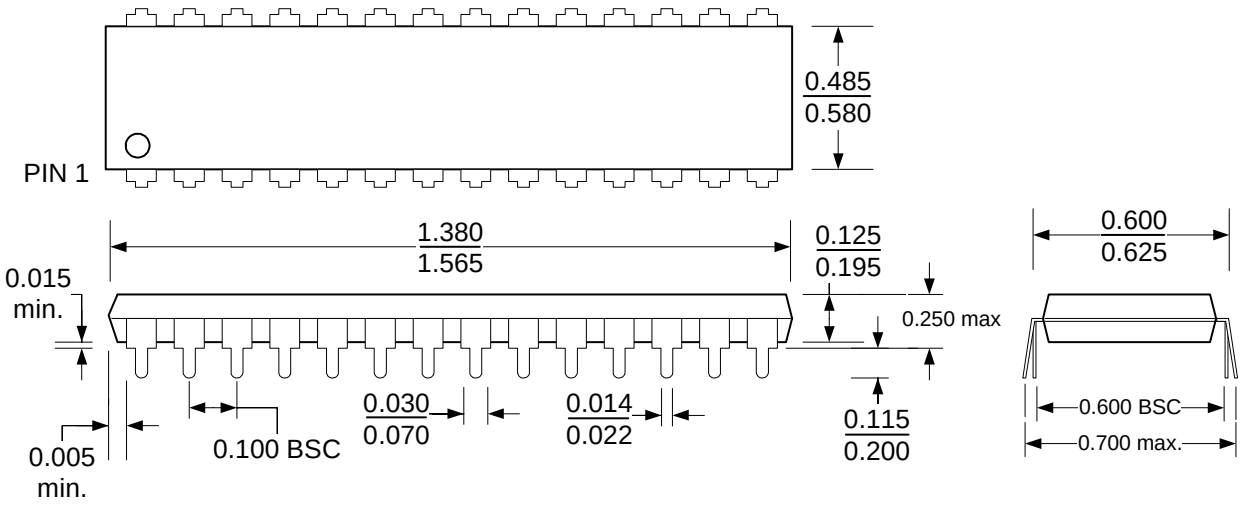


Legend:
XXXX= part number, S=speed (-70), P= package type (-SG)
R=rev code, YY=year, WW=work week, LLLLLL= lot code

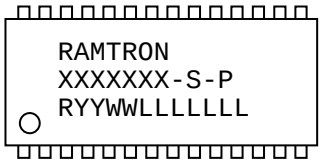
Example: FM18L08, 70ns speed, "Green" SOIC package,
B rev., Year 2006, Work Week 30, Lot code 50013G

RAMTRON
FM18L08-70-SG
B063050013G

28-pin 600-mil DIP (JEDEC MS-011)
All dimensions in inches



DIP Package Marking Scheme

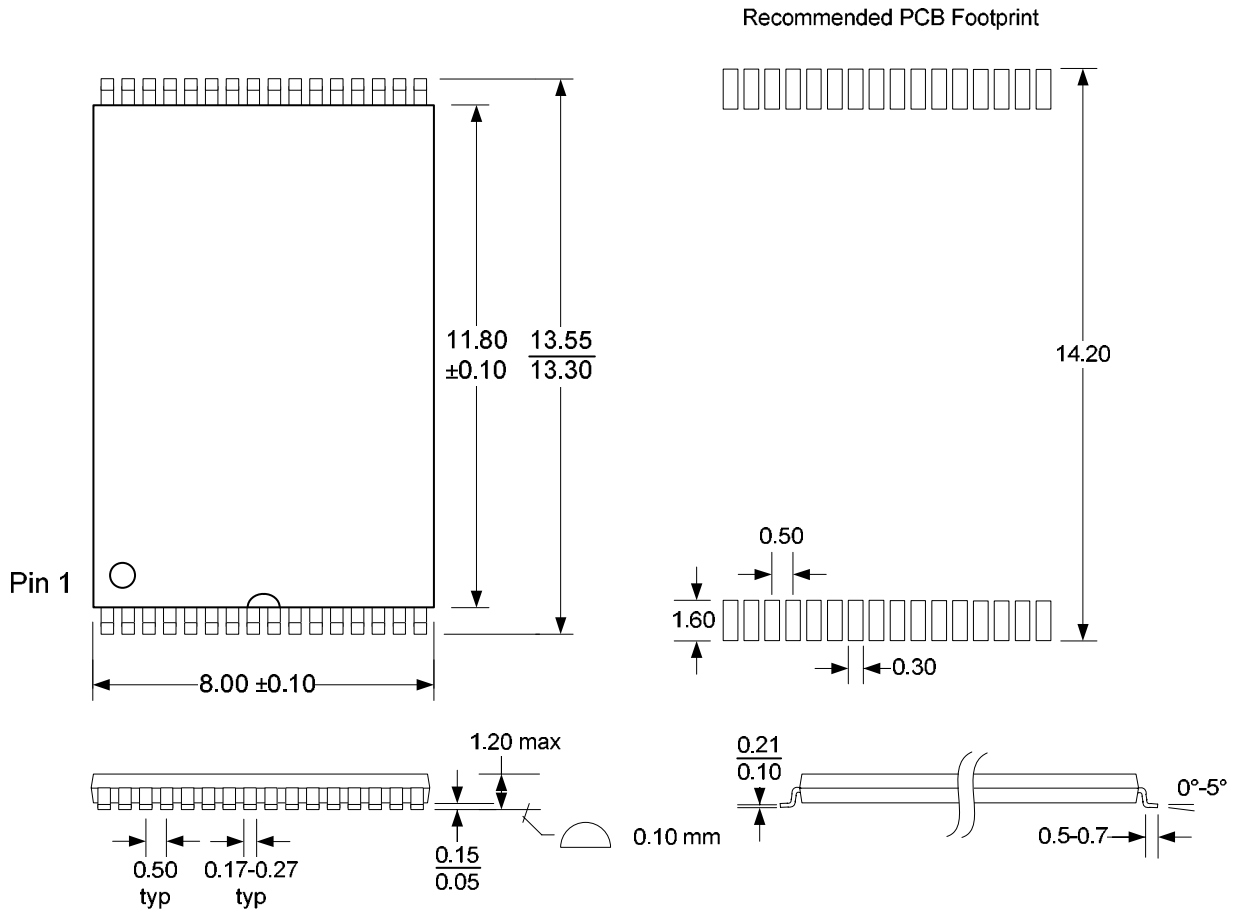


Legend:
XXXX= part number, S=speed (-70), P= package type (-PG)
R=rev code, YY=year, WW=work week, LLLLLL= lot code

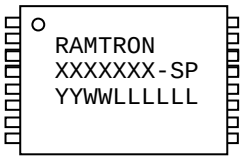
Example: FM18L08, 70ns speed, "Green" DIP package,
B rev., Year 2006, Work Week 30, Lot code 50013G

RAMTRON
FM18L08-70-PG
B063050013G

32-pin Shrunk TSOP-I (8.0 x 13.4 mm)
All dimensions in millimeters



TSOP Package Marking Scheme



Legend:
XXXXXX= part number, SP= speed/package (-70TG)
R=rev code, YY=year, WW=work week, LLLLLL= lot code

Example: FM18L08-70-TG, "green" TSOP package,
B rev., Year 2006, Work Week 51, Lot 60012T2
RAMTRON
FM18L08-70TG
B065160012T2

Revision History

Revision	Date	Summary
0.1	3/23/01	Initial Release
0.2	9/28/01	Changed Data Retention table. Modified temperature range to commercial.
0.3	3/18/02	Changed temperature range to industrial and Vdd range to 3V – 3.65V. Changed precharge time to 70ns. Added note for 2.7V operation. Updated package drawings.
1.0	6/15/02	Updated to Preliminary status, changed storage temperature.
2.0	12/10/02	Updated to Production status, removed ref to 2.7V operation.
2.1	5/1/03	Changed tCA (max) value. Reworded notes 2 and 3 in DC Operating Conditions table.
2.2	7/14/04	Added “green” packaging options.
3.0	6/12/06	Added ESD and package MSL ratings. Updated rev numbering and footer. Added recommendation on CE pin during power cycles.
3.1	11/27/06	Added TSOP packaging option.
3.2	2/20/07	Updated TSOP MSL rating.
3.3	5/15/07	Redraw package outlines, added marking scheme to SOIC/DIP.
3.4	7/30/07	Extended data retention to 45 years based on recent test results.