



March 2008
QFET[®]

FQD3N50C / FQU3N50C 500V N-Channel MOSFET

Features

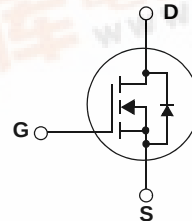
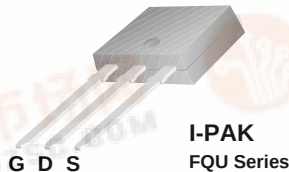
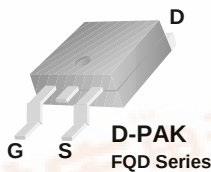
- 2.5A, 500V, $R_{DS(on)} = 2.5\Omega$ @ $V_{GS} = 10\text{ V}$
- Low gate charge (typical 10 nC)
- Low C_{rss} (typical 8.5pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQD3N50C/FQU3N50C	Units
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	2.5	A
	- Continuous ($T_C = 100^\circ\text{C}$)	1.5	A
I_{DM}	Drain Current - Pulsed (Note 1)	10	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	200	mJ
I_{AR}	Avalanche Current (Note 1)	2.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	3.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	35	W
	- Derate above 25°C	0.28	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	--	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)



Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD3N50C	FQD3N50CTM	D-PAK	380mm	16mm	2500
FQD3N50C	FQD3N50CTF	D-PAK	380mm	16mm	2500
FQU3N50C	FQU3N50CTU	I-PAK	-	-	70

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	500	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 400 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 1.25 A	--	2.1	2.5	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 1.25 A (Note 4)	--	1.5	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	280	365	pF
C _{oss}	Output Capacitance		--	50	65	pF
C _{rss}	Reverse Transfer Capacitance		--	8.5	11	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 2.5A, R _G = 25 Ω (Note 4, 5)	--	10	30	ns
t _r	Turn-On Rise Time		--	25	60	ns
t _{d(off)}	Turn-Off Delay Time		--	35	80	ns
t _f	Turn-Off Fall Time		--	25	60	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 2.5A, V _{GS} = 10 V (Note 4, 5)	--	10	13	nC
Q _{gs}	Gate-Source Charge		--	1.5	--	nC
Q _{gd}	Gate-Drain Charge		--	5.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	10	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.5 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 3 A, dl _F / dt = 100 A/μs (Note 4)	--	170	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.7	--	μC

NOTES:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 58mH, I_{AS} = 2.5A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

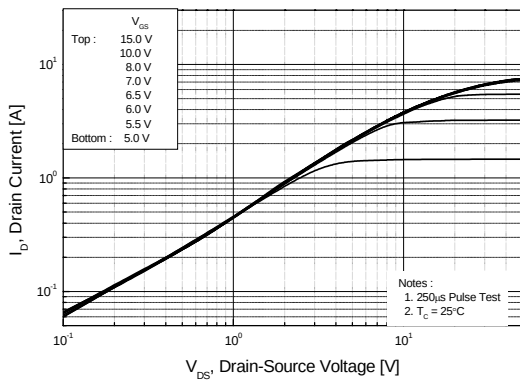


Figure 2. Transfer Characteristics

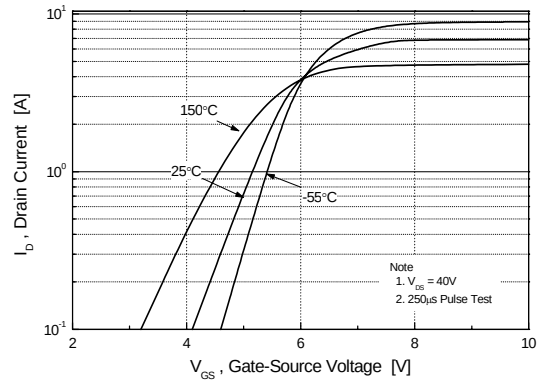


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

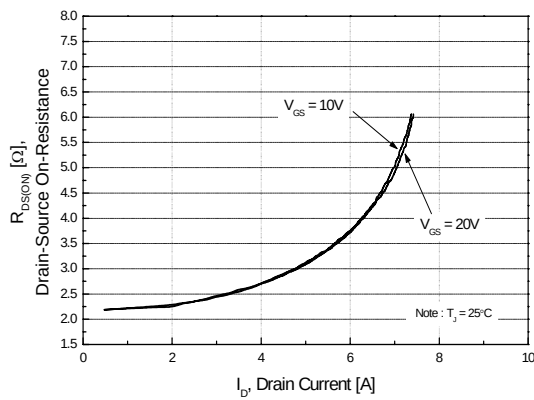


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

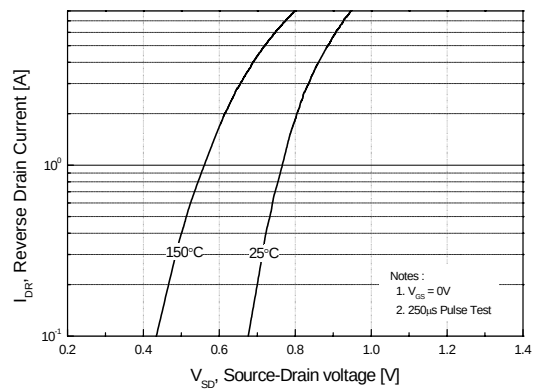


Figure 5. Capacitance Characteristics

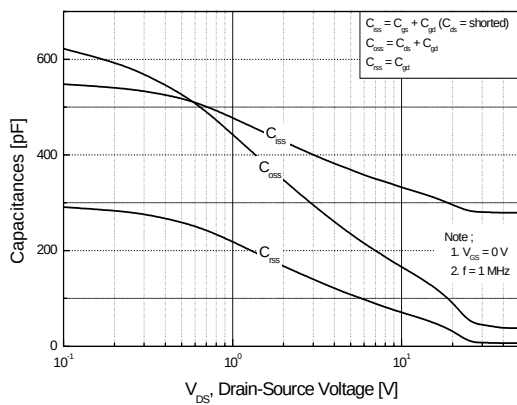
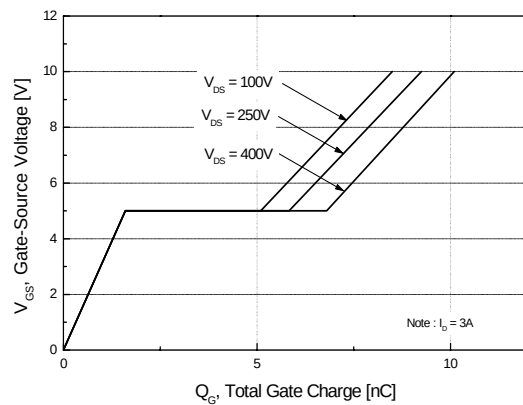


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

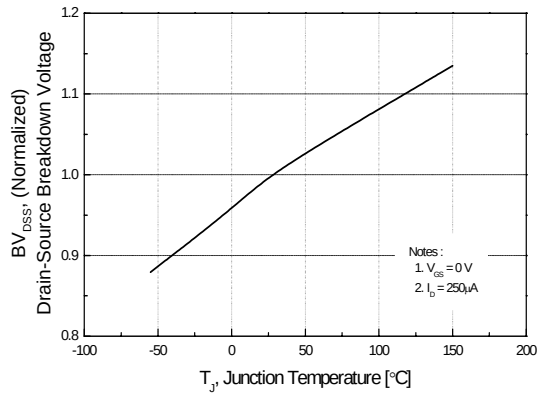


Figure 8. On-Resistance Variation vs. Temperature

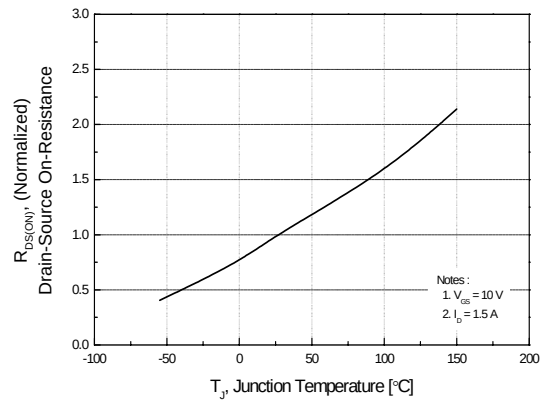


Figure 9. Maximum Safe Operating Area

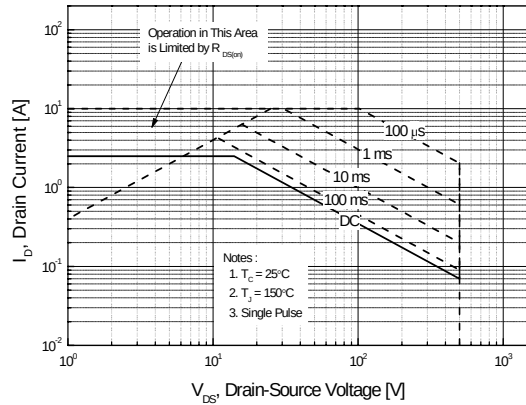


Figure 10. Maximum Drain Current vs. Case Temperature

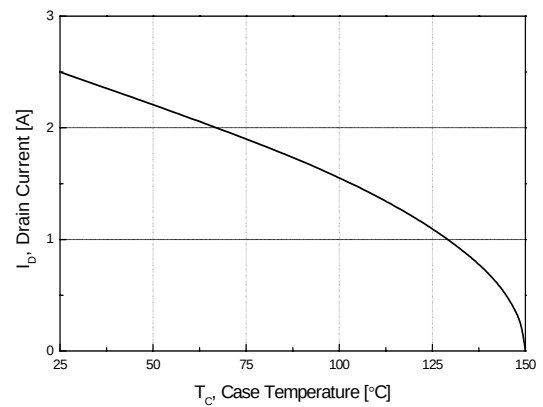
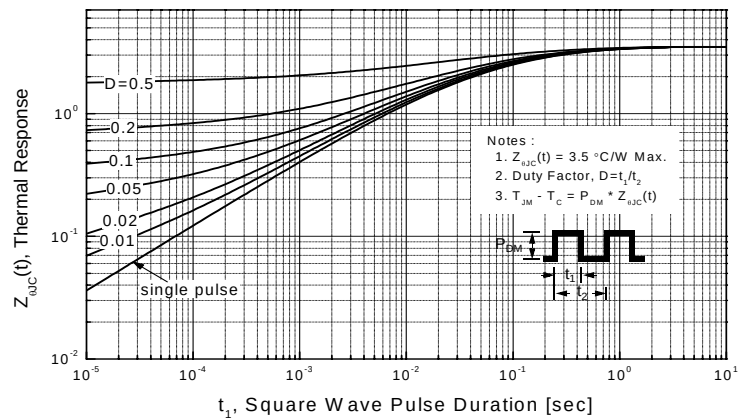
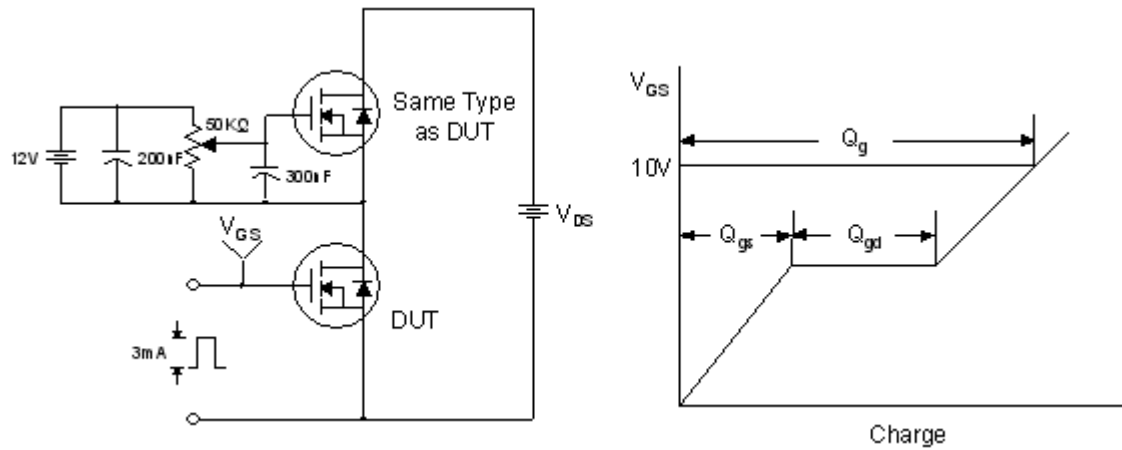


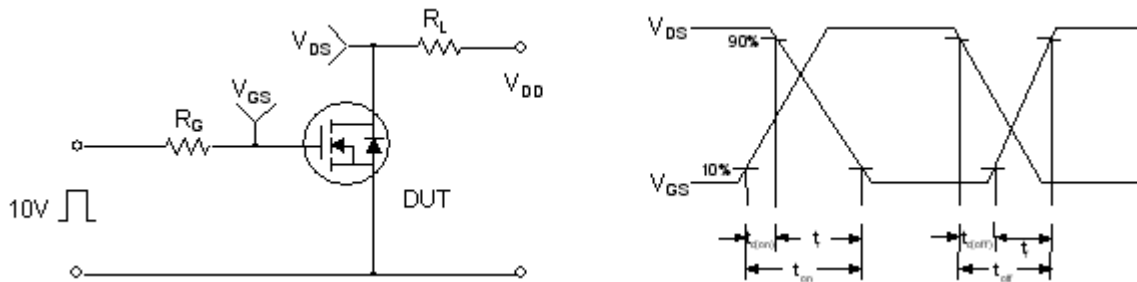
Figure 11. Transient Thermal Response Curve



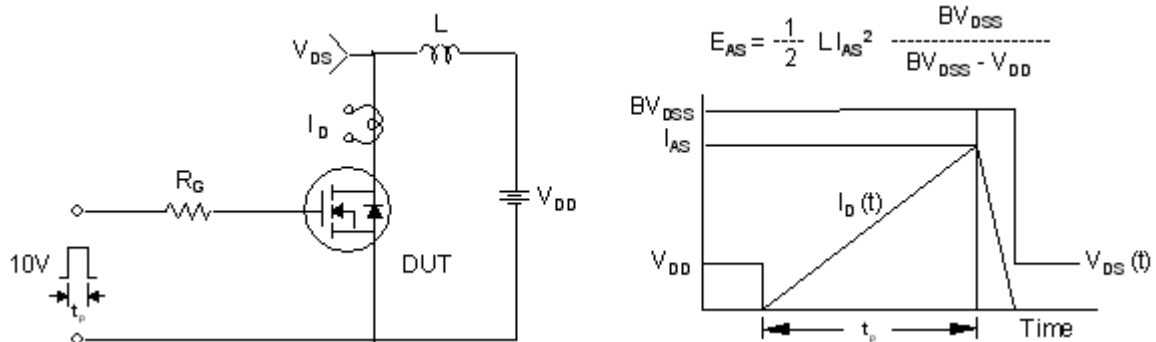
Gate Charge Test Circuit & Waveform



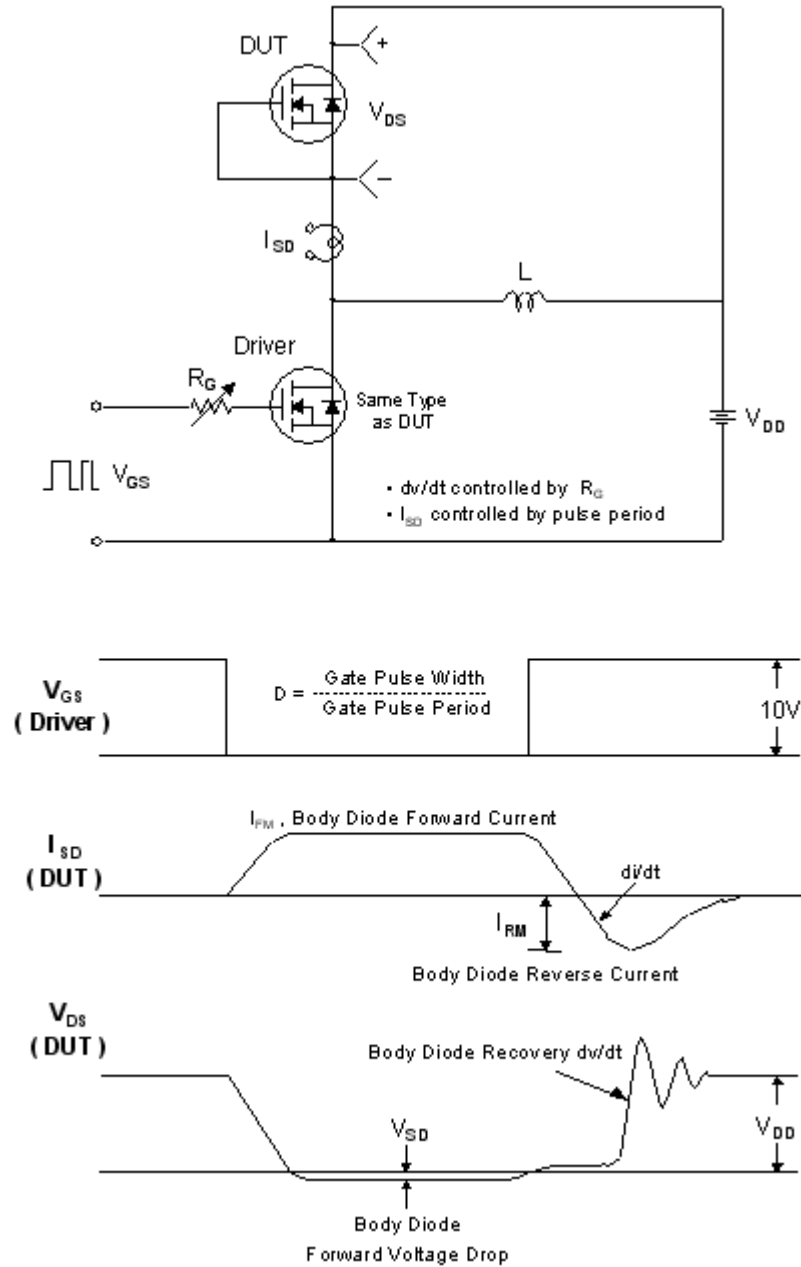
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

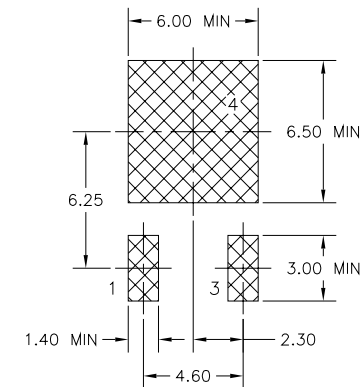
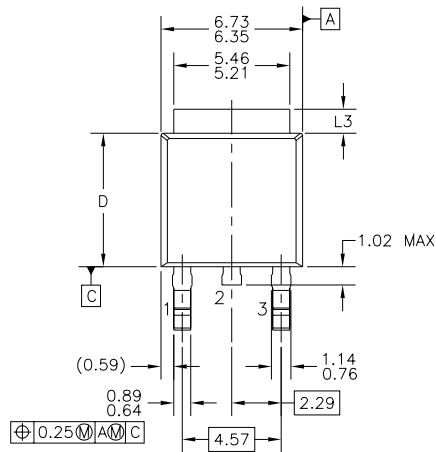


Peak Diode Recovery dv/dt Test Circuit & Waveforms

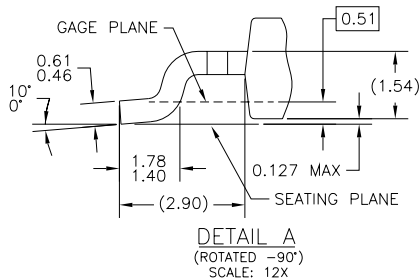
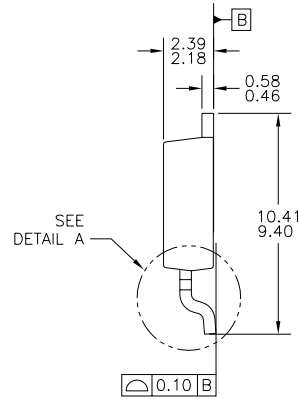
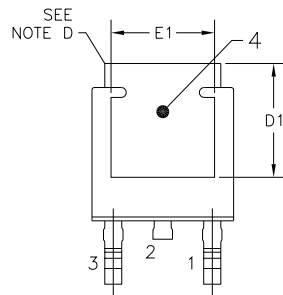


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3, D, E1 & D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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