FAIRCHILD SEMICONDUCTOR®

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FSA2467
0.4Ω Low-Voltage Dual DPDT Analog Switch

Features

- Typical 0.4Ω On Resistance (R_{ON}) for +2.7V supply
- Features Less then12µA I_{CCT} Current when Sn Input is Lower than V_{CC}
- 0.25Ω Maximum R_{ON} Flatness for +2.7V Supply
- 3x3mm 16-Lead Pb-Free MLP Package
- 1.8x2.6mm 16-Lead Pb-Free UMLP Package
- Broad V_{CC} Operating Range
- Low THD (0.02% Typical for 32Ω Load)

Applications

- Cell Phone
- PDA
- Portable Media Player

Description

The FSA2467 is a dual Double-Pole, Double-Throw (DPDT) analog switch. The FSA2467 operates from a single 1.65V to 4.3V supply. The FSA2467 features an ultra-low on resistance of 0.4Ω at a +2.7V supply and 25°C. This device is fabricated with sub-micron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation.

FSA2467 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature allows mobile handset applications direct interface with baseband processor general-purpose I/Os.

Ordering Information

Part Number	Package Description
FSA2467MPX	16-lead Molded Leadless Package (MLP), JEDEC MO-220, 3x3mm Square
FSA2467UMX	16-lead Ultrathin Molded Leadless Package (UMLP), 1.8x2.6mm

All packages are lead free per JEDEC: J-STD-020B standard.

Application Diagram

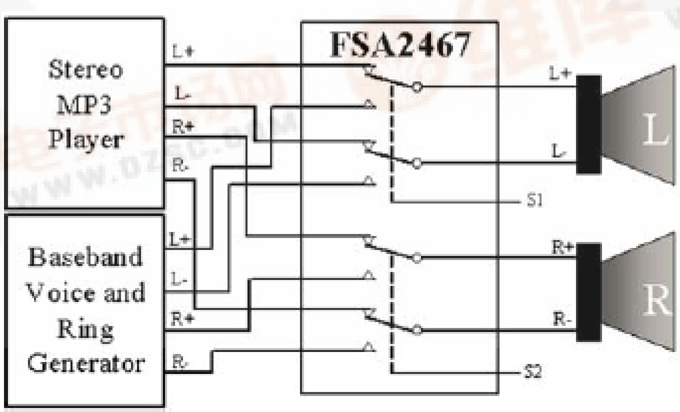


Figure 1. Application Diagram

Pin Assignments

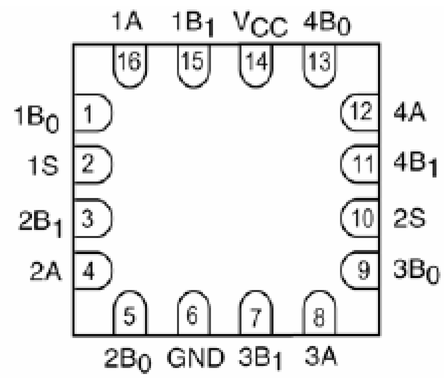


Figure 2. Pin Assignments

Truth Table

Control Inputs	Function
LOW	nB_0 Connected to nA
HIGH	nB_1 Connected to nA

Pin Descriptions

Name	Function
nA, nB_0, nB_1	Data Ports
nS	Control Input

Analog Symbol

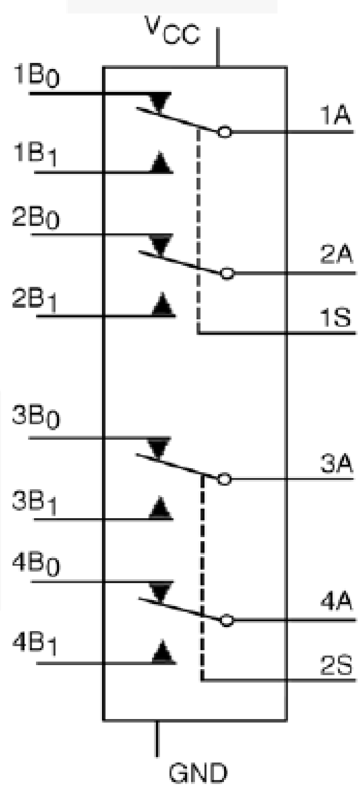


Figure 3. Analog Symbol

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	4.6	V
V_S	Switch Voltage	-0.5	V_{CC}+0.3	V
V_{IN}	Input Voltage	-0.5	4.6	V
I_{IK}	Input Diode Current	-50		mA
I_{SW}	Switch Current		350	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms duration, <10% Duty Cycle)		500	mA
T_{STG}	Storage Temperature Range	-65	+150	ºC
T_J	Junction Temperature		+150	ºC
T_L	Lead Temperature, Soldering 10 Seconds		+260	ºC
ESD	Human Body Model		5.5	kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.65	4.30	V
V_{IN}	Control Input Voltage[1]	0	V_{CC}	V
V_{IN}	Switch Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	ºC

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25ºC			T_A = -40 to +85ºC		Units
				Min.	Typ.	Max.	Min	Max.	
V_{IH}	Input Voltage High		4.3				1.4		V
			2.7 to 3.6				1.3		
			2.3 to 2.7				1.1		
			1.65 to 1.95				0.9		
V_{IL}	Input Voltage Low		4.3					0.7	V
			2.7 to 3.6					0.5	
			2.3 to 2.7					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage	V_{IN}=0V to V_{CC}	1.65 to 4.30				-0.5	0.5	µA
$I_{NO(OFF)}$ $I_{NC(OFF)}$	Off Leakage Current of Port nB_0 and nB_1	nA=0.3V, V_{CC}-0.3V	1.95 to 4.30	-10.0		10.0	-50.0	50.0	nA
		nB_0 or nB_1=0.3V, V_{CC}-0.3V or floating							
$I_{A(ON)}$	On Leakage Current of Port A	nA=0.3V,V_{CC}-0.3V	1.95 to 4.30	-10.0		10.0	-50.0	50.0	nA
		nB_0 or nB_1=0.3V, V_{CC}-0.3V or floating							
R_{ON}	Switch On Resistance(2)	I_{OUT}=100mA	4.3		0.4			0.6	Ω
		nB_0 or nB_1=0V,0.8V, 1.8V,2.7V	2.7		0.4			0.6	
		I_{OUT}=100mA, nB_0 or $_1$=0V,0.7V, 1.2V, 2.3V	2.3	0.55				0.95	
		I_{OUT}=100mA, nB_0 or nB_1=1.0V	1.8	0.8				2.0	
ΔR_{ON}	On Resistance Matching Between Channels(3)	I_{OUT}=100mA, nB_0 or nB_1=0.8V	2.7	0.04				0.10	Ω
		I_{OUT}=100mA, nB_0 or nB_1=0.7V	2.3	0.03				0.10	
$R_{FLAT(ON)}$	On Resistance Flatness(4)	I_{OUT}=100mA, B_0 or nB_1=0V to V_{CC}	2.7					0.25	Ω
			2.3					0.3	
I_{CC}	Quiescent Supply Current	V_{IN}=0V to V_{CC} I_{OUT}=0V	4.3	-100		100	-500	500	nA
I_{CCT}	Increase in I_{CC} Current per Control Voltage	V_{IN}=1.8V	4.3		7.0	12.0		15.0	µA
		V_{IN}=2.6V	4.3		3.0	6.0		7.0	

Notes:
2. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
3. $\Delta R_{ON}=R_{ON\ max} - R_{ON\ min}$ measured at identical Vcc, temperature and voltage.
4. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

Typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}	T_A = +25ºC			T_A = -40 to +85ºC		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	nB0 or nB1=1.5V	3.6 to 4.3			50		60	ns	Figure 7
		R_L=50Ω, C_L=35pF	2.7 to 3.6			65		75		
			2.3 to 2.7			80		90		
t_{OFF}	Turn-Off Time	nB0 or nB1=1.5V	3.6 to 4.3			32		40	ns	Figure 7
		R_L=50Ω, C_L=35pF	2.7 to 3.6			42		50		
			2.3 to 2.7			52		60		
t_{BBM}	Break-Before-Make Time	nB0 or nB1=1.5V	3.6 to 4.3		12				ns	Figure 8
		R_L=50Ω, C_L=35pF	2.7 to 3.6		15					
			2.3 to 2.7		20					
Q	Charge Injection	C_L=100pF, V_{GEN}=0V, R_{GEN}=0Ω	3.6 to 4.3		15				pC	Figure 10
		C_L=100pF, V_{GEN}=0V, R_{GEN}=0Ω	2.7 to 3.6		10					
		C_L=100pF, V_{GEN}=0V, R_{GEN}=0Ω	2.3 to 2.7		8					
OIRR	Off Isolation	f=100KHz, R_L=50Ω,C_L=5pF	3.6 to 4.3		-75				dB	Figure 9
			2.7 to 3.6		-75					
			2.3 to 2.7		-75					
Xtalk	Crosstalk	f=100KHz, R_L=50Ω, C_L=5pF	3.6 to 4.3		-75				dB	Figure 9
			2.7 to 3.6		-75					
			2.3 to 2.7		-75					
BW	-3dB Bandwidth	R_L=50Ω	2.3 to 4.3		85				MHZ	Figure 12
THD	Total Harmonic Distortion	R_L=32Ω, V_{IN}=2V_{PP}, f=20 to 20kHZ	3.6 to 4.3		0.02				%	Figure 13
		R_L=32Ω, V_{IN}=2V_{PP}, f=20 to 20kHZ	2.7 to 3.6		0.02					
		R_L=32Ω, V_{IN}=2V_{PP}, f=20 to 20kHZ	2.3. to 2.7		0.02					

Capacitance

Symbol	Parameter	Conditions	V_{CC}	T_A = +25ºC Typical	Units	Figure
C_{IN}	Control Pin Input Capacitance	f=1MHZ	0	1.5	pF	Figure 7
C_{OFF}	B Port Off Capacitance	f=1MHZ	3.3	32	pF	Figure 7
C_{ON}	A Port On Capacitance	f=1MHZ	3.3	118	pF	Figure 7

Typical Applications

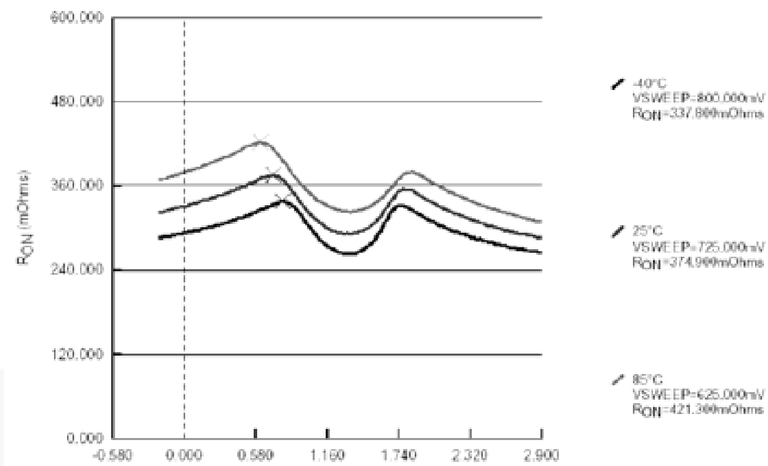


Figure 4. R_{ON} at 2.7V V_{CC}

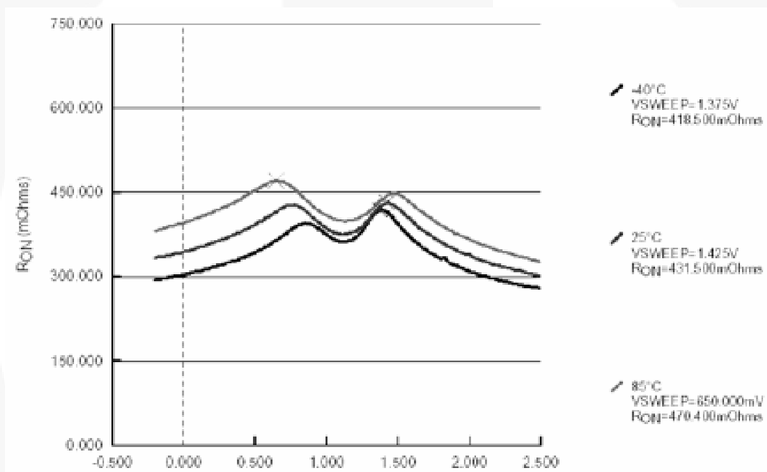


Figure 5. R_{ON} at 2.3V V_{CC}

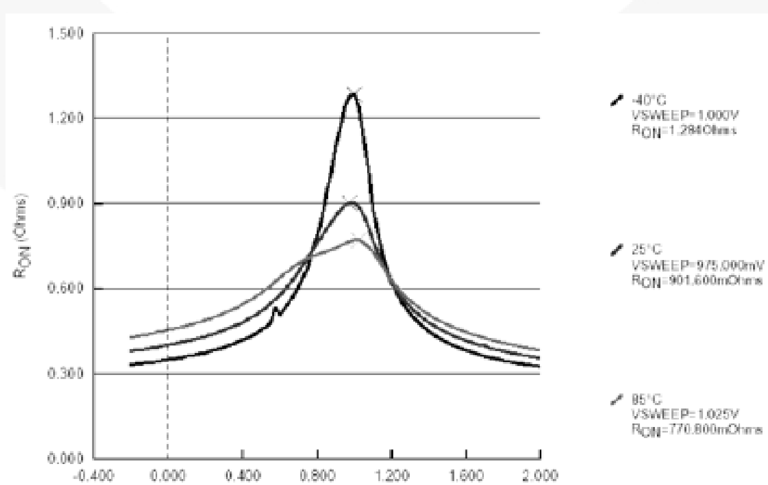


Figure 6. R_{ON} at 1.8V V_{CC}

AC Loadings and Waveforms

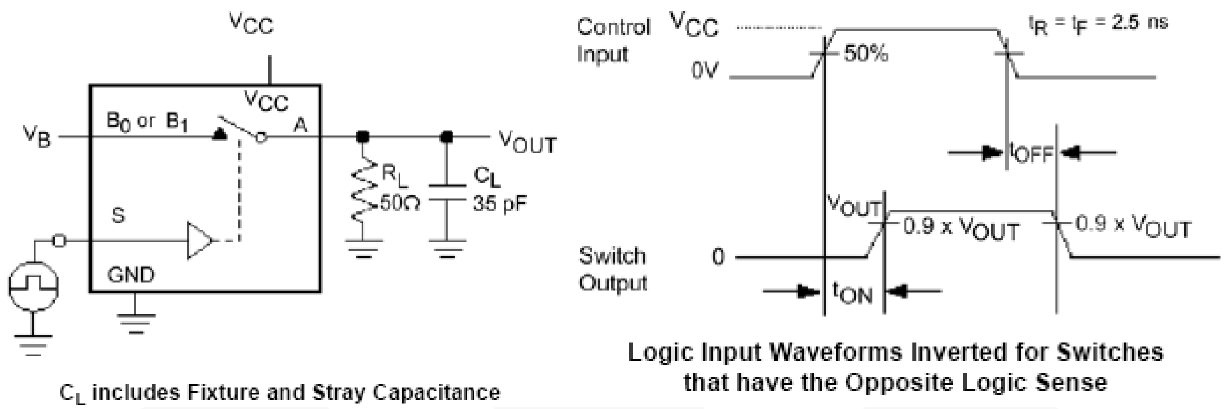


Figure 7. Turn-On / Turn-Off Timing

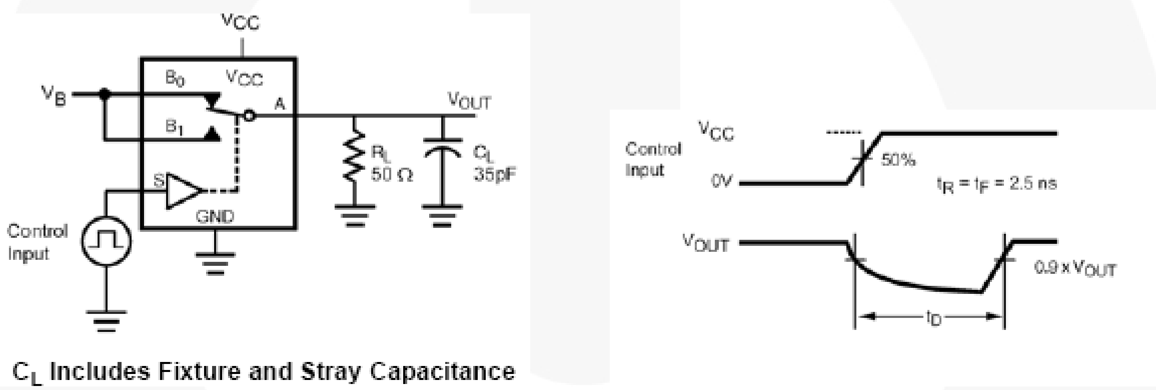


Figure 8. Break-Before-Make Timing

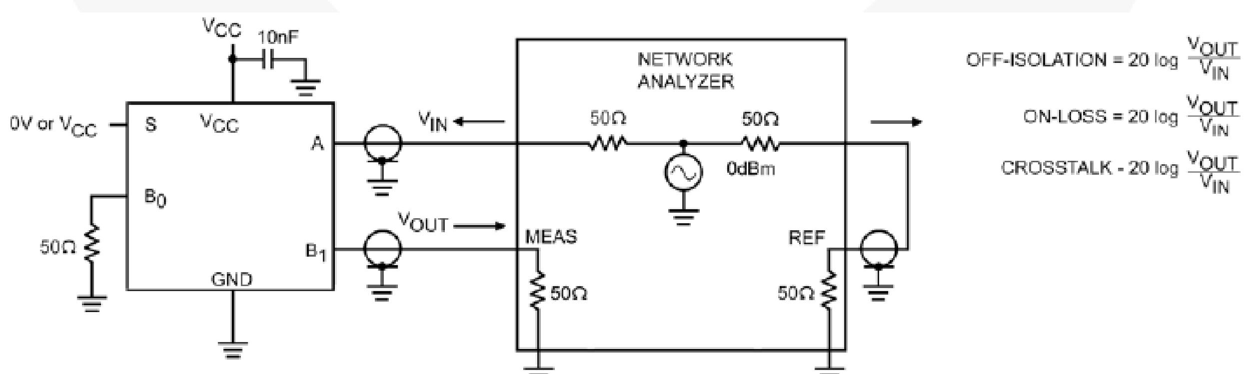


Figure 9. Off Isolation and Crosstalk

AC Loadings and Waveforms (Continued)

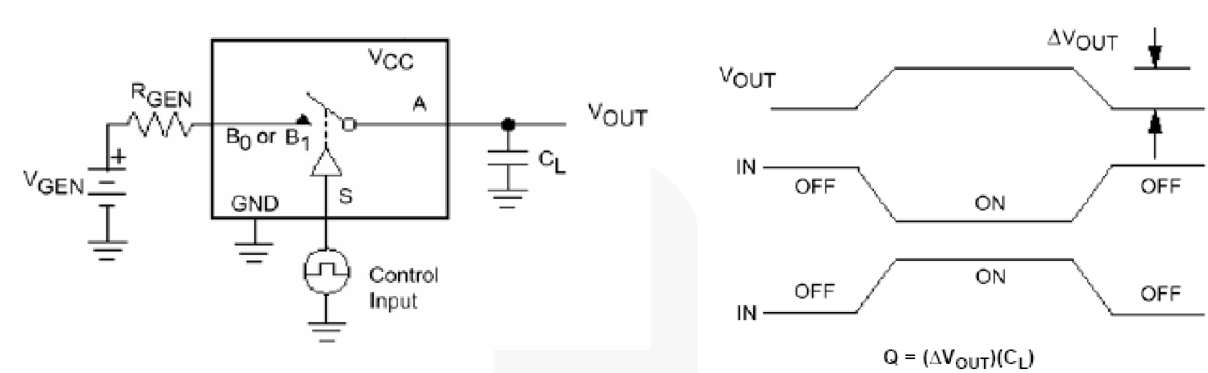


Figure 10. Charge Injection

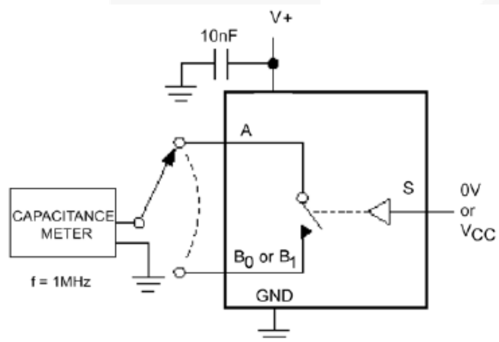


Figure 11. On / Off Capacitance Measurement Setup

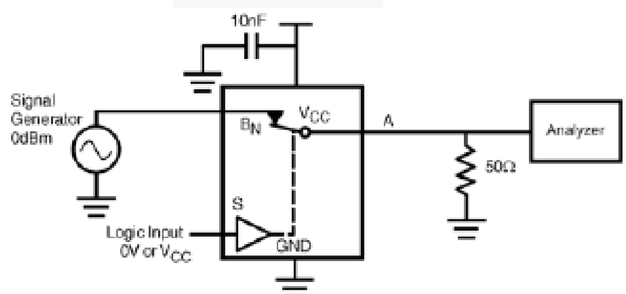


Figure 12. Bandwidth

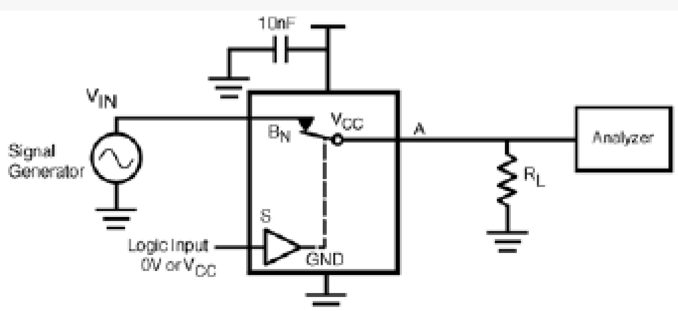
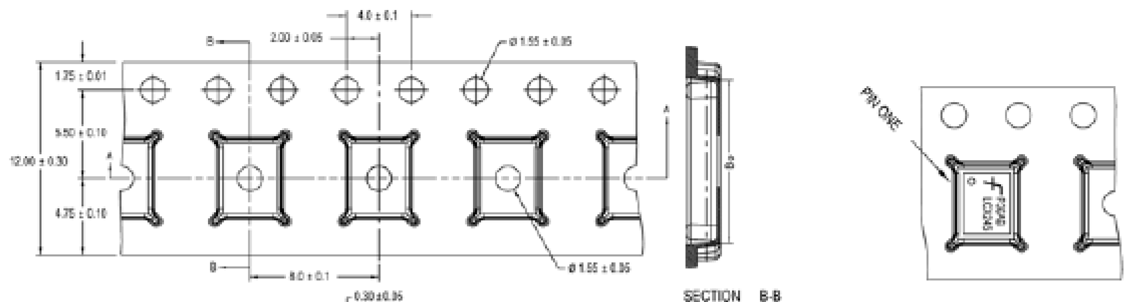


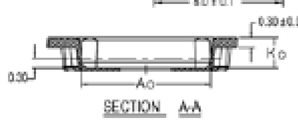
Figure 13. Harmonic Distortion

Tape and Reel Specifications

Tape Format for MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MPX	Leader (Start End)	125 (typical)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typical)	Empty	Sealed



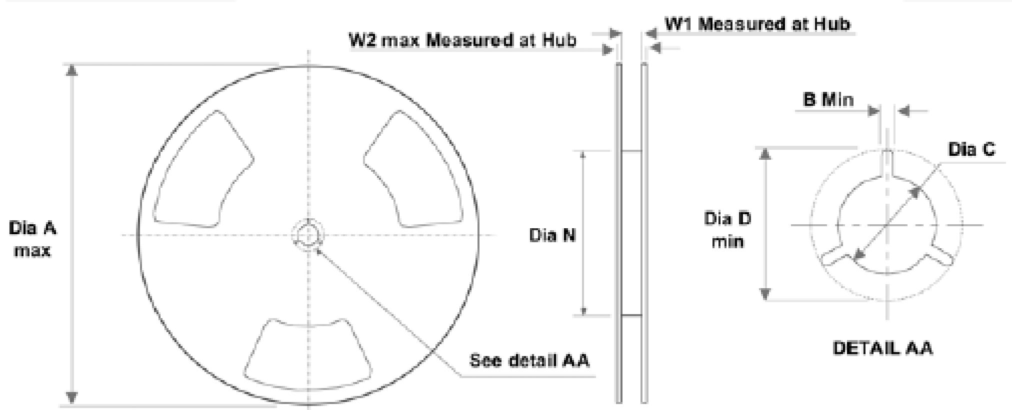


PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

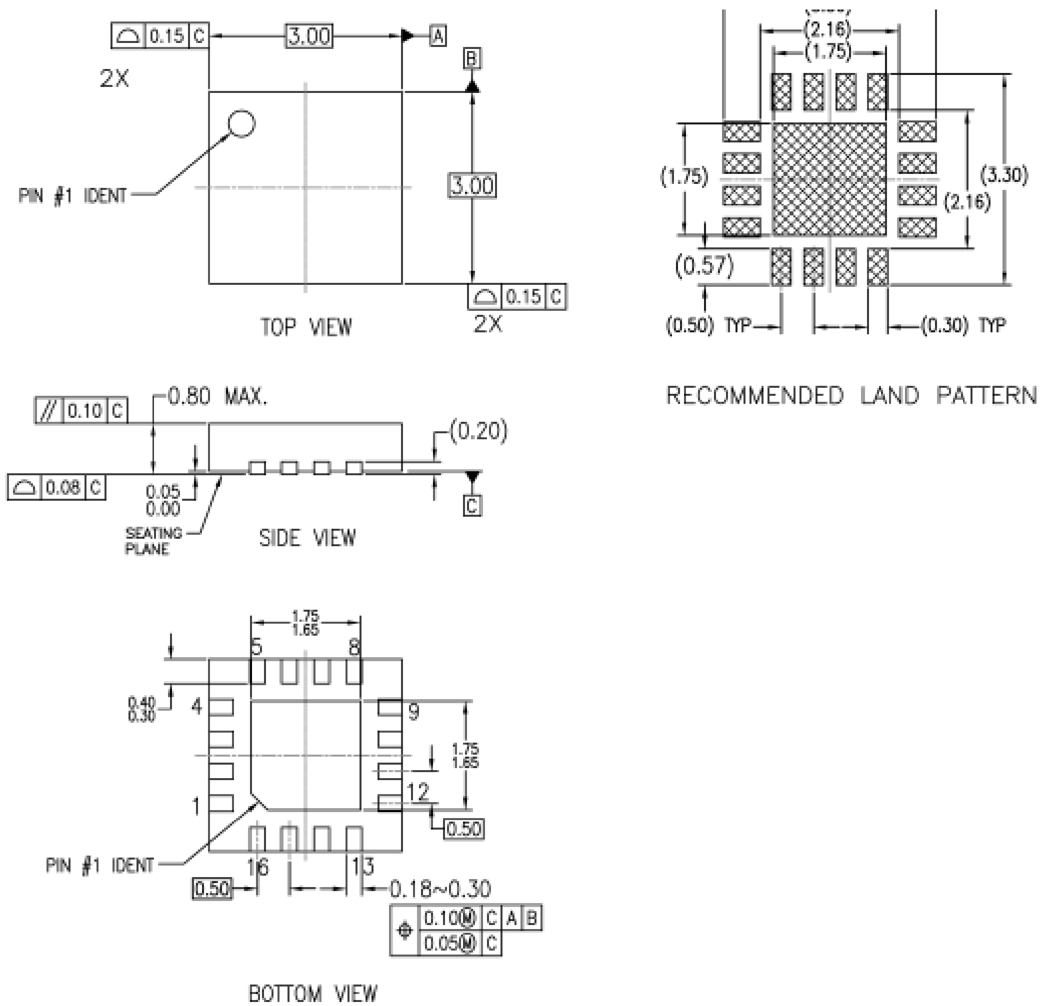
NOTES: unless otherwise specified

1. Cummulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Diemension in inches rounded.



Tape Size	A	B	C	D	N	W1	W2
	13.000	0.059	0.512	0.795	7.008	0.488	0.724
(12mm)	(330.00)	(1.50)	(13.00)	(20.20)	(178.00)	(12.40)	(18.40)

Package Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−220, VARIATION WEED−Pending, DATED pending

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MLP16BrevB

Figure 14. 16-Lead, Molded Leadless Package (MLP), JEDEC MO-220 3x3mm Square

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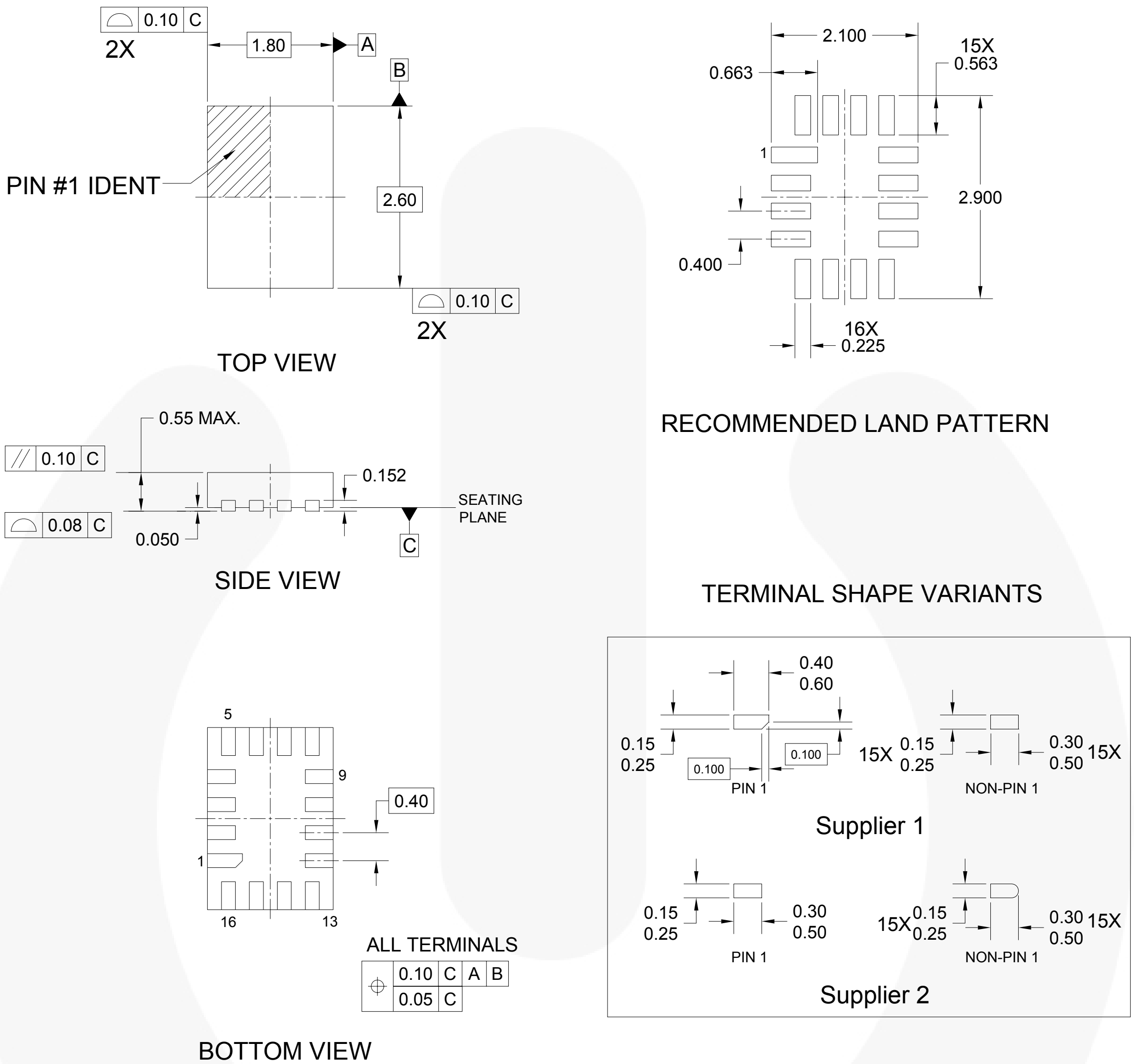
Package Dimensions



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C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
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E. LAND PATTERN IS A MINIMAL TOE DESIGN
F. DRAWING FILE NAME : UMLP16AREV3

Figure 15. 16-Lead, Ultrathin Molded Leadless Package (UMLP)

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