8Mbit (1Mx8)

3V Only Serial Flash Memory

■ FEATURES

- Single supply voltage 2.7~3.6V
- Speed
  - Read max frequency : 33MHz
  - Fast Read max frequency : 50MHz; 100MHz
- Low power consumption
  - typical active current
  - 15μA typical standby current
- Reliability
  - 100,000 typical program/erase cycles
  - 20 years Data Retention
- Program
  - Byte program time 7μs(typical)
- Erase
  - Chip erase time 8s(typical)
    block erase time 1sec (typical)
  - Sector erase time 60ms (typical),
- Auto Address Increment (AAI) WORD Programming
  - Decrease total chip programming time over Byte-Program operations
- SPI Serial Interface
  - SPI Compatible : Mode 0 and Mode3
- End of program or erase detection
- Write Protect ($\overline{\text{WP}}$)
- Hold Pin ($\overline{\text{HOLD}}$)
- Package available
  - 8-pin SOIC 200-mil

ORDERING INFORMATION

Part No.	Speed	Package		COMMENTS
F25L008A –50PAG	50MHz	8 lead SOIC	200mil	Pb-free
F25L008A –100PAG	100MHz	8 lead SOIC	200mil	Pb-free
F25L008A –50DG	50MHz	8 lead PDIP	300mil	Pb-free
F25L008A –100DG	100MHz	8 lead PDIP	300mil	Pb-free

GENERAL DESCRIPTION

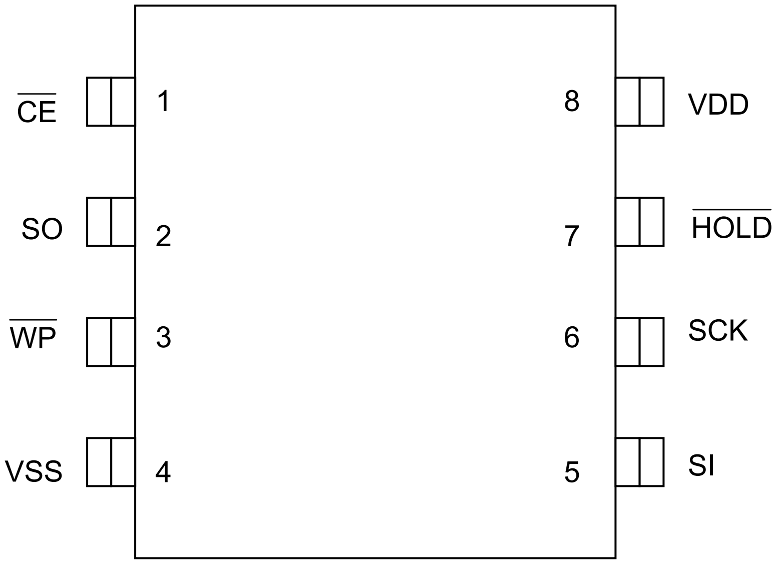
The F25L008A is a 8Megablt, 3V only CMOS Serial Flash memory device organized as 1M bytes of 8 bits. This device is packaged in 8-lead SOIC 200mil. ESMT's memory devices reliably store memory data even after 100,000 program and erase cycles.

The F25L008A features a sector erase architecture. The device memory array is divided into 256 uniform sectors with 4K byte each ; 16 uniform blocks with 64K byte each. Sectors can be erased individually without affecting the data in other sectors. Blocks can be erased individually without affecting the data in other blocks. Whole chip erase capabilities provide the flexibility to revise the data in the device.

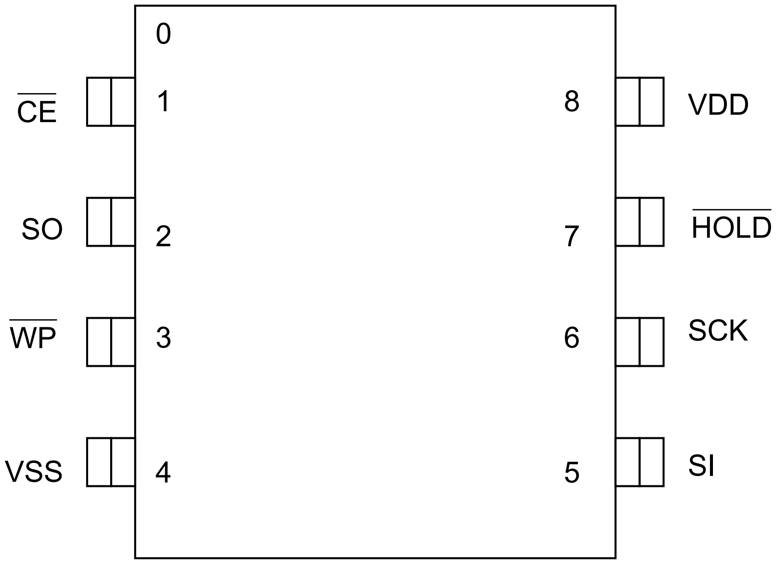
The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

PIN CONFIGURATIONS

8-PIN SOIC



8-PIN PDIP



PIN Description

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing for serial input and output operations
SI	Serial Data Input	To transfer commands, addresses or data serially into the device. Data is latched on the rising edge of SCK.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of SCK.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{WP}$	Write Protect	The Write Protect ($\overline{WP}$) pin is used to enable/disable BPL bit in the status register.
$\overline{HOLD}$	Hold	To temporality stop serial communication with SPI flash memory without resetting the device.
VDD	Power Supply	To provide power.
VSS	Ground	

SECTOR STRUCTURE

Table1 : F25L008A Sector Address Table

Block	Sector	Sector Size (Kbytes)	Address range	Block Address			
				A19	A18	A17	A16
15	255	4KB	0FF000H – 0FFFFFH	1	1	1	1
	:	:	:				
	240	4KB	0F0000H – 0F0FFFH				
14	239	4KB	0EF000H – 0EFFFFH	1	1	1	0
	:	:	:				
	224	4KB	0E0000H – 0E0FFFH				
13	223	4KB	0DF000H – 0DFFFFH	1	1	0	1
	:	:	:				
	208	4KB	0D0000H – 0D0FFFH				
12	207	4KB	0CF000H – 0CFFFFH	1	1	0	0
	:	:	:				
	192	4KB	0C0000H – 0C0FFFH				
11	191	4KB	0BF000H – 0BFFFFH	1	0	1	1
	:	:	:				
	176	4KB	0B0000H – 0B0FFFH				
10	175	4KB	0AF000H – 0AFFFFH	1	0	1	0
	:	:	:				
	160	4KB	0A0000H – 0A0FFFH				
9	159	4KB	09F000H – 09FFFFH	1	0	0	1
	:	:	:				
	144	4KB	090000H – 090FFFH				
8	143	4KB	08F000H – 08FFFFH	1	0	0	0
	:	:	:				
	128	4KB	080000H – 080FFFH				
7	127	4KB	07F000H – 07FFFFH	0	1	1	1
	:	:	:				
	112	4KB	070000H – 070FFFH				
6	111	4KB	06F000H – 06FFFFH	0	1	1	0
	:	:	:				
	96	4KB	060000H – 060FFFH				
5	95	4KB	05F000H – 05FFFFH	0	1	0	1
	:	:	:				
	80	4KB	050000H – 050FFFH				
4	79	4KB	04F000H – 04FFFFH	0	1	0	0
	:	:	:				
	64	4KB	040000H – 040FFFH				
3	63	4KB	03F000H – 03FFFFH	0	0	1	1
	:	:	:				
	48	4KB	030000H – 030FFFH				

2	47	4KB	02F000H – 02FFFFH	0	0	1	0
	:	:	:				
	32	4KB	020000H – 020FFFH				
1	31	4KB	01F000H – 01FFFFH	0	0	0	1
	:	:	:				
	16	4KB	010000H – 010FFFH				
0	15	4KB	00F000H – 00FFFFH	0	0	0	0
	:	:	:				
	0	4KB	000000H – 000FFFH				

Table2 : F25L008A Block Protection Table

TOP

Protection Level	Status Register Bit			Protected Memory Area	
	BP2	BP1	BP0	Block Range	Address Range
0	0	0	0	None	None
Upper 1/16	0	0	1	Block 15	F0000H – FFFFFH
Upper 1/8	0	1	0	Block 14~15	E0000H – FFFFFH
Upper 1/4	0	1	1	Block 12~15	C0000H – FFFFFH
Upper 1/2	1	0	0	Block 8~15	80000H – FFFFFH
All Blocks	1	0	1	Block 0~15	00000H – FFFFFH
All Blocks	1	1	0	Block 0~15	00000H – FFFFFH
All Blocks	1	1	1	Block 0~15	00000H – FFFFFH

BOTTOM

Protection Level	Status Register Bit			Protected Memory Area	
	BP2	BP1	BP0	Block Range	Address Range
0	0	0	0	None	None
Bottom 1/16	0	0	1	Block 0	00000H – 0FFFFH
Bottom 1/8	0	1	0	Block 0~1	00000H – 1FFFFH
Bottom 1/4	0	1	1	Block 0~3	00000H – 3FFFFH
Bottom 1/2	1	0	0	Block 0~7	00000H – 7FFFFH
All Blocks	1	0	1	Block 0~15	00000H – FFFFFH
All Blocks	1	1	0	Block 0~15	00000H – FFFFFH
All Blocks	1	1	1	Block 0~15	00000H – FFFFFH

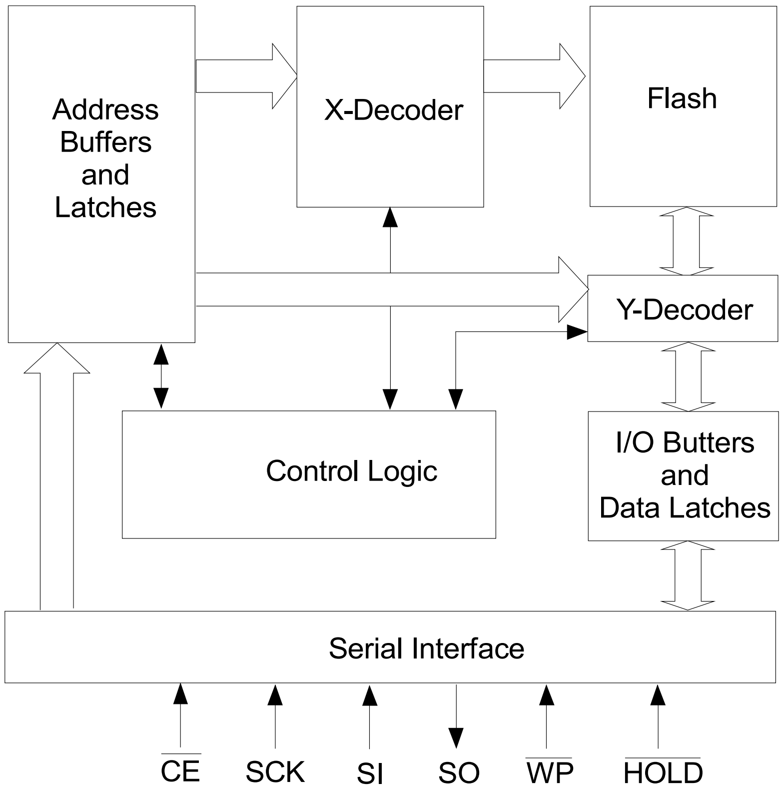
Block Protection (BP2, BP1, BP0)

The Block-Protection (BP2, BP1, BP0) bits define the size of the memory area, as defined in Table2 to be software protected against any memory Write (Program or Erase) operations. The Write-Status-Register (WRSR) instruction is used to program the BP2, P1, BP0 bits as long as $\overline{WP}$ is high or the Block-Protection-Look (BPL) bit is 0. Chip-Erase can only be executed if Block-Protection bits are all 0. After power-up, BP2, BP1 and BP0 are set to1.

Block Protection Lock-Down (BPL)

$\overline{WP}$ pin driven low (V_{IL}), enables the Block-Protection -Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP2, BP1, and BP0 bits. When the $\overline{WP}$ pin is driven high (V_{IH}), the BPL bit has no effect and its value is "Don't Care". After power-up, the BPL bit is reset to 0.

FUNTIONAL BLOCK DIAGRAM



Hold Operation

HOLD pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the HOLD mode, CE must be in active low state. The HOLD mode begins when the SCK active low state coincides with the falling edge of the HOLD signal. The HOLD mode ends when the HOLD signal's rising edge coincides with the SCK active low state.

If the falling edge of the HOLD signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state.

Similarly, if the rising edge of the HOLD signal does not coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 1 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE is driven active high during a Hold condition, it resets the internal logic of the device. As long as HOLD signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD must be driven active high, and CE must be driven active low. See Figure 14 for Hold timing.

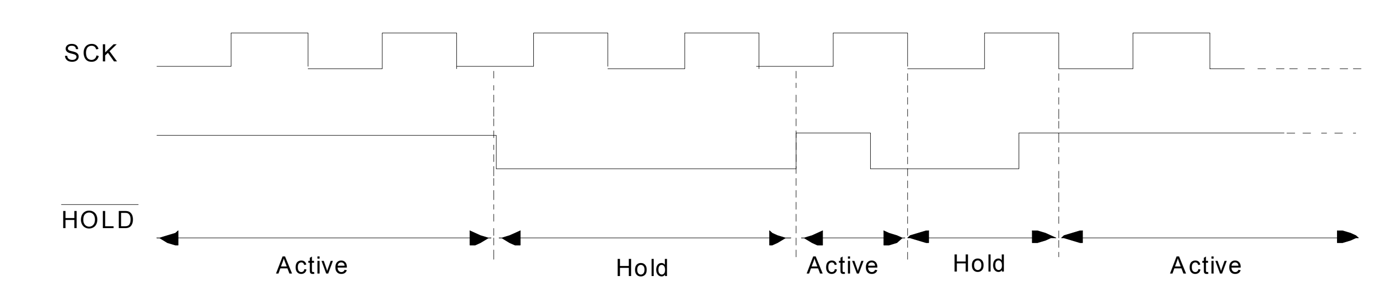


Figure 1 : HOLD CONDITION WAVEFORM

Write Protection

F25L008A provides software Write protection.

The Write Protect pin (WP) enables or disables the lockdown function of the status register. The Block-Protection bits (BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 5 for Block-Protection description.

Write Protect Pin (WP)

The Write Protect (WP) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When WP is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see Table 3). When WP is high, the lock-down function of the BPL bit is disabled.

TABLE3: CONDITIONS TO EXECUTE WRITE-STATUS- REGISTER (WRSR) INSTRUCTION

WP	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the memory Write protection. During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress.
Table 4 describes the function of each bit in the software status register.

TABLE 4: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 5)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 5)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 5)	1	R/W
5	RESERVED	Reserved for future use	0	N/A
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte-Program mode	0	R
7	BPL	1 = BP2,BP1,BP0 are read-only bits 0 = BP2,BP1,BP0 are read/writable	0	R/W

Note1 : Only BP0,BP1,BP2 and BPL are writable

Note2 : All register bits are volatility

Note3 : All area are protected at power-on (BP2=BP1=BP0=1)

Busy

The Busy bit determines whether there is an internal Erase or Program operation in progress. A “1” for the Busy bit indicates the device is busy with an operation in progress. A “0” indicates the device is ready for the next valid operation.

Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If the Write-Enable-Latch bit is set to “1”, it indicates the device is Write enabled. If the bit is set to “0” (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/ Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-up
- Write-Disable (WRDI) instruction completion
- Byte-Program instruction completion
- Auto Address Increment (AAI) programming reached its highest memory address
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Status-Register instructions

Instructions

Instructions are used to Read, Write (Erase and Program), and configure the F25L008A. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Byte-Program, Sector-Erase, Block-Erase, or Chip-Erase instructions, the Write-Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high to low transition of $\overline{CE}$. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. $\overline{CE}$ must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID and Read-Status-Register instructions). Any low to high transition on $\overline{CE}$, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to the standby mode.

Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

TABLE 5: DEVICE OPERATION INSTRUCTIONS

Cycle Type/ Operation[1,2]	Max Freq	Bus Cycle 1		2		3		4		5		6	
		S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}
Read	33 MHz	03H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	X	D_{OUT}		
High-Speed-Read		0BH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	X	X	X	D_{OUT}
Sector-Erase[4,5] (4K Byte)		20H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	-	-		
Block-Erase (64K Byte)		D8H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	-	-		
Chip-Erase[6]		60H C7H	Hi-Z	-	-	-	-	-	-	-	-		
Byte-Program[5]		02H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	D_{IN}	Hi-Z		
Auto-Address-Increment-word programming (AAI)		ADH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	$D_{IN}0$	Hi-Z	$D_{IN}1$	Hi-Z
Read-Status-Register (**RDSR**)		05H	Hi-Z	X	D_{OUT}	-	Note[7]	-	Note[7]	-	Note[7]		
Enable-Write-Status-Register (**EWSR**)[8]	50MHz	50H	Hi-Z	-	-	-	-	-	-	-	-		
Write-Status-Register (**WRSR**)[8]		01H	Hi-Z	Data	Hi-Z	-	-	-.	-	-	-		
Write-Enable (**WREN**)[11]		06H	Hi-Z	-	-	-	-	-	-	-	-		
Write-Disable (**WRDI**)	100MHz	04H	Hi-Z	-									
Read-Electronic-Signature (**RES**)		ABH	Hi-Z	X	13H	-	-	-	-	-	-		
Jedec-Read-ID (**JEDEC-ID**)[10]		9FH	Hi-Z	X	8CH	X	20H(Top) 21H(Bottom)	X	14H	-	-		
Read-ID (**RDID**)		90H (A0=0) 90H (A0=1)	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_{8}	Hi-Z	A_{7}-A_{0}	Hi-Z	X	8CH 13H	X	13H 8CH
Enable SO to output RY/BY# Status during AAI (**EBSY**)		70H	Hi-Z	-	-	-	-	-	-	-	-		
Disable SO to output RY/BY# Status during AAI (**DBSY**)		80H	Hi-Z	-	-	-	-	-	-	-	-		

1. Operation: S_{IN} = Serial In, S_{OUT} = Serial Out
2. X = Dummy Input Cycles (V_{IL} or V_{IH}); - = Non-Applicable Cycles (Cycles are not necessary)
3. One bus cycle is eight clock periods.
4. Sector addresses: use AMS-A12, remaining addresses can be V_{IL} or V_{IH}
5. Prior to any Byte-Program, Sector-Erase , Block-Erase ,or Chip-Erase operation, the Write-Enable (WREN) instruction must be executed.
6. To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by the data to be programmed.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on $\overline{CE}$.
8. The Enable-Write-Status-Register (EWSR) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the EWSR instruction to make both

instructions effective.

9. The Read-Electronic-Signature is continuous with on going clock cycles until terminated by a low to high transition on $\overline{CE}$.
10. The Jedec-Read-ID is output first byte 8CH as manufacture ID; second byte 20H as top memory type and second byte 21H as bottom memory type ; third byte 14H as memory capacity.
11. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both instructions effective. Both EWSR and WREN can enable WRSR, user just need to execute one of it. A successful WRSR can reset WREN.

Read (33 MHz)

The Read instruction supports up to 33 MHz, it outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on $\overline{CE}$. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 8Mbit density, once the data from address location FFFFFH had been read, the next output will be from address location 00000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A_{23}-A_0]. $\overline{CE}$ must remain active low for the duration of the Read cycle. See Figure 2 for the Read sequence.

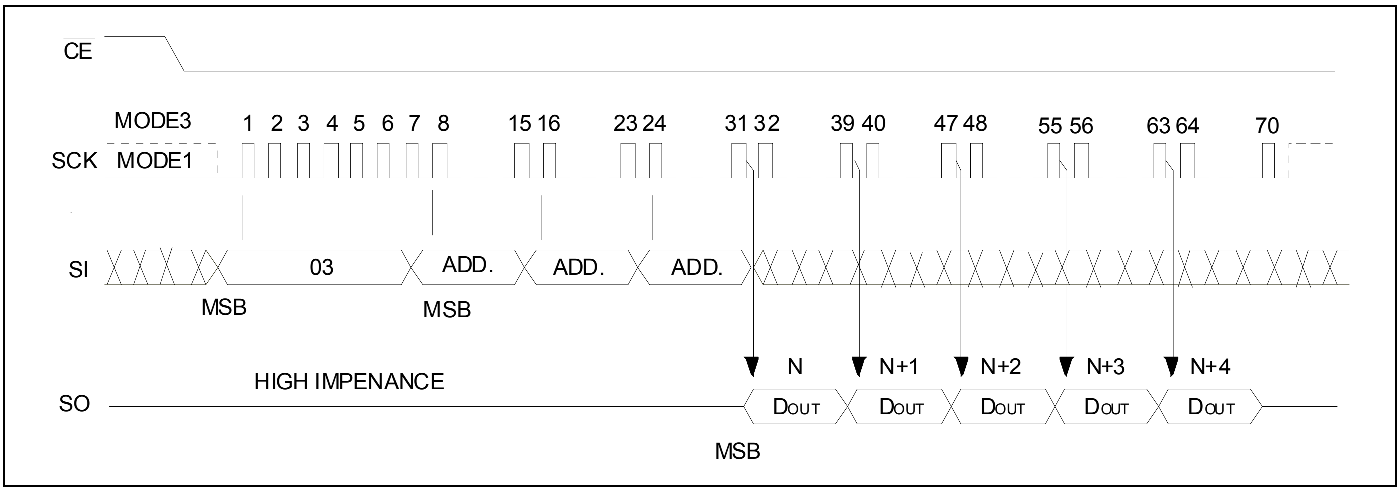


Figure 2 : READ SEQUENCE

Fast-Read (50 MHz ; 100 MHz)

The High-Speed-Read instruction supporting up to 100 MHz is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23}-A_0] and a dummy byte. $\overline{CE}$ must remain active low for the duration of the High-Speed-Read cycle. See Figure 3 for the High-Speed-Read sequence.

Following a dummy byte (8 clocks input dummy cycle), the High-Speed-Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on $\overline{CE}$. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 8Mbit density, once the data from address location FFFFFH has been read, the next output will be from address location 000000H.

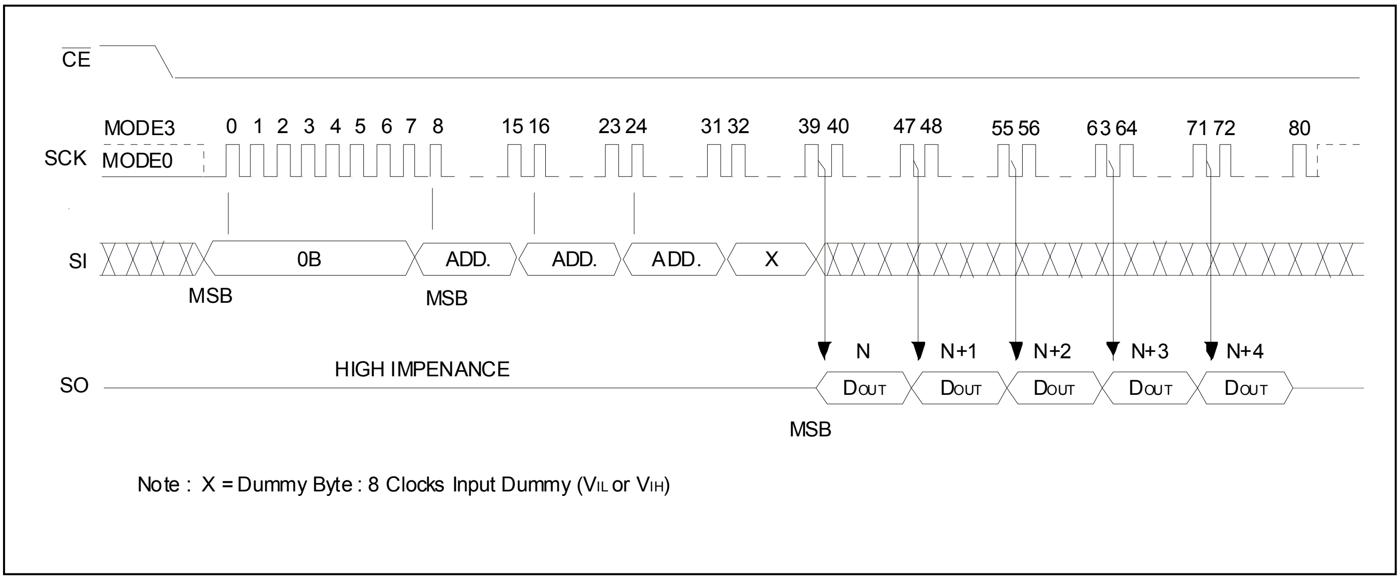


Figure 3 : HIGH-SPEED-READ SEQUENCE

Byte-Program

The Byte-Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. A Byte-Program instruction applied to a protected memory area will be ignored.
Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the Byte-Program instruction. The Byte-Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A_{23}-A_0]. Following the address, the data is input in order from MSB (bit 7) to LSB (bit 0). $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait TBP for the completion of the internal self-timed Byte-Program operation. See Figure 4 for the Byte-Program sequence.

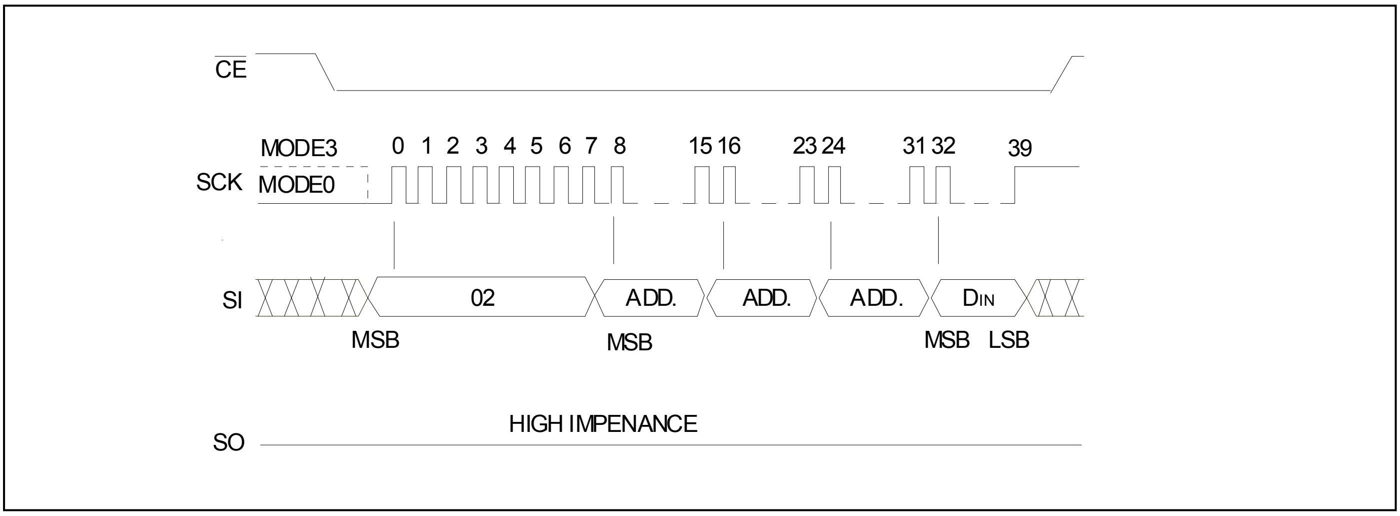


Figure 4 : BYTE-PROGRAM SEQUENCE

Auto Address Increment (AAI) WORD Program

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when the multiple bytes or entire memory array is to be programmed. An AAI program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI program instruction. While within AAI WORD programming sequence, the only valid instructions are AAI WORD program operation, RDSR, WRDI. Users have three options to determine the completion of each AAI WORD program cycle: hardware detection by reading the SO; software detection by polling the BUSY in the software status register or wait T_{BP}. Refer to End-of-Write Detection section for details.

Prior to any write operation, the Write-Enable (WREN) instruction must be executed. The AAI WORD program instruction is initiated by executing an 8-bit command, ADH, followed by address bits [A_{23}-A_0]. Following the addresses, two bytes of data is input sequentially. The data is input sequentially from MSB (bit 7) to LSB (bit 0). The first byte of data(DO) will be programmed into the initial address [A_{23}-A_1] with A_0 =0; The second byte of data(D1) will be programmed into the initial address [A_{23}-A_1] with A_0 =1. $\overline{CE}$ must be driven high before the AAI WORD program instruction is executed. The user must check the BUSY status before entering the next valid command. Once the device indicates it is no longer busy, data for next two sequential addresses may be programmed and so on. When the last desired byte had been entered, check the busy status using the hardware method or the RDSR instruction and execute the WRDI instruction, to terminate AAI. User must check busy status after WRDI to determine if the device is ready for any command. Please refer to Figures 9 and Figures 10.

There is no wrap mode during AAI programming; once the highest unprotected memory address is reached, the device will exit AAI operation and reset the Write-Enable-Latch bit (WEL = 0) and the AAI bit (AAI=0).

End of Write Detection

There are three methods to determine completion of a program cycle during AAI WORD programming: hardware detection by reading the SO, software detection by polling the BUSY bit in the Software Status Register or wait T_{BP}. The hardware end of write detection method is described in the section below.

Hardware End of Write Detection

The hardware end of write detection method eliminates the overhead of polling the BUSY bit in the software status register during an AAI Word PROGRAM OPERATION. The 8bit command, 70H, configures the SO to indicate Flash Busy status during AAI WORD programming (refer to figure7). The 8bit command, 70H, must be executed prior to executing an AAI WORD program instruction. Once an internal programming operation begins, asserting $\overline{CE}$ will immediately drive the status of the internal flash status on the SO pin. A “0” Indicates the device is busy ; a “1” Indicates the device is ready for the next instruction. De-asserting $\overline{CE}$ will return the SO pin to tri-state. The 8bit command, 80H,disables the SO pin to output busy status during AAI WORD program operation and return SO pin to output software register data during AAI WORD programming (refer to figure8).

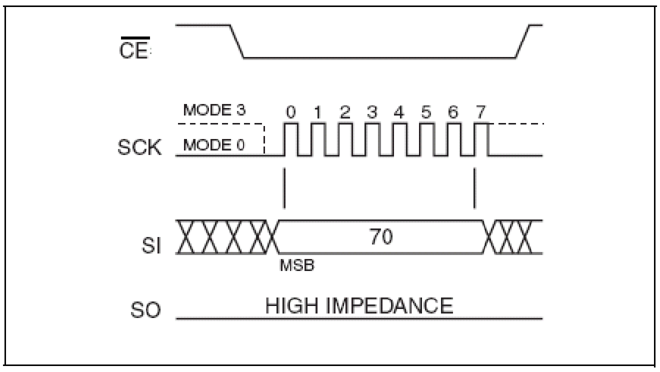


FIGURE 8 : ENABLE SO AS HARDWARE $\overline{RY/BY}$ DURING AAI PROGRAMMING

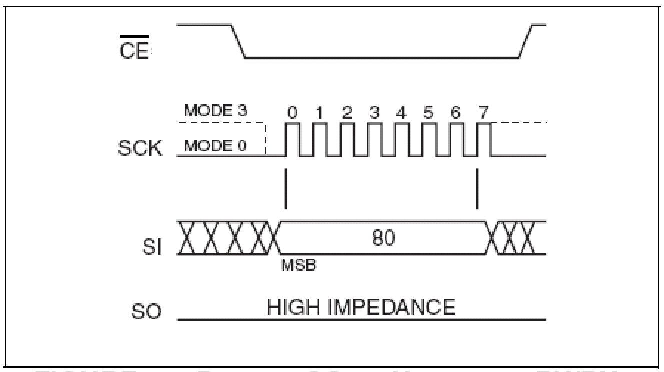


FIGURE 9 : DISABLE SO AS HARDWARE $\overline{RY/BY}$ DURING AAI PROGRAMMING

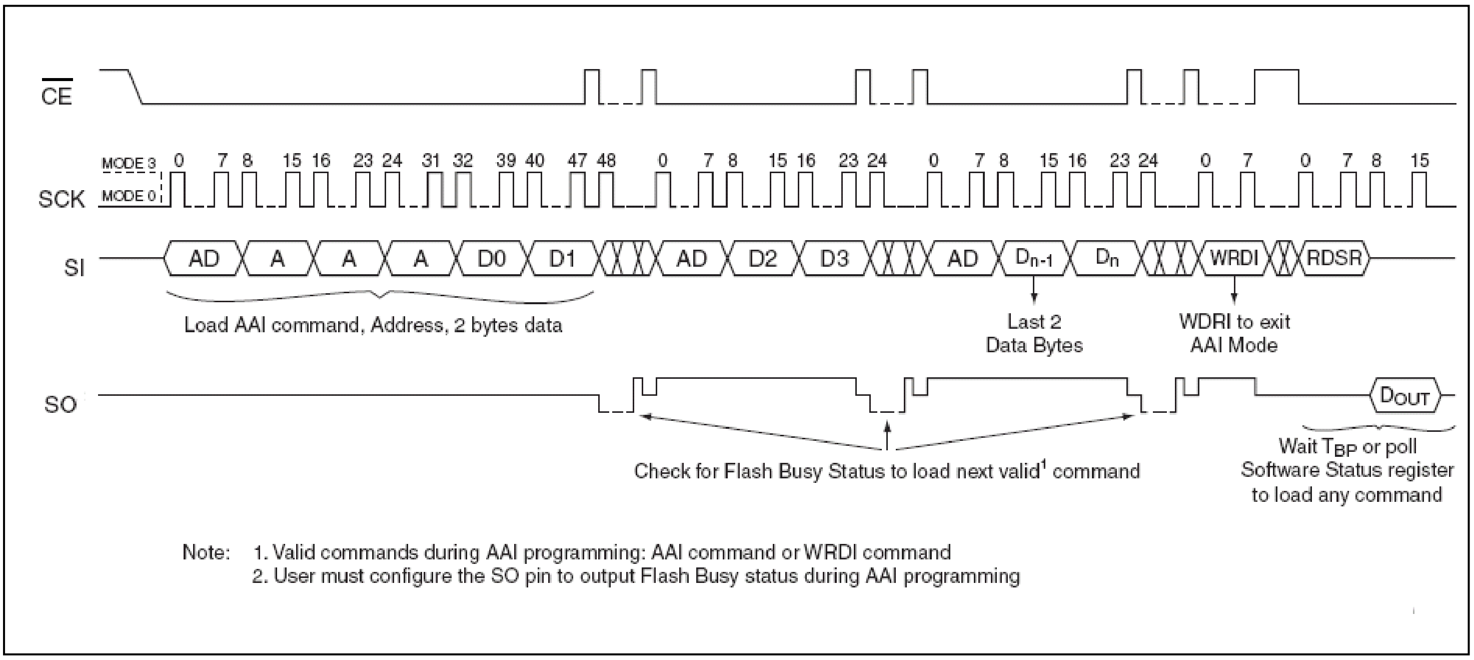


FIGURE 10 : AUTO ADDRESS INCREMENT (AAI) WORD-PROGRAM SEQUENCE WITH HARDWARE END-OF-WRITE DETETION

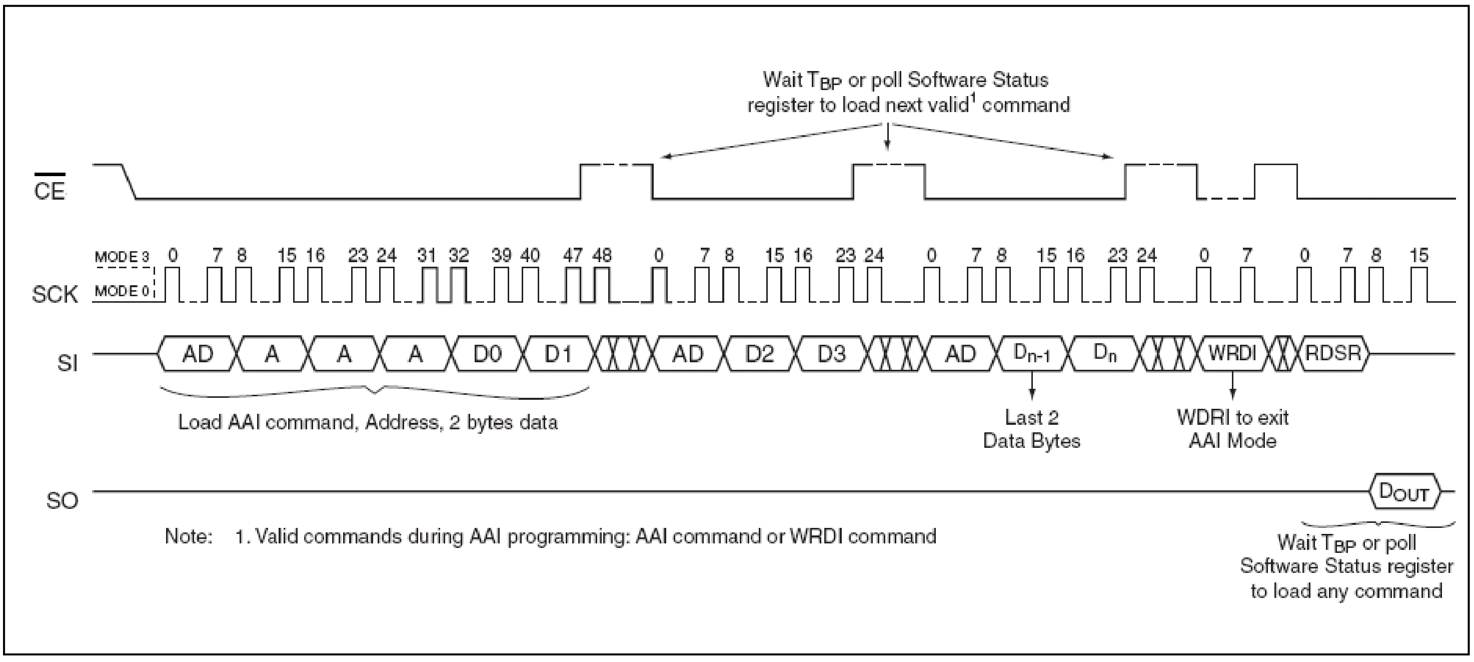


FIGURE 11 : AUTO ADDRESS INCREMENT (AAI) WORD-PROGRAM SEQUENCE WITH SOFTWARE END-OF-WRITE DETETION

64K-Byte Block-Erase

The 64K Byte Block-Erase instruction clears all bits in the selected block to FFH. A Block-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the any command sequence. The Block-Erase instruction is initiated by executing an 8-bit command, D8H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{16}] (A_{MS} = Most Significant address) are used to determine the block address (BA_X), remaining address bits can be VIL or VIH. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait TBE for the completion of the internal self-timed Block-Erase cycle. See Figure 5 for the Block-Erase sequence.

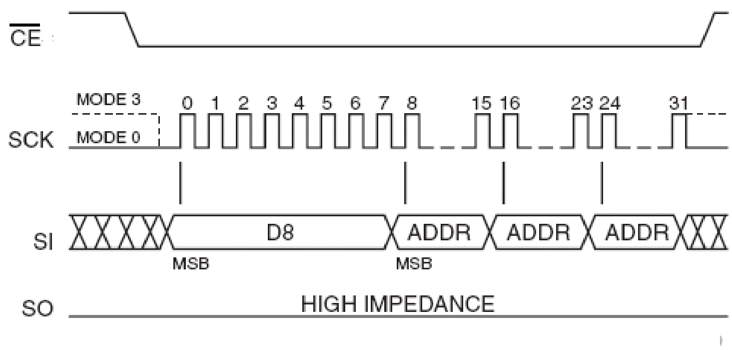


FIGURE 5 : 64-KBYTE BLOCK-ERASE SEQUENCE

4K-Byte-Sector-Erase

The Sector-Erase instruction clears all bits in the selected sector to FFH. A Sector-Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the any command sequence. The Sector-Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A_{23}-A_0]. Address bits [A_{MS}-A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA_X), remaining address bits can be VIL or VIH. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait TSE for the completion of the internal self-timed Sector-Erase cycle. See Figure 6 for the Sector-Erase sequence.

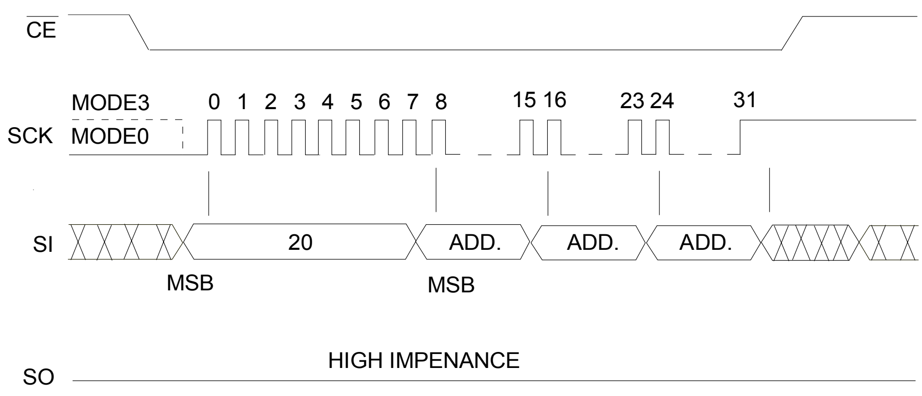


FIGURE 6 : SEQUENCE-ERASE SEQUENCE

Chip-Erase

The Chip-Erase instruction clears all bits in the device to FFH. A Chip-Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write-Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the Chip-Erase instruction sequence. The Chip-Erase instruction is initiated by executing an 8-bit command, 60H or C7H. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the Busy bit in the software status register or wait T_{CE} for the completion of the internal self-timed Chip-Erase cycle.
See Figure 7 for the Chip-Erase sequence.

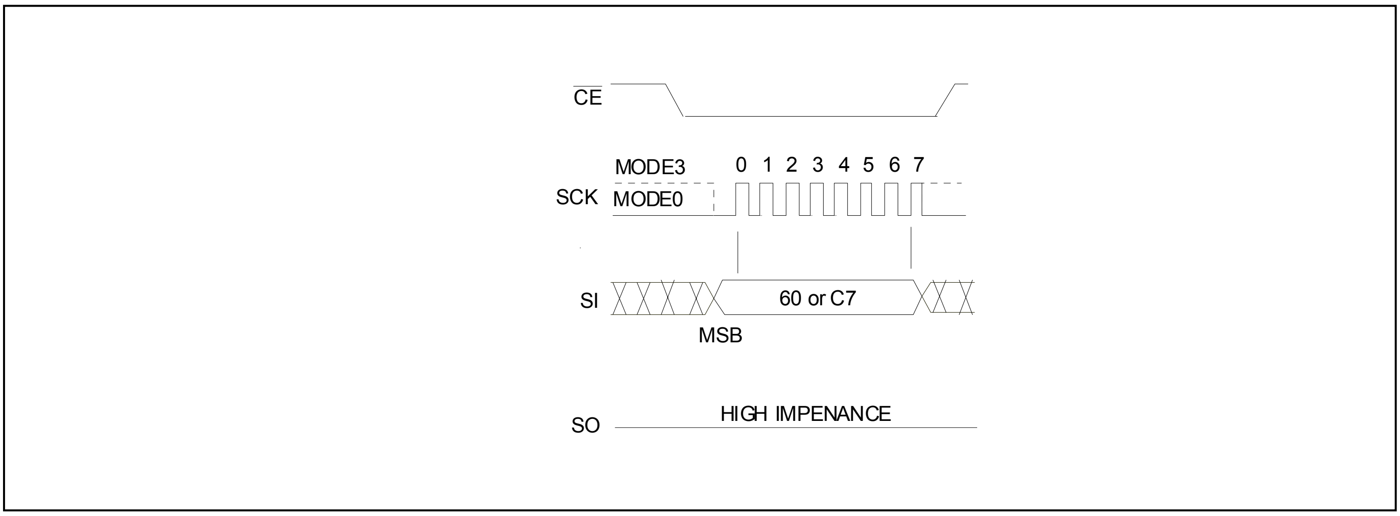


FIGURE 7 : CHIP-ERASE SEQUENCE

Read-Status-Register (RDSR)

The Read-Status-Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation.
When a Write operation is in progress, the Busy bit may be checked before sending any new commands to assure that the new commands are properly received by the device.
$\overline{CE}$ must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read-Status-Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the $\overline{CE}$
See Figure 8 for the RDSR instruction sequence.

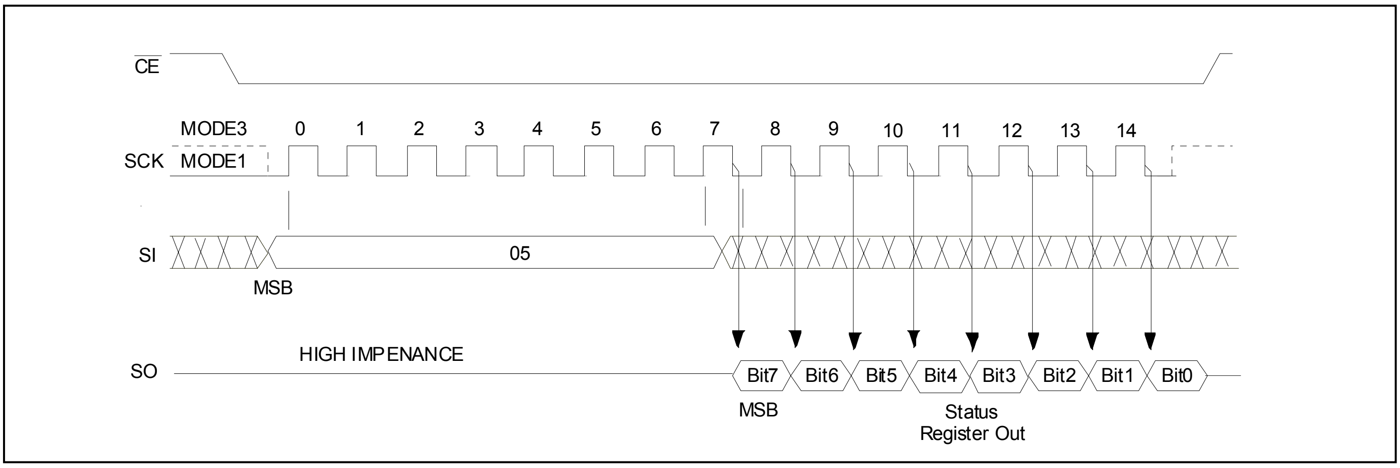


Figure 8 : READ-STATUS-REGISTER (RDSR) SEQUENCE

Write-Enable (WREN)

The Write-Enable (WREN) instruction sets the Write-Enable-Latch bit to 1 allowing Write operations to occur. The WREN instruction must be executed prior to any Write (Program/Erase) operation. $\overline{CE}$ must be driven high before the WREN instruction is executed.

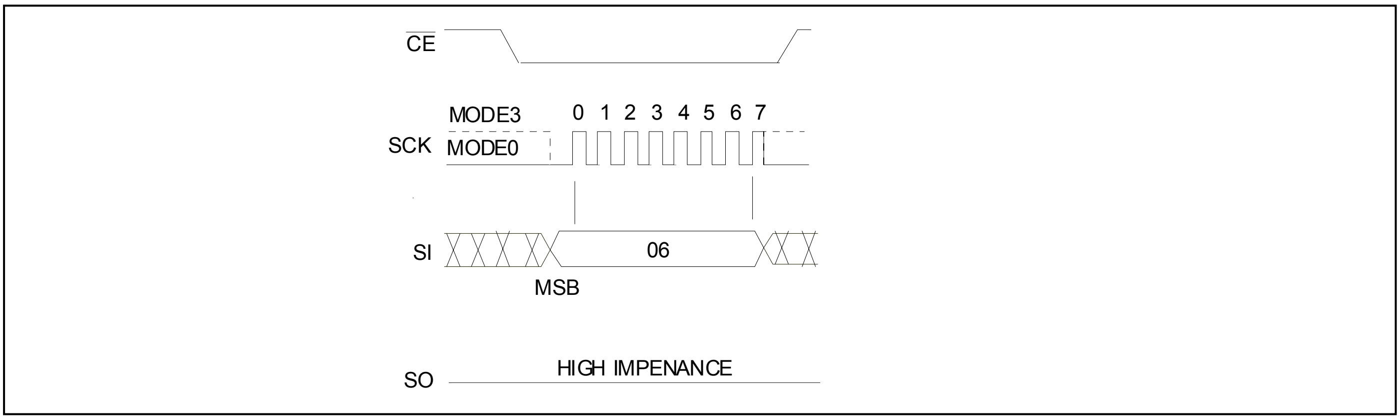


FIGURE 9 : WRITE ENABLE (WREN) SEQUENCE

Write-Disable (WRDI)

The Write-Disable (WRDI) instruction resets the Write-Enable-Latch bit disabling any new Write operations from occurring. $\overline{CE}$ must be driven high before the WRDI instruction is executed.

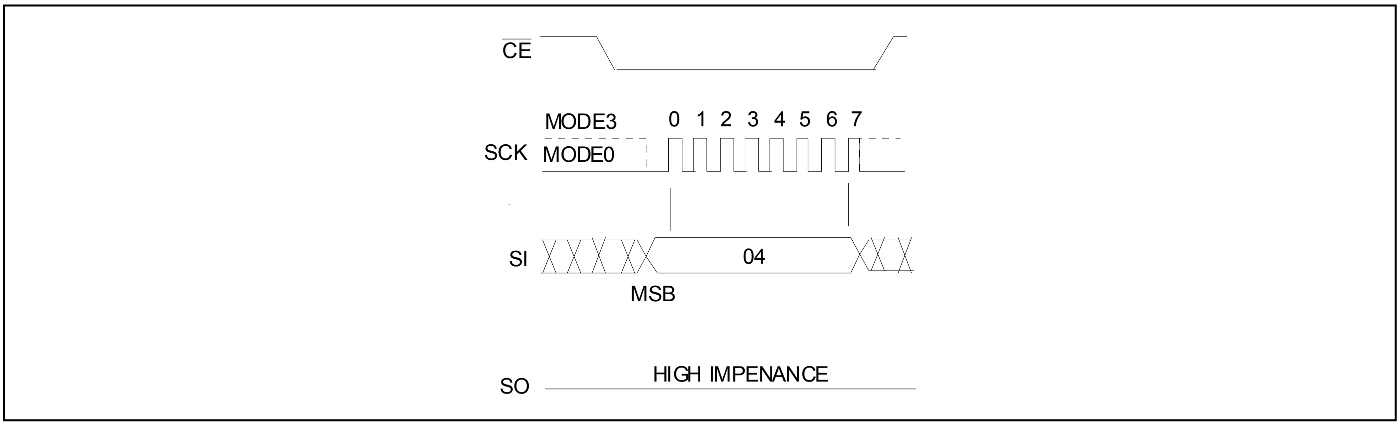


Figure 10 : WRITE DISABLE (WRDI) SEQUENCE

Enable-Write-Status-Register (EWSR)

The Enable-Write-Status-Register (EWSR) instruction arms the Write-Status-Register (WRSR) instruction and opens the status register for alteration. The Enable-Write-Status-Register instruction does not have any effect and will be wasted, if it is not followed immediately by the Write-Status-Register (WRSR) instruction. $\overline{CE}$ must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

Write-Status-Register (WRSR)

The Write-Status-Register instruction writes new values to the BP2, BP1, BP0, and BPL bits of the status register. $\overline{CE}$ must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 11 for EWSR or WREN and WRSR instruction sequences.

Executing the Write-Status-Register instruction will be ignored when $\overline{WP}$ is low and BPL bit is set to “1”. When the $\overline{WP}$ is low, the BPL bit can only be set from “0” to “1” to lockdown the status register, but cannot be reset from “1” to “0”.

When $\overline{WP}$ is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1,and BP2 bits in the status register can all be changed. As long as BPL bit is set to 0 or $\overline{WP}$ pin is driven high (V_{IH}) prior to the low-to-high transition of the $\overline{CE}$ pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to “1” to lock down the status register as well as altering the BP0 ;BP1 and BP2 bits at the same time. See Table 3 for a summary description of $\overline{WP}$ and BPL functions.

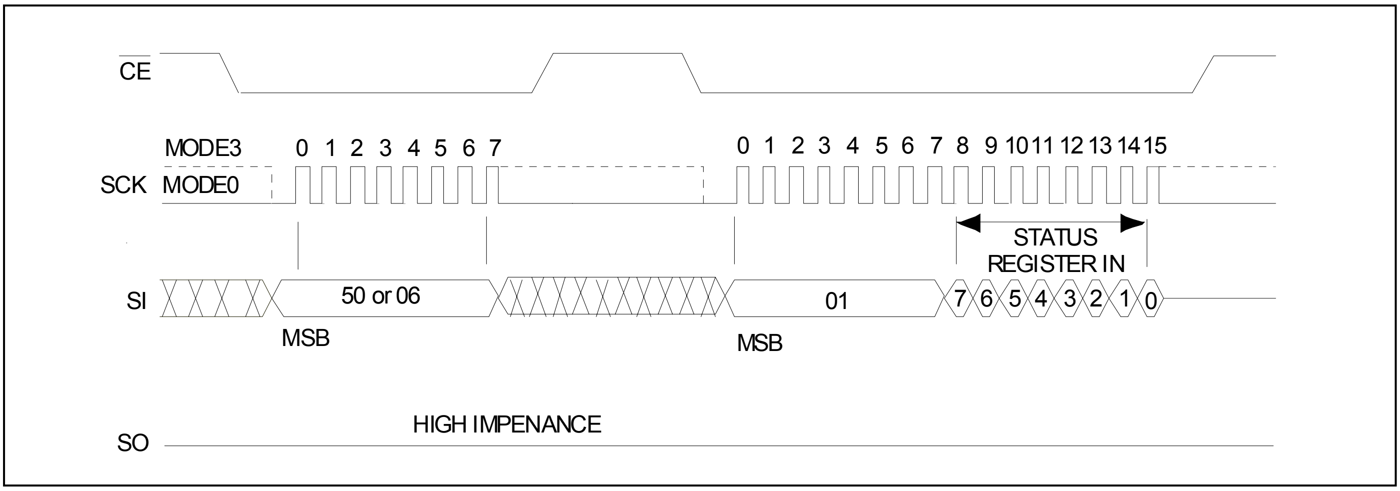


Figure 11 : ENABLE-WRITE-STATUS-REGISTER (EWSR) or WRITE-ENABLE(WREN) and WRITE-STATUS-REGISTER (WRSR)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . -55°C to +125°C
Storage Temperature . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . -0.5V to VDD+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . -2.0V to VDD+2.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . 240°C
Output Short Circuit Current1. . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . 5 ns
Output Load . . . . C_L = 15 pF for ≧75MHz
. . . . C_L = 30 pF for ≦50MHz
See Figures 12 and 13

TABLE 6: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V ; TA=0~70oC

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DDR}	Read Current		15	mA	$\overline{CE}$ =0.1 V_{DD}/0.9 V_{DD}@33 MHz, SO=open
I_{DDW}	Program and Erase Current		40	mA	$\overline{CE}$ =V_{DD}
I_{SB}	Standby Current		75	µA	$\overline{CE}$ =V_{DD}, VIN=V_{DD} or V_{SS}
I_{LI} I_{LO}	Input Leakage Current Output Leakage Current		1 1	µA µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	0.7 V_{DD}	0.8	V V	V_{DD}=V_{DD} Min V_{DD}=V_{DD} Max
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	V_{DD}-0.2	0.2	V V	I_{OL}=100 µA, V_{DD}=V_{DD} Min I_{OH}=-100 µA, V_{DD}=V_{DD} Min

TABLE 7 : RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	10	µs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	10	µs

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Read-Electronic-Signature (RES)

The RES instruction can be used to read the 8-bit Electronic Signature of the device on the SO pin. The RES instruction can provide access to the Electronic Signature of the device (except while an Erase, Program or WRSR cycle is in progress), Any ERS instruction executed while an Erase, Program or WRSR cycle is in progress is no decoded, and has no effect on the cycle in progress.

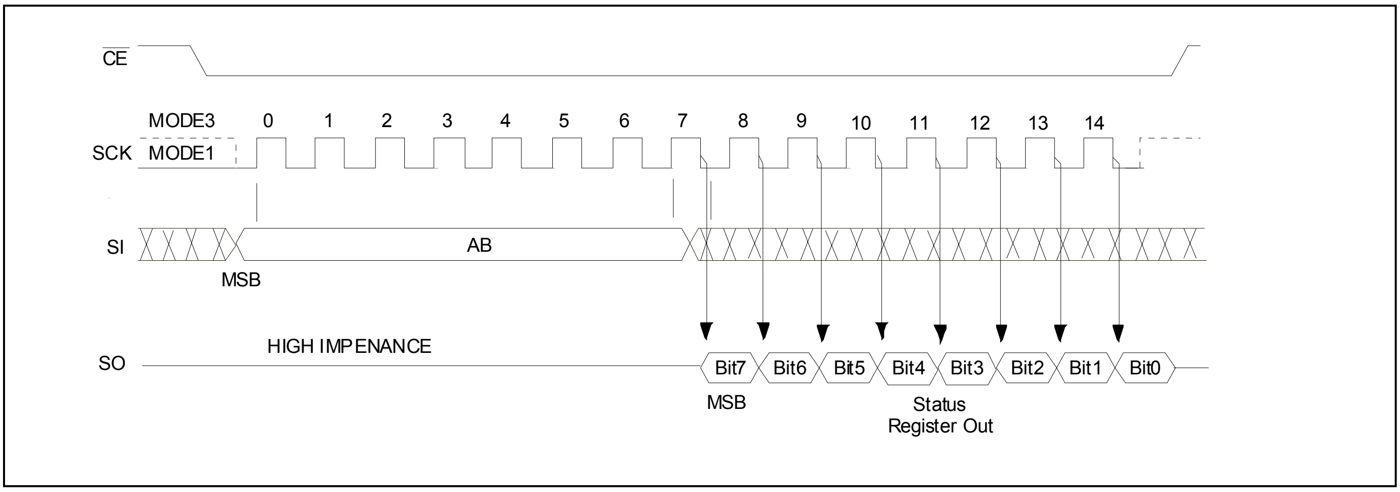


Figure 12 : Read-Electronic-Signature (RES)

JEDEC Read-ID

The JEDEC Read-ID instruction identifies the device as F25L008A and the manufacturer as ESMT. The device information can be read from executing the 8-bit command,.9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, 8CH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. Byte1, BFH, identifies the manufacturer as ESMT. Byte2, 20H (for TOP), 21H (for BOTTOM),identifies the memory type as SPI Flash. Byte3, 14H, identifies the device as F25L008A. The instruction sequence is shown in Figure13.

The JEDEC Read ID instruction is terminated by a low to high transition on $\overline{CE}$ at any time during data output. If no other command is issued after executing the JEDEC Read-ID instruction, issue a 00H (NOP) command before going into Standby Mode ($\overline{CE}$ =V_{IH}).

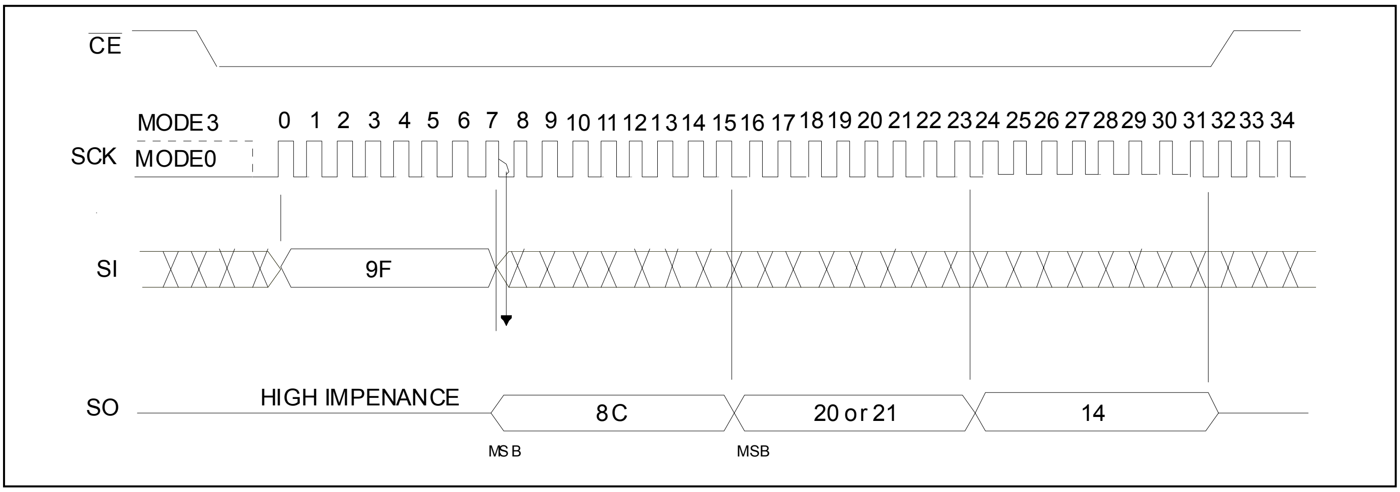


Figure 13 : Jedec Read ID Sequence

Table 9 : JEDEC READ-ID DATA

Manufacturer's ID	**Device ID**	
	Memory Type	**Memory Capacity**
Byte1	Byte 2	Byte 3
8CH	20H (for TOP)	14H
	21H (for Bottom)	

Read-ID (RDID)

The Read-ID instruction (RDID) identifies the devices as F25L008A and manufacturer as ESMT. This command is backward compatible to all ESMT SPI devices and should be used as default device identification when multiple versions of ESMT SPI devices are used in one design. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits [A_{23}-A_0]. Following the Read-ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low to high transition on $\overline{CE}$.

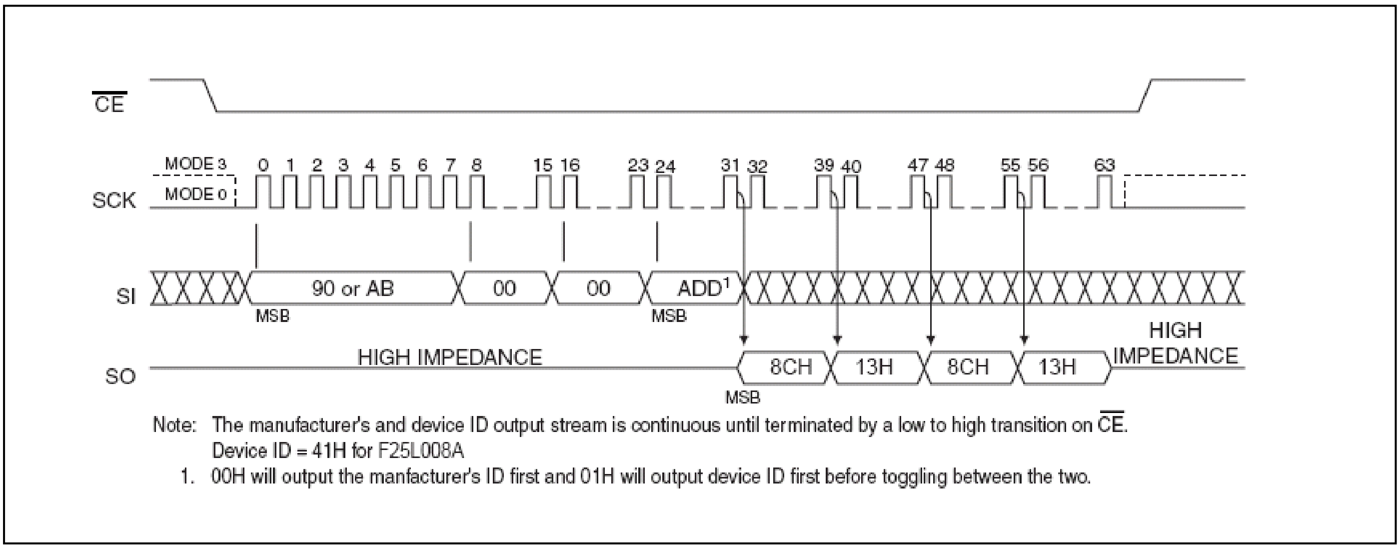


Figure 14 : Read-Electronic-Signature

Table 10 : JEDEC READ-ID DATA

	Address	**Byte1**	**Byte2**
Manufacturer's ID	00000H	8CH	13H
Device ID ESMT F25L008A	00001H	13H	8CH

TABLE 11: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	10	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + IDD	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12 : AC OPERATING CHARACTERISTICS T_A=0~70oC

		Normal 33MHz		Fast 50 MHz		Fast 100 MHz		
		VDD=2.7~3.6V		VDD=2.7~3.6V		VDD=3.0~3.6V		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
F_{CLK}	Serial Clock Frequency		33		50		100	MHz
T_{SCKH}	Serial Clock High Time	13		9		5		ns
T_{SCKL}	Serial Clock Low Time	13		9		5		ns
T_{CES}[1]	$\overline{CE}$ Active Setup Time	5		5		5		ns
T_{CEH}[1]	$\overline{CE}$ Active Hold Time	5		5		5		ns
T_{CHS}[1]	$\overline{CE}$ Not Active Setup Time	5		5		5		ns
T_{CHH}[1]	$\overline{CE}$ Not Active Hold Time	5		5		5		ns
T_{CPH}	$\overline{CE}$ High Time	100		100		100		ns
T_{CHZ}	$\overline{CE}$ High to High-Z Output		9		9		9	ns
T_{CLZ}	SCK Low to Low-Z Output	0		0		0		ns
T_{DS}	Data In Setup Time	3		3		3		ns
T_{DH}	Data In Hold Time	3		3		3		ns
T_{HLS}	$\overline{HOLD}$ Low Setup Time	5		5		5		ns
T_{HHS}	$\overline{HOLD}$ High Setup Time	5		5		5		ns
T_{HLH}	$\overline{HOLD}$ Low Hold Time	5		5		5		ns
T_{HHH}	$\overline{HOLD}$ High Hold Time	5		5		5		ns
T_{HZ}	$\overline{HOLD}$ Low to High-Z Output		9		9		9	ns
T_{LZ}	$\overline{HOLD}$ High to Low-Z Output		9		9		9	ns
T_{OH}	Output Hold from SCK Change	0		0		0		ns
T_V	Output Valid from SCK		12		8		7	ns

1. Relative to SCK.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits		Unit
	Typ.(2)	Max.(3)	
Sector Erase Time	60	120	ms
Block Erase Time	1	2	s
Chip Erase Time	8	30	s
Byte Programming Time	7	30	us
Chip Programming Time	25	100	s
Erase/Program Cycles (1)	100,000	-	Cycles
Data Retention	20	-	Years

Notes:

1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25°C, 3V.
3.Maximum values measured at 85°C, 2.7V.

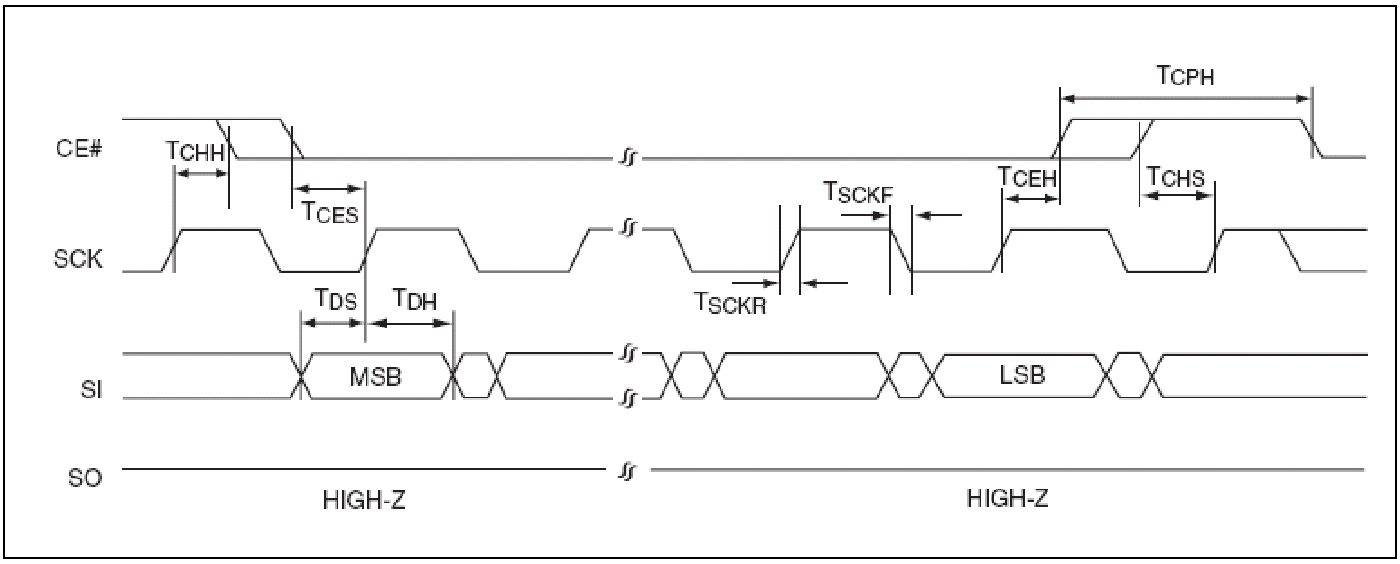


FIGURE 15: SERIAL INPUT TIMING DIAGRAM

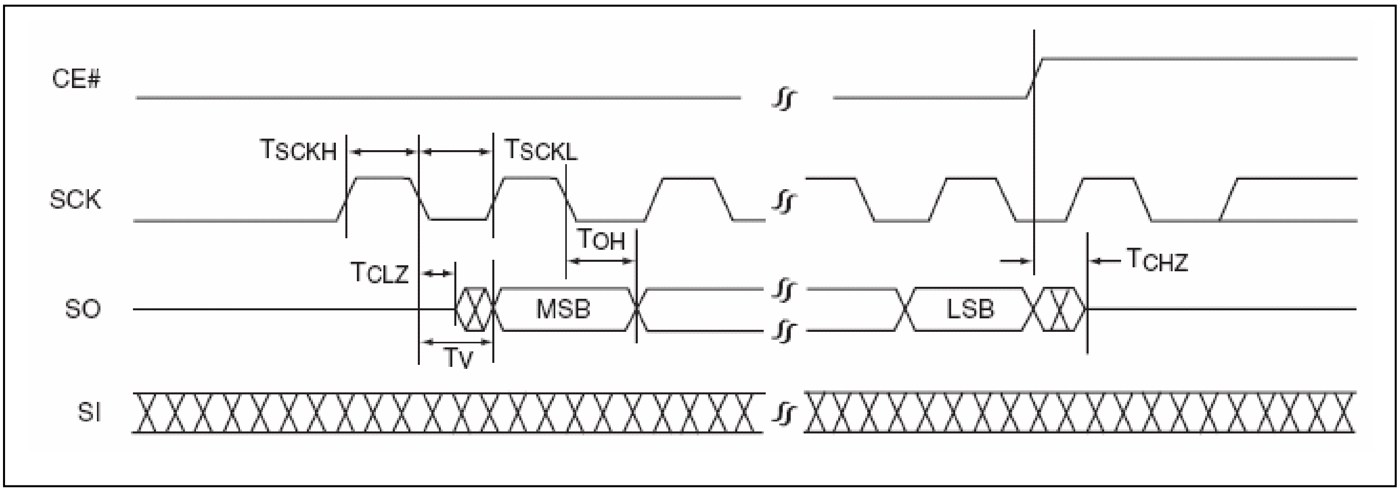


FIGURE 16: SERIAL OUTPUT TIMING DIAGRAM

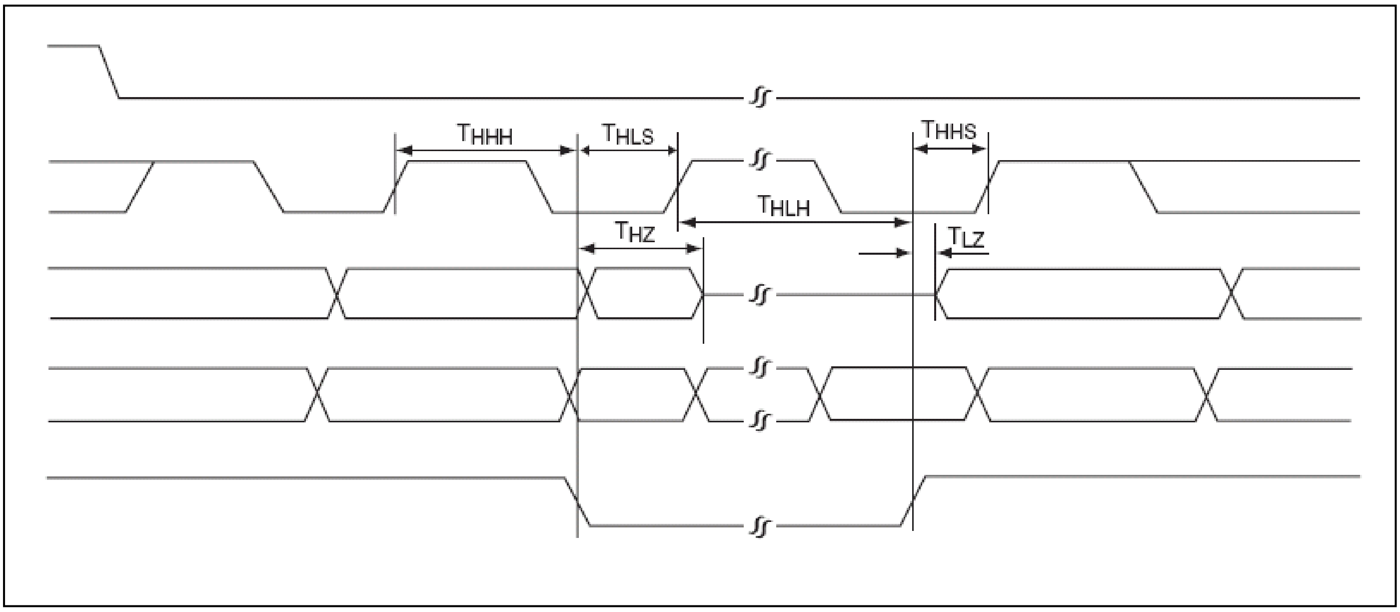


FIGURE 17: HOLD TIMING DIAGRAM

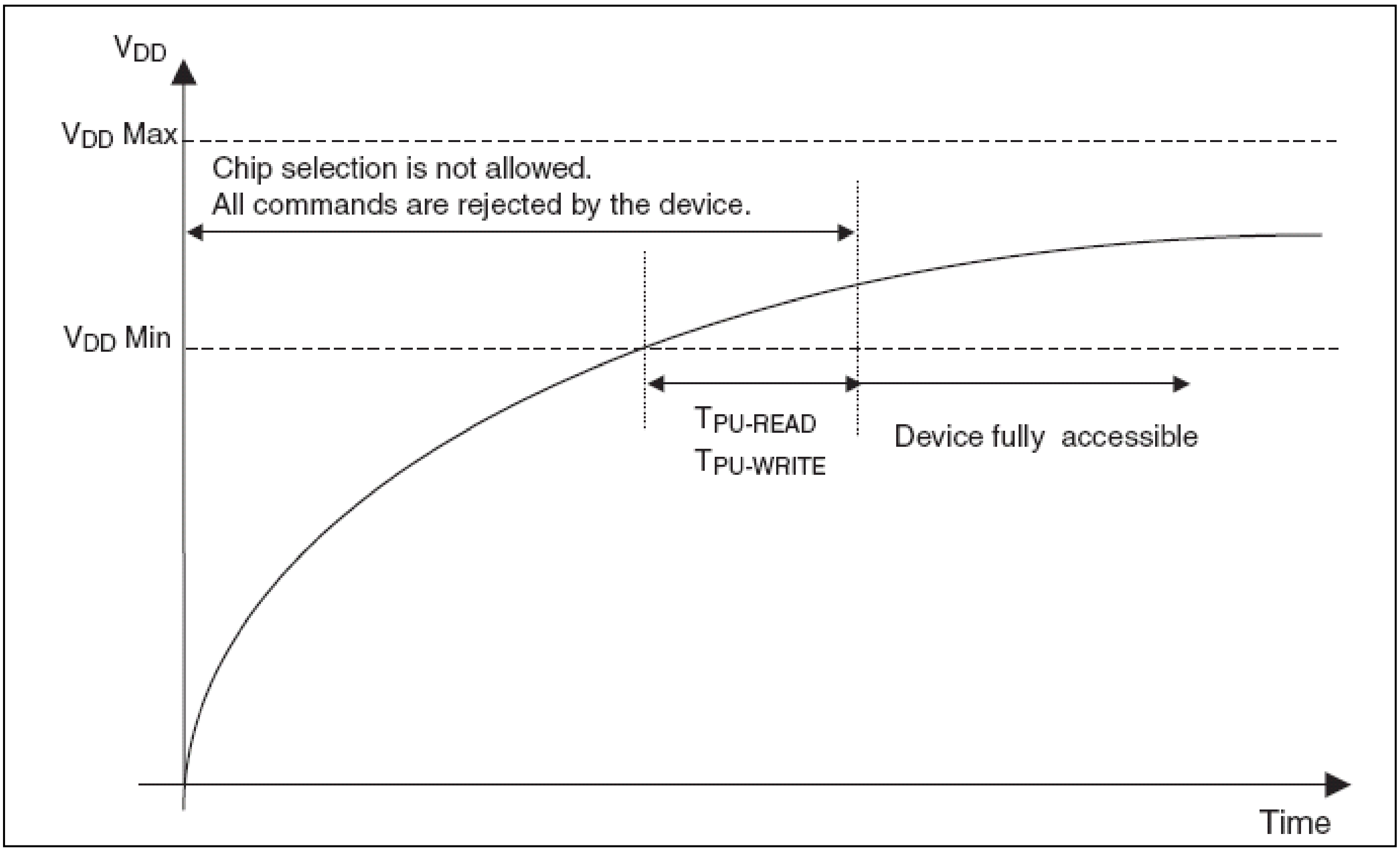


FIGURE 18: POWER-UP TIMING DIAGRAM

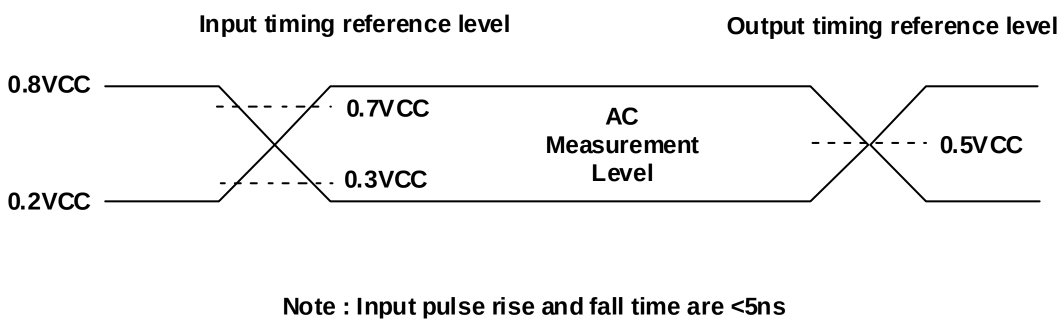


FIGURE 19 : AC INPUT/OUTPUT REFERENCE WAVEFORMS

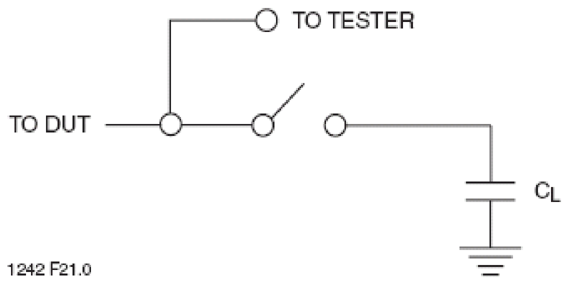
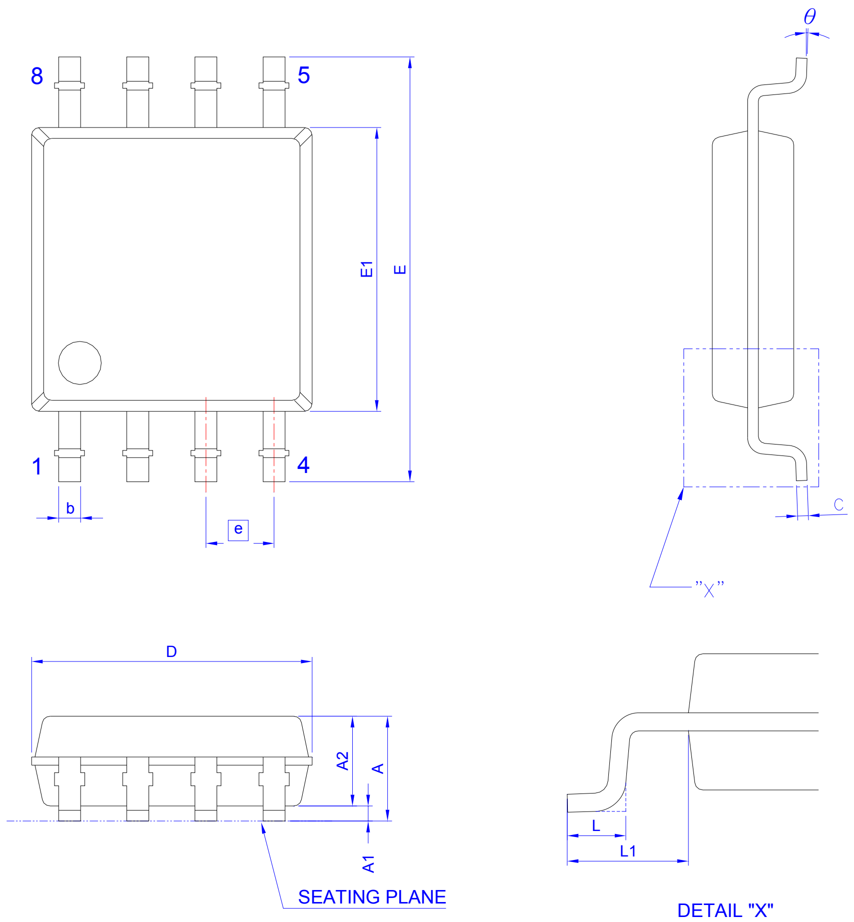


FIGURE 20: A TEST LOAD EXAMPLE

PACKING DIMENSIONS

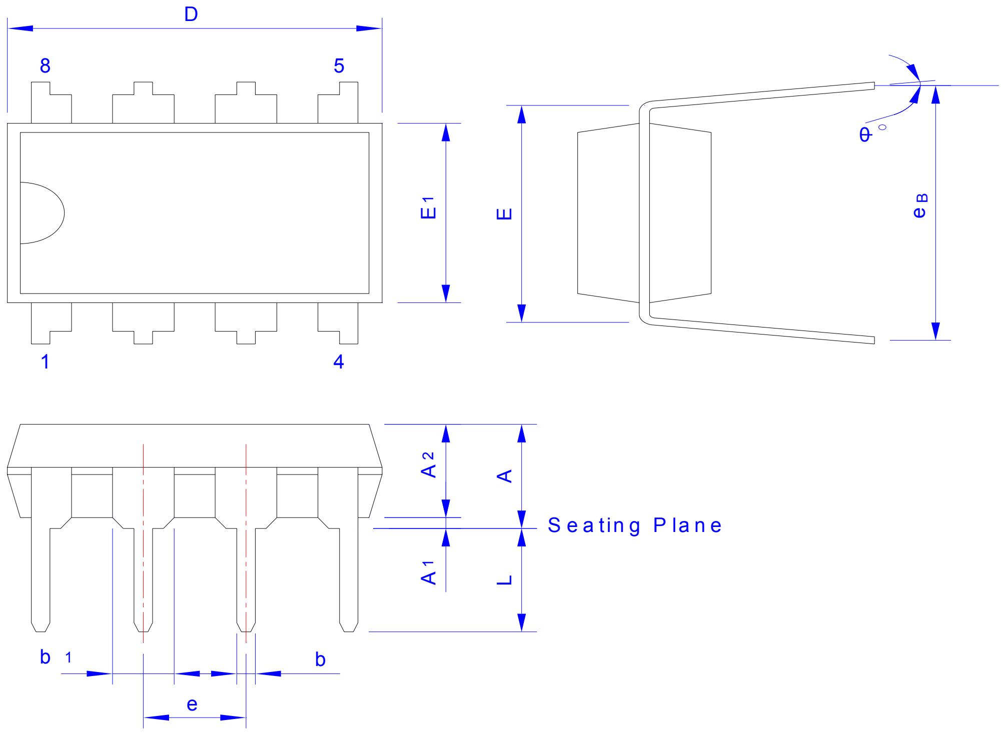
8-LEAD SOP (200 mil)



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	---	---	2.16	---	---	0.085	E	7.70	7.90	8.10	0.303	0.311	0.319
A_1	0.05	0.15	0.25	0.002	0.006	0.010	E_1	5.18	5.28	5.38	0.204	0.208	0.212
A_2	1.70	1.80	1.91	0.067	0.071	0.075	L	0.50	0.65	0.80	0.020	0.026	0.032
b	0.36	0.41	0.51	0.014	0.016	0.020	e	1.27 BSC			0.050 BSC		
c	0.19	0.20	0.25	0.007	0.008	0.010	L_1	1.27	1.37	1.47	0.050	0.054	0.058
D	5.13	5.23	5.33	0.202	0.206	0.210	θ	0°	---	8°	0°	---	8°

Controlling dimension : millimenter

PACKING DIMENSIONS
8-Leads P-DIP (300 MIL)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	5.00	——	——	0.21
A_1	0.38	——	——	0.015	——	——
A_2	3.18	3.30	3.43	0.125	0.130	0.135
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62 BSC.			0.300 BSC.		
E_1	6.22	6.35	6.48	0.245	0.250	0.255
L	9.02	9.27	10.16	0.115	0.130	0.150
e	2.54 TYP.			0.100 TYP.		
e_B	8.51	9.02	9.53	0.335	0.355	0.375
b	0.46 TYP.			0.018 TYP.		
b_1	1.52 TYP.			0.060 TYP.		
θ^{o}	0^{o}	7^{o}	15^{o}	0^{o}	7^{o}	15^{o}

Controlling dimension : Inch.

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