SUMITOMO ELECTRIC

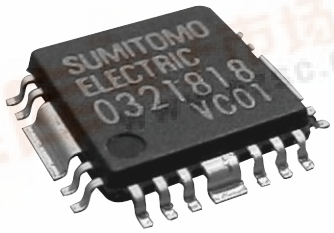
Preliminary

01.08.28

F0321818Q

2 GHz Bandwidth

Limiting Amplifier



♦ *Features*

- -5 V single power supply
- 20 dB typical gain
- 2.0 GHz typical -3 dB cutoff frequency
- On-chip matching to 50 Ω
- 55 mA typical operating current
- Low-cost 20-lead QFP package
- Differential input and output
- Differential ECL compatible input

♦ *Applications*

- Post-amplifier of an optical receiver circuit
  up to 2.5 Gbps
- Logic gate buffer to interface between analog circuit and logic circuit

♦ *Functional Decription*

The F0321818Q is a stable GaAs integrated limiting amplifier for use in a post-amplifier of an optical receiver circuit up to 2.5 Gbps. The F0321818Q typically specifies a small signal gain of 20 dB (Rs=RL=50 Ω) with a 3 dB-cutoff-frequency of 2.0 GHz. It features single +5 V supply operation, excellent VSWR's of 1.1:1, and a typical dissipation current of 55 mA.

The F0321818Q can be also used as interface circuits in sensing systems and measurement instruments. Emitter coupled logic (ECL) or source coupled FET logic (SCFL) circuits are the most popular IC's for high speed digital circuits; the F0321818Q operating under a differential ECL compatible input condition is the best choice as the interface IC to join analog circuits to ECL circuits or conventional GaAs logic IC's.

♦ *Absolute Maximum Ratings*

T_a=25 °C, unless specified

Parameter	Symbol	Value	Unit
Supply Voltage	V_{SS}	V_{DD}-7 to V_{DD}+0.5	V
Supply Current	I_{DD}	80	mA
Input Voltage Swing (AC)	V_{IN+}, V_{IN-}	1	V
Output Voltage	V_{OUT+}, V_{OUT-}	V_{SS}-2.5 to V_{SS}	V
Ambient Operating Temperature	T_a	0 to +70	°C
Strage Temperature	Tstg	-55 to +125	°C

♦ *Recommended Operating Conditions*

V_{DD} = GND

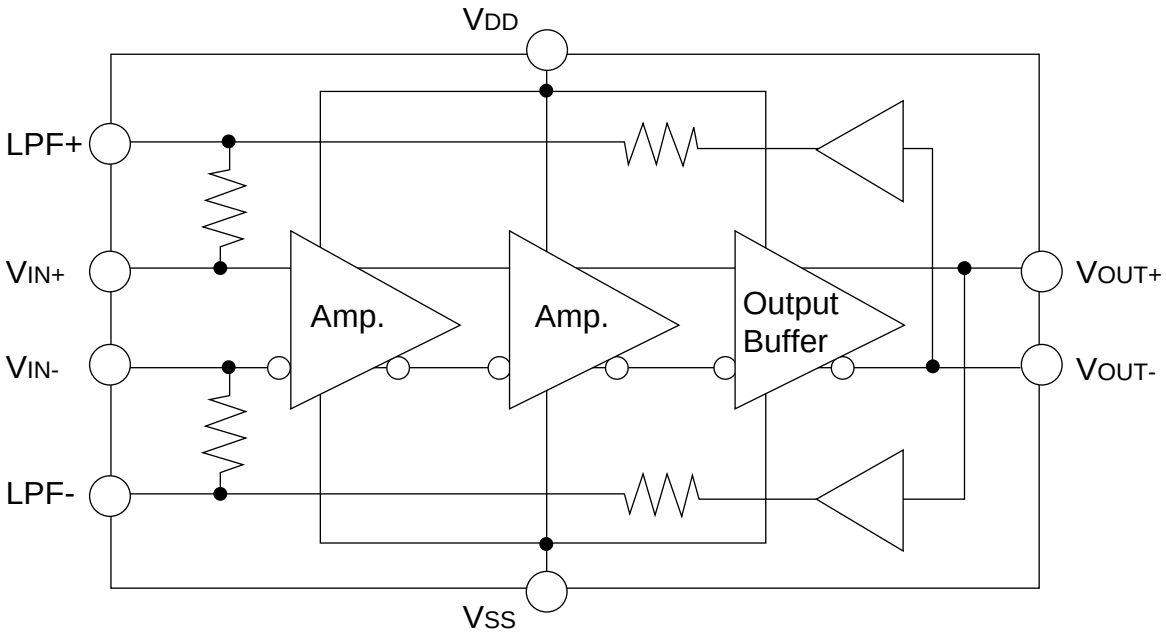
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{SS}	-5.46	-5	-4.75	V
AC Coupled Load	RL	-	50	-	Ω
Ambient Operating Temperature	T_a	0	25	70	°C

♦ *Electrical Characteristics*

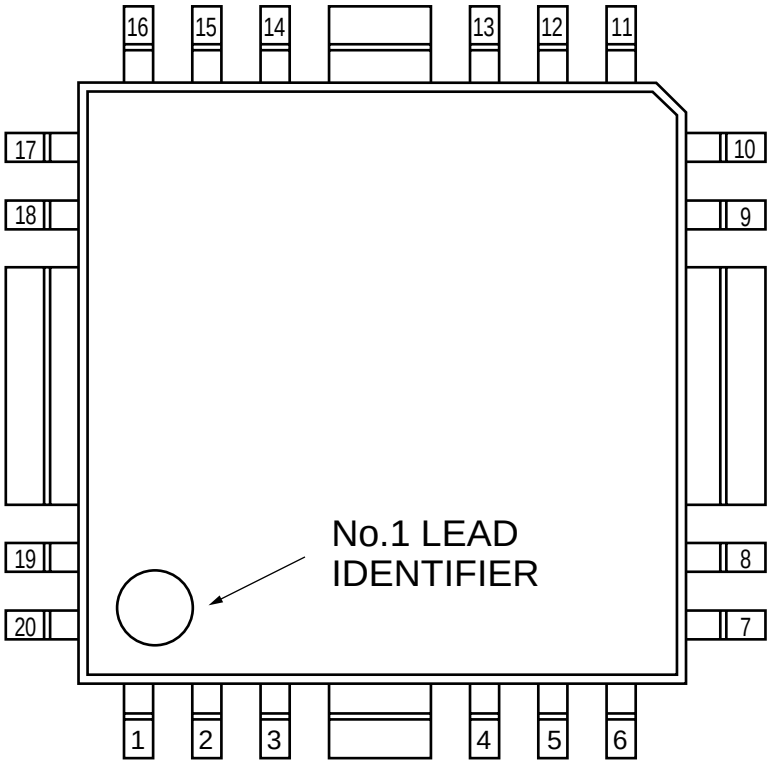
T_a = 25 °C, V_{DD} = 0 V, V_{SS} = -5V, unless specified

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply Current	V_{DD}	Pin=-40dBm	-	55	70	mA
Input Bias Point	V_{IN}		-	-3.5	-	V
Output Bias Point	V_{OUT}		-	-1.5	-	V
VSWR (IN,OUT)	SWR	Pin=-40dBm f=1NHz	-	1.1	1.8	-
Gain	GV	Pin=-40dBm RL-50Ω f=1NHz	18	20	-	dB
-3dB High Frequency Cutoff	Fc	Pin=-40dBm RL-50Ω		2.0	-	GHz
Maximum Output Swing (single output)	Vom	RL-50Ω	0.4	0.6	0.8	V

♦ *Block Diagram*



♦ *Pin Assignments(Top View)*



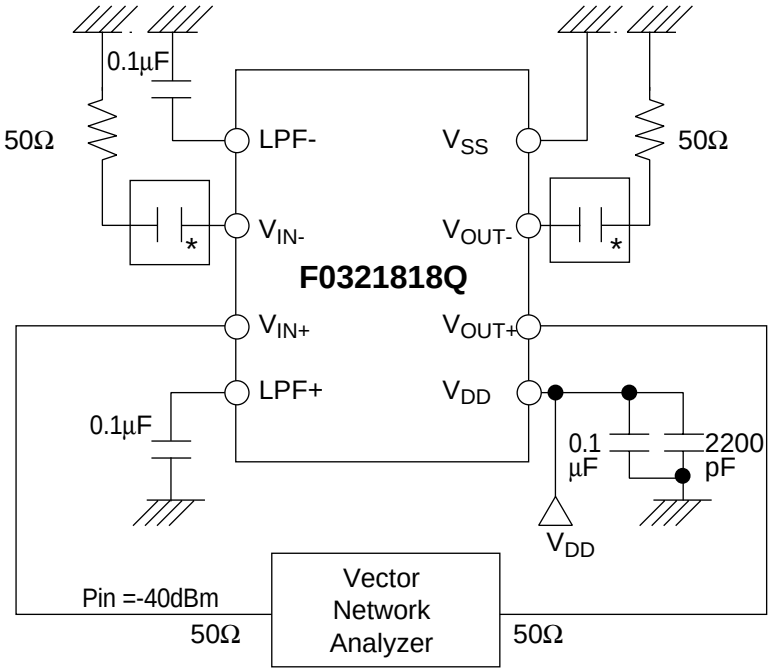
♦ *Pin Descriptions*

1	V_{DD}	Supply Voltage
2	V_{DD}	Supply Voltage
3	V_{OUT}	Output
4	V_{OUT}	Output
5	V_{DD}	Supply Voltage
6	V_{DD}	Supply Voltage
7	V_{SS}	Supply Voltage
8	V_{SS}	Supply Voltage
9	V_{SS}	Supply Voltage
10	V_{SS}	Supply Voltage
11	LPF+	LPF - AC - GND
12	LPF+	LPF - AC - GND
13	V_{IN-}	Input
14	V_{IN+}	Input
15	LPF-	LPF$\pm$ AC - GND
16	LPF-	LPF + AC - GND
17	V_{SS}	Supply Voltage
18	V_{SS}	Supply Voltage
19	V_{SS}	Supply Voltage
20	NC	No Connection

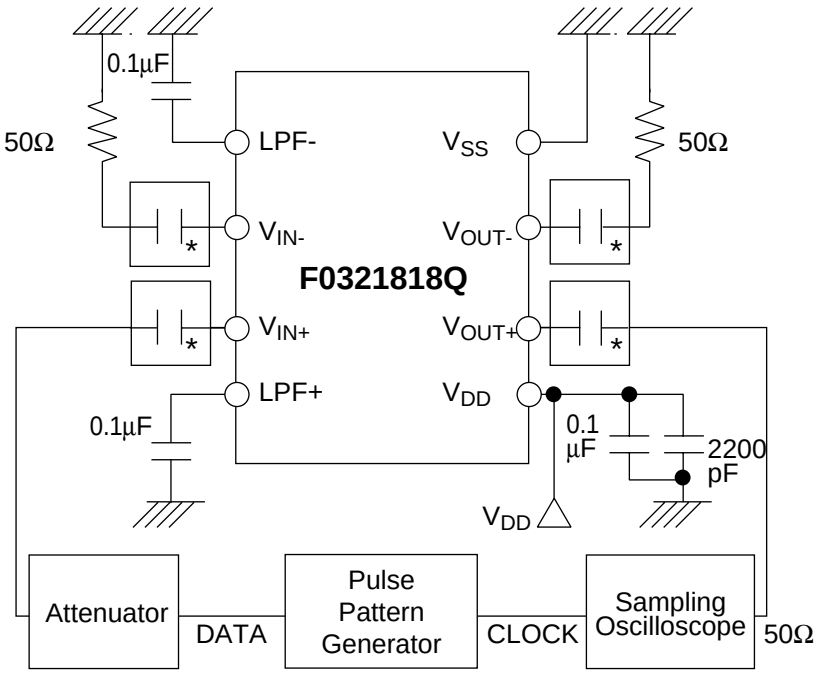
* Other pins are V_{DD}

♦ *Test Circuits*

1)AC Characteristics



2)Limiting Characteristcs

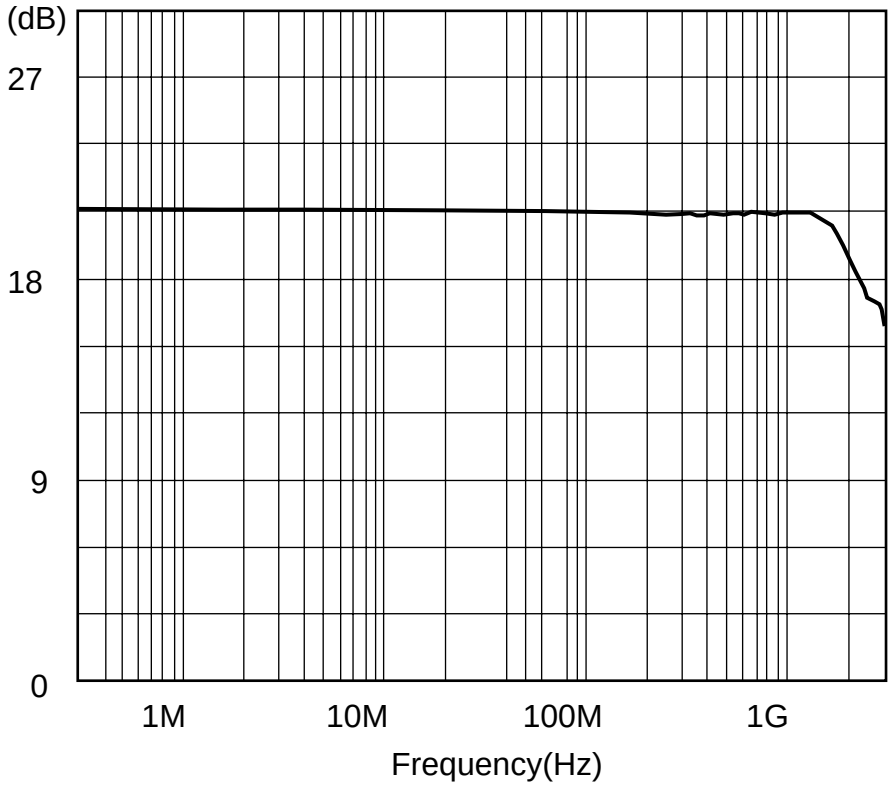


* DC BLOCK(PICOSECIND PULSE LABS, MODEL 5501)

♦ *Typical AC Characteristics*

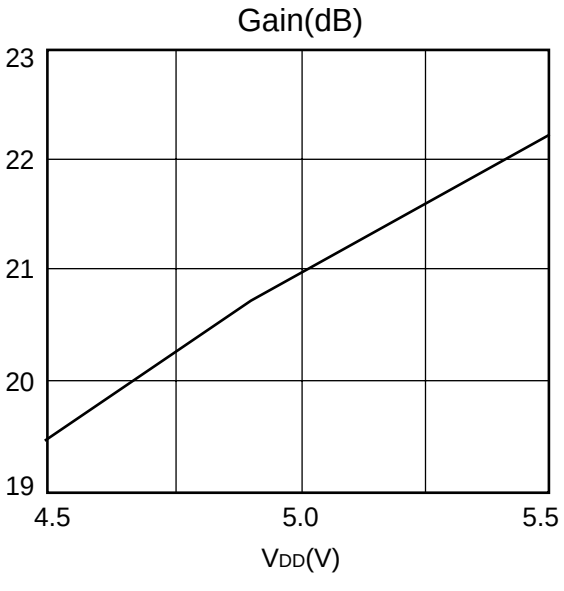
(1) Gain

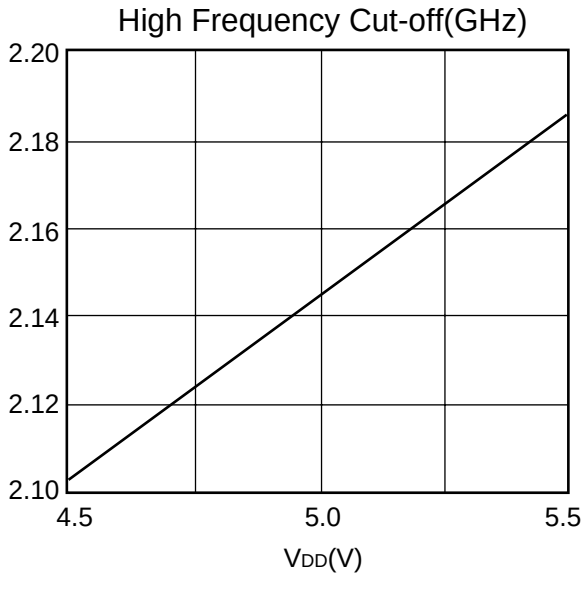
T_a =25 °C, V_{DD} =+5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω,300 kHz-3 GHz



(2) Depemdence of Gain and High Frequency Cutoff on Power Supply Variations

T_a =25 °C, V_{DD} =-5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω,300 kHz-3 GHz



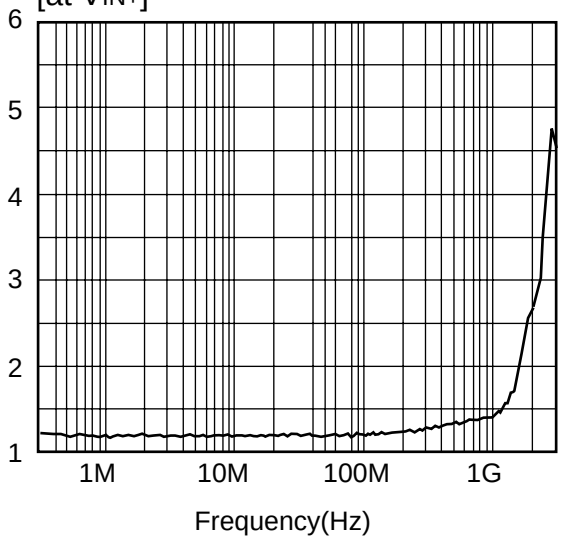


♦ *Typical AC Characteristics*

(3) VSWR's

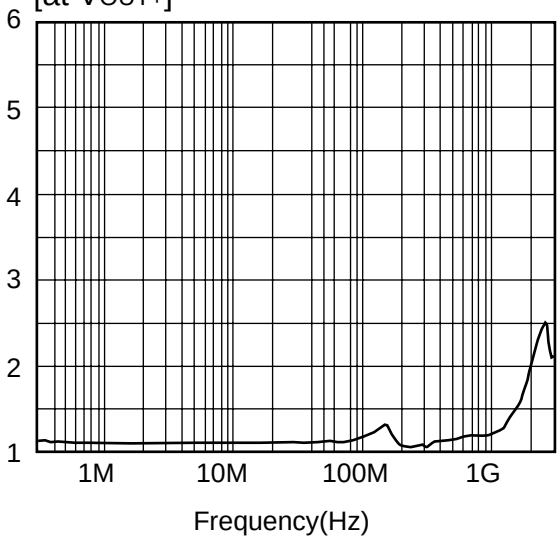
T_a =25 °C, V_{DD} =+5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω, 300 kHz - 3 GHz

[at V_{IN+}]



*Almost same characteristics is exhibited at V_{IN-}

[at V_{OUT+}]

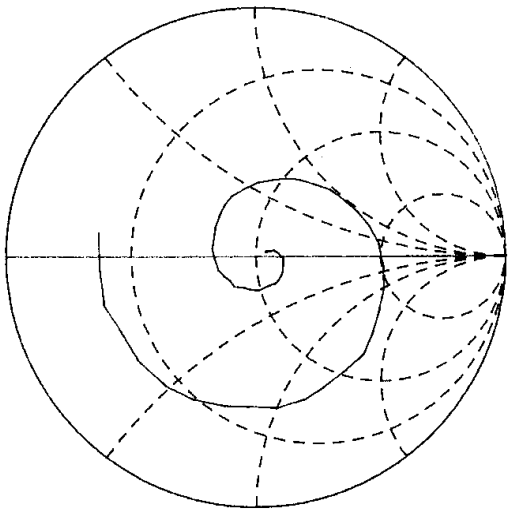


*Almost same characteristics is exhibited at V_{OUT-}

(4) S parameters on Smith Chart

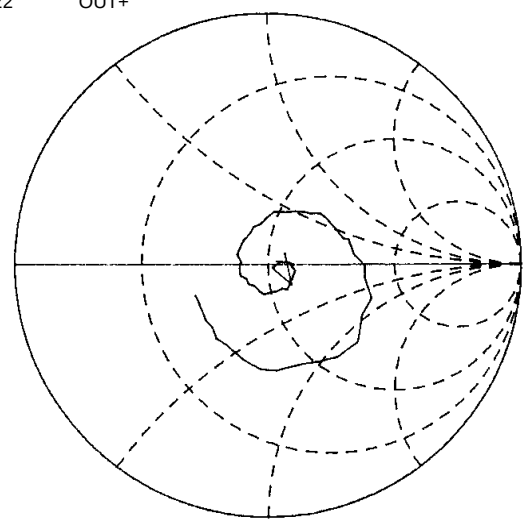
T_a =25 °C, V_{DD} =+5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω

S_{11} at V_{IN+}



START 100MHz STOP 3GHz

S_{22} at V_{OUT+}



START 100MHz STOP 3GHz

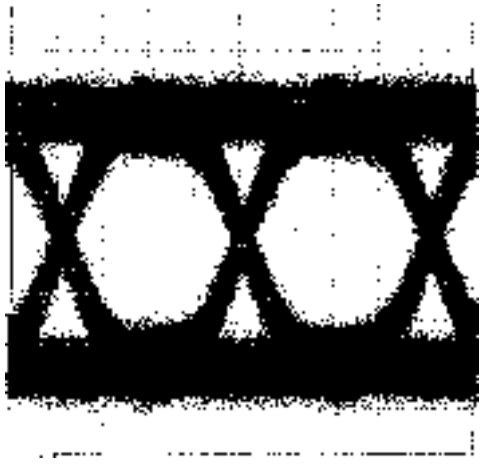
♦ *Typical Limiting Characteristics*

(1) Eye diagrams for 2.5Gbps NRZ Pseudo-random Data Responce

2^{23}-1, T_a = 25 °C, V_{DD} =5 V, V_{SS} =GND, RL =50 Ω

(a) V_{IN+} = 5mVp-p

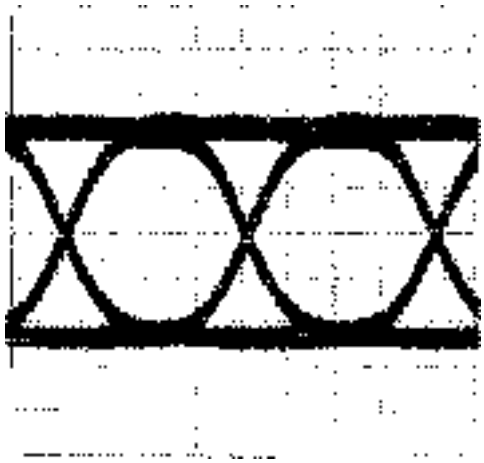
10mV/div



100psec/div

(b) V_{IN+} = 50mVp-p

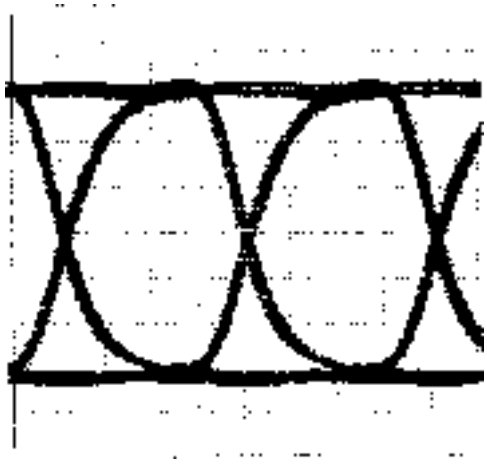
100mV/div



100psec/div

(c) V_{IN+} = 500mVp-p

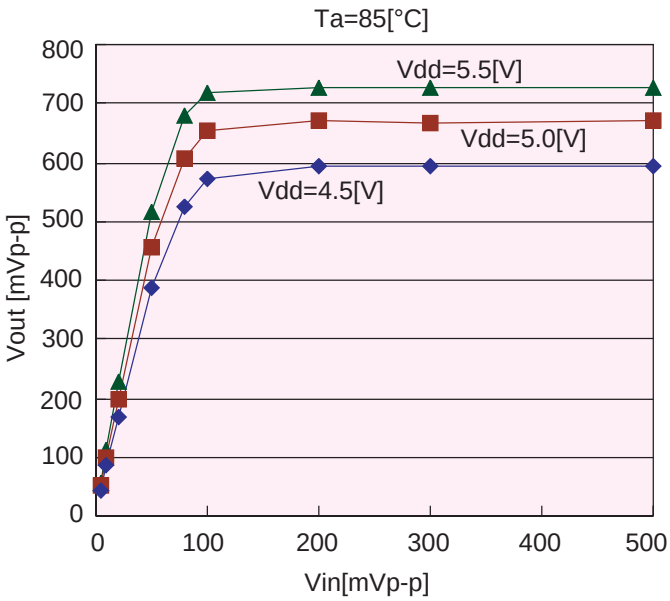
100mV/div

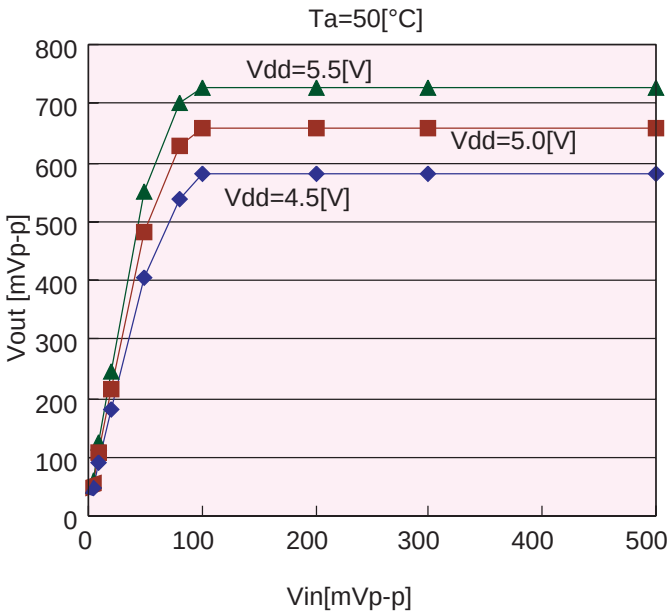


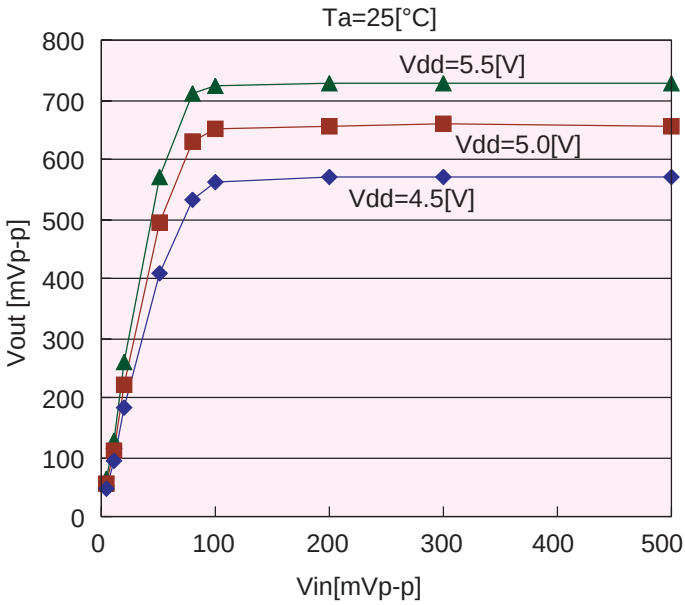
100psec/div

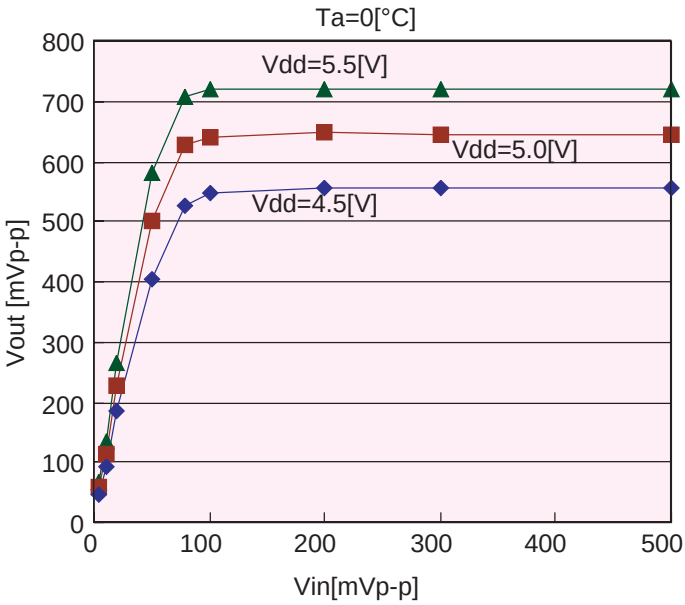
(2) Output amplitude vs Input amplitude

f=2 GHz, PRBS=2^{23}-1 ,RL=50 Ω









♦ *General Discription*

A post-amplifier is positioned between a pre-amplifier (an amplifier for a faint photo-current from PIN photo diode) and a decision circuit (a circuit to discriminate the logic level of the received signal) , enlarging the output signal from the pre-amplifier to a higher level to discriminate the logic level. The input signal amplitude of the post-amplifier, meaning the output signal of the pre-amplifier, varies widely, because the optical signal power received by the PIN photo diode depends on the length of the transmission line. Therefore, the post-amplifier should function to output an almost constant signal level under widely varying input voltage. This is called a limiting function, and the F0321818Q provides excellent limiting characteristics. As shown in the data sheet, the increase of only 200 mV (400 mV→600 mV) in the output voltage can be observed even if the 2.5 Gps input signal varies widely from 50 mV to 500 mV.

Wide use analog IC's having satisfactory limiting functions as described above can not be found except for the F0321818Q. Customized IC's for each application or a circuit designed by discrete transistors are believed to have been developed.

♦ *Port Matching*

Input/output VSWR's of the F0321818Q are well-designed for 50 Ω, typically showing excellent VSWR's of 1.1:1. Therefore, the F0321818Q can be applied for 50 Ω systems with no external parts. Furthermore, the fine VSWR characteristics provide stable operation even for cascade connections of two IC's for a higher gain. The excellent VSWR characteristics of the F0321818Q gives full play in a clock recovery system using SAW filters, because the impedance mismatch has a significant effect on the quality of the recovered clock signal.

♦ *Gain Consideration*

The F0321818Q has a small signal gain of 20 dB. A too high gain can be harmful because of parasitic oscillation. If a slightly higher gain is needed, a 6 dB higher gain of 26 dB can be obtained by a high impedance termination instead of a 50 Ω load. A double gain can be achieved by simple cascade connection if a still higher gain is required.

♦ *Noise Performance*

The F0321818Q based on the GaAs FET fabrication process intrinsically has more excellent low-noise characteristics compared with IC's based on the silicon bipolar process. Many transmission systems often demand superior signal-to-noise ratio; the F0321818Q is the best choice for such applications.

The differential circuit configuration in the input and output enable a complete differential operation to reduce common mode noise: simple single ended input and output operation is also available.

♦ *LPF+ & LPF-*

The F0321818Q has two terminals, LPF+ and LPF-, for AC ground. These terminals are connected to ground by a capacitor. The time constant of the feedback loop in the F0321818Q depends on the capacitor, giving the lower frequency cutoff of the circuit by the large capacitor. A 0.1micro farad is employed for conventional applications.

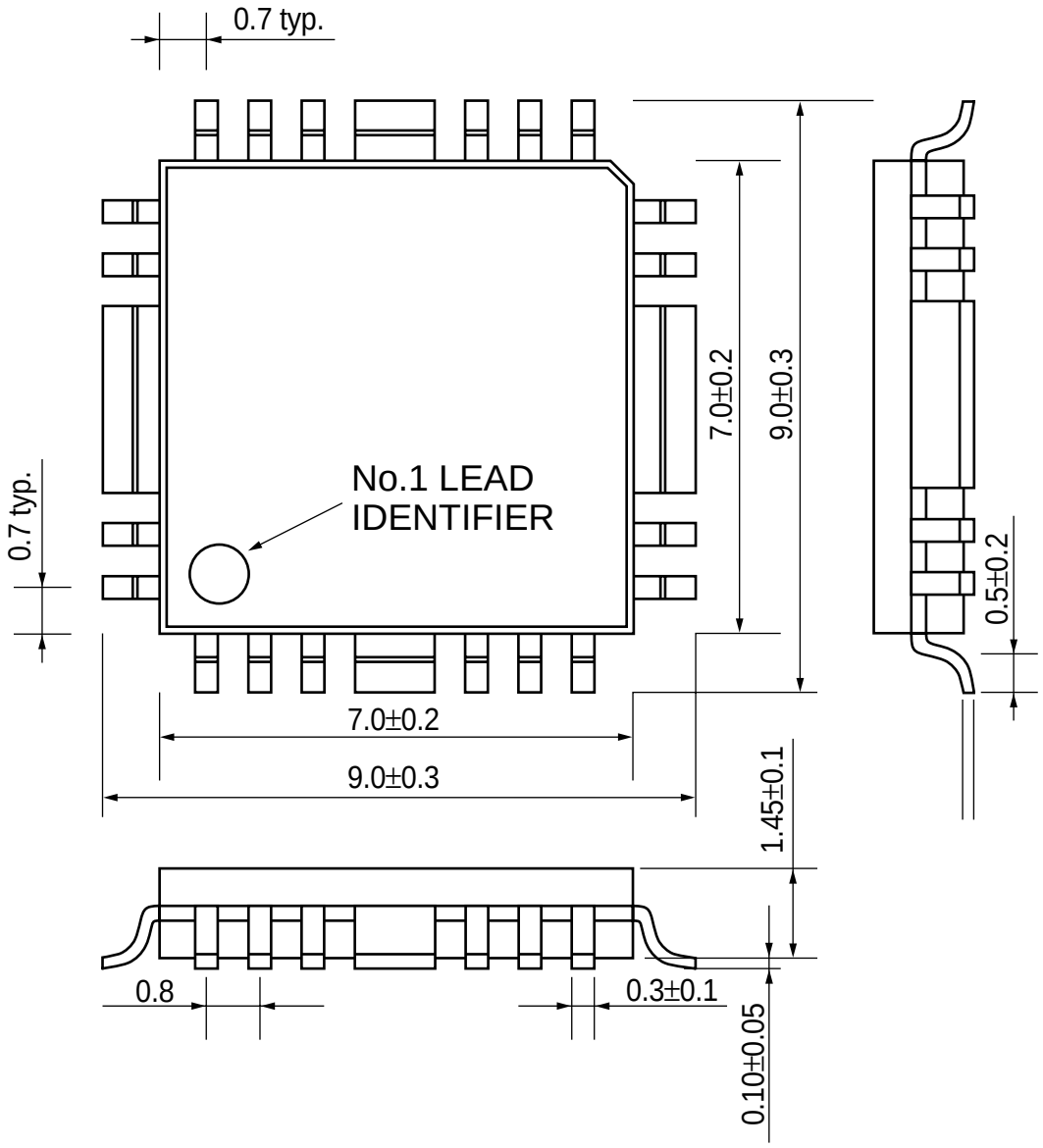
♦ *Packaging*

The F0321818Q is in an 20-lead quadruplel flat package (QFP) about 350 mil square with the lead pitch of 32 mil, achieving miniaturization and low cost. It is originally developed by SEI to improve RF performance and heat radiation. Comparing with the SOP, the ground potential steadier at microwave frequency range and the thermal receptivity is smaller due to the metal based bottom structure made from Cu with a high thermal conductivity. The intrinsic broad band performance of the F0321818Q can not be brought out by the standard SOP and LCC, because it is difficult to overcome impedance mismatch at high frequency around 2 GHz. Therefore, SEI's superior package technology enable to achieve the excellent wide band limiting performance of the F0321818Q.

♦ *Precautions*

Owing to their small dimensions, the GaAs FET's from which the F0321818M is designed are easily damaged or destroyed if subjected to large transient voltages. Such transients can be generated by power supplies when switched on if not properly decoupled. It is also possible to induce spikes from static-electricity-charged operations or ungrounded equipment.

♦ *Package Drawings*



All Dimensions shown in millimeters