

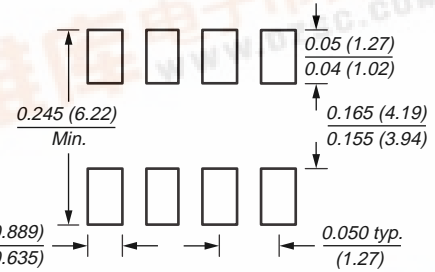
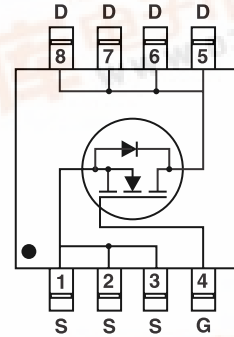
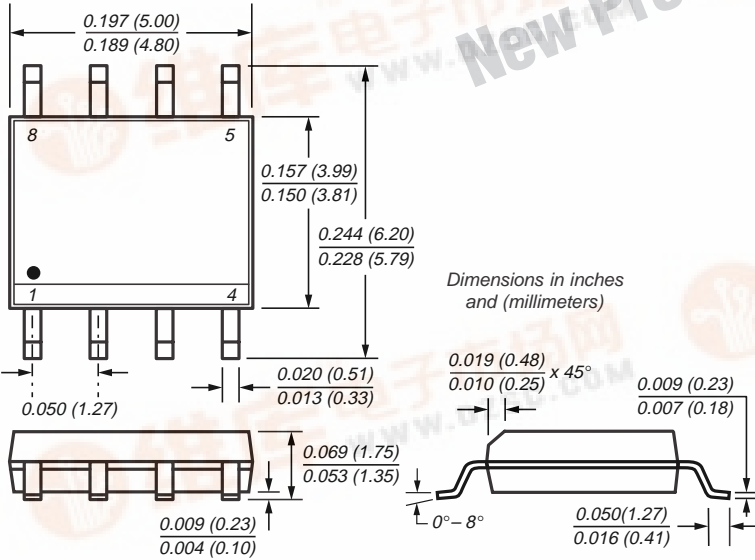


N-Channel Enhancement-Mode MOSFET

V_{DS} 60V R_{DS(ON)} 24mΩ I_D 7.5A

TRENCH GENFET®

SO-8



Mounting Pad Layout

Mechanical Data

- Case:** SO-8 molded plastic body
- Terminals:** Leads solderable per MIL-STD-750, Method 2026
- High temperature soldering guaranteed:** 250°C/10 seconds at terminals
- Mounting Position:** Any
- Weight:** 0.5g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Low Voltage DC/DC Converters
- Fast Switching for High Efficiency

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	±20	
Continuous Drain Current ⁽¹⁾	I _D	7.5	A
Pulsed Drain Current	I _{DM}	50	
Maximum Power Dissipation ⁽¹⁾	T _A = 25°C T _A = 70°C	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance ⁽¹⁾	R _{θJA}	50	°C/W

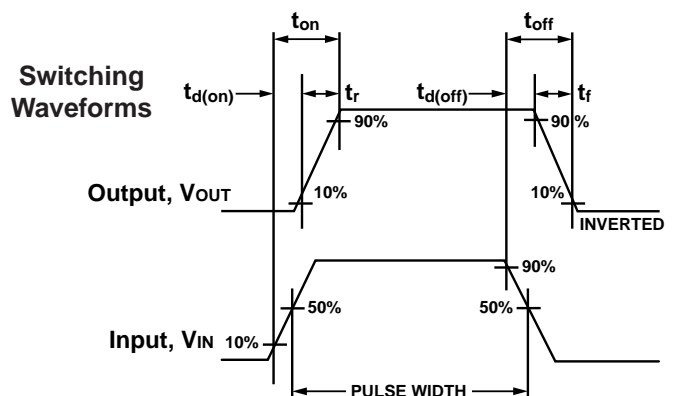
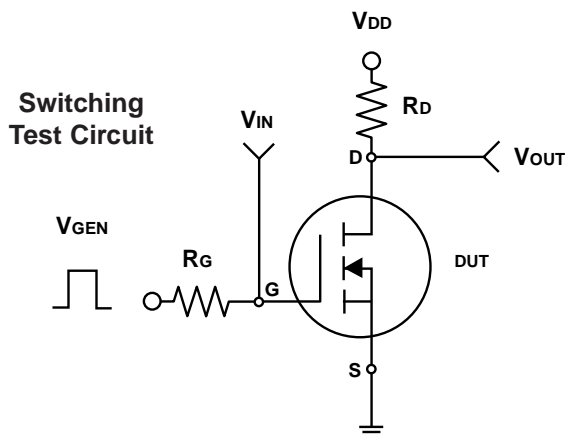
Note: (1) Surface Mounted on FR4 Board, t ≤ 10s

N-Channel Enhancement-Mode MOSFET

Electrical Characteristics (T_J = 25°C unless otherwise noted)

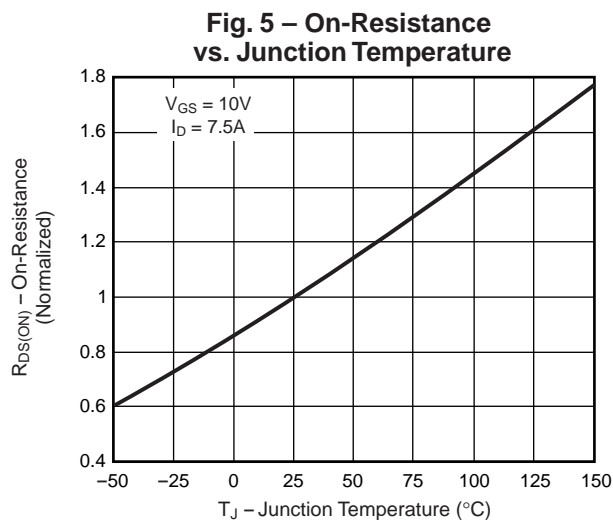
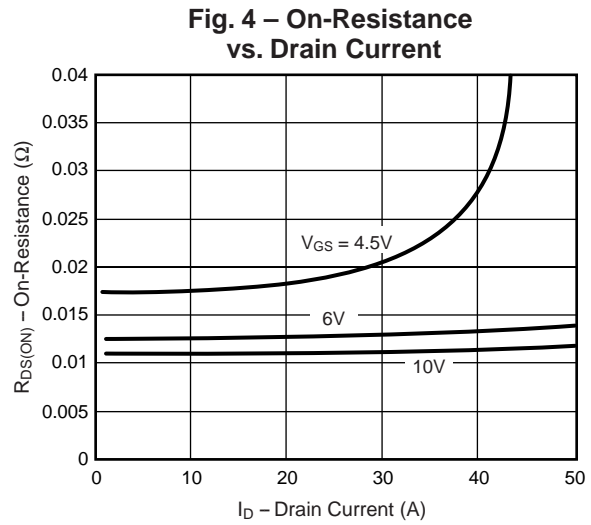
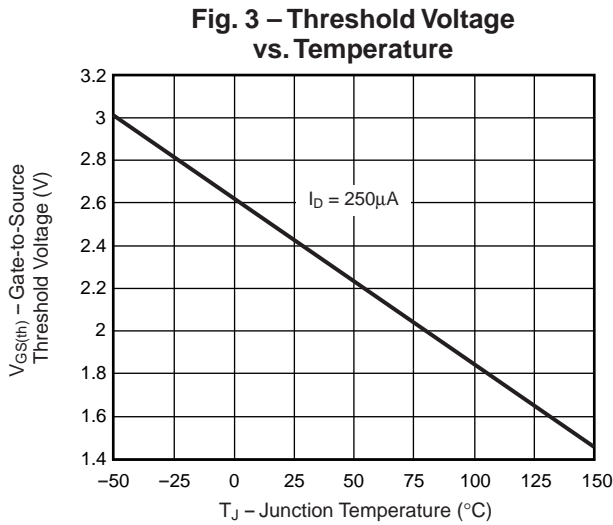
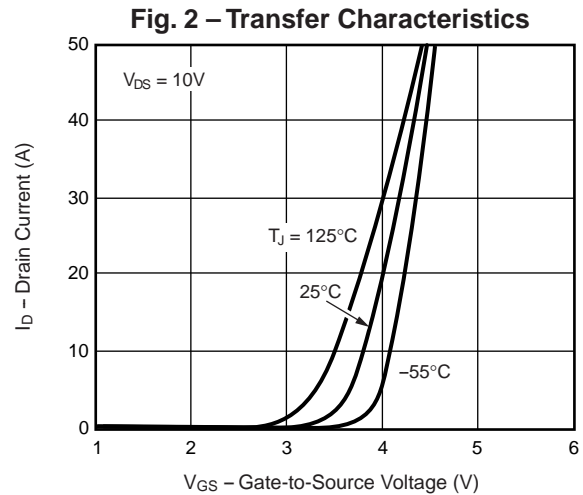
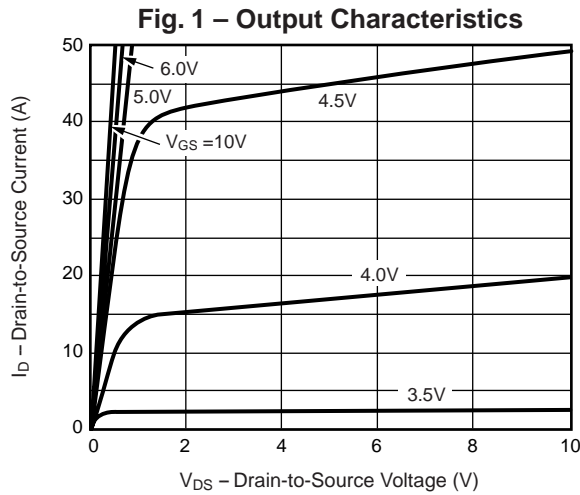
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	60	–	–	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	–	–	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	–	–	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V	–	–	1.0	μA
On-State Drain Current ⁽²⁾	I _{D(on)}	V _{DS} ≥ 5V, V _{GS} = 10V	20	–	–	A
Drain-Source On-State Resistance ⁽²⁾	R _{DS(on)}	V _{GS} = 10V, I _D = 7.5A	–	12	24	mΩ
		V _{GS} = 6.0V, I _D = 6.5A	–	14	30	
Forward Transconductance ⁽²⁾	g _{fs}	V _{DS} = 15V, I _D = 7.5A	–	36	–	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 30V, V _{GS} = 10V I _D = 7.5A	–	65	91	nC
Gate-Source Charge	Q _{gs}		–	12	–	
Gate-Drain Charge	Q _{gd}		–	14	–	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30V, R _L = 30Ω I _D ≈ 1A, V _{GEN} = 10V R _G = 6Ω	–	17	30	ns
Rise Time	t _r		–	13	20	
Turn-Off Delay Time	t _{d(off)}		–	78	117	
Fall Time	t _f		–	31	40	
Input Capacitance	C _{iss}	V _{GS} = 0V	–	3147	–	pF
Output Capacitance	C _{oss}	V _{DS} = 30V	–	283	–	
Reverse Transfer Capacitance	C _{rss}	f = 1.0MHz	–	140	–	
Source-Drain Diode						
Diode Forward Voltage	V _{SD}	I _S = 2.1A, V _{GS} = 0V	–	0.71	1.2	V
Max. Diode Forward Current	I _S		–	–	2.1	A

Notes: (1) Surface Mounted on FR4 Board, t ≤ 10s
(2) Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%



N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)



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Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

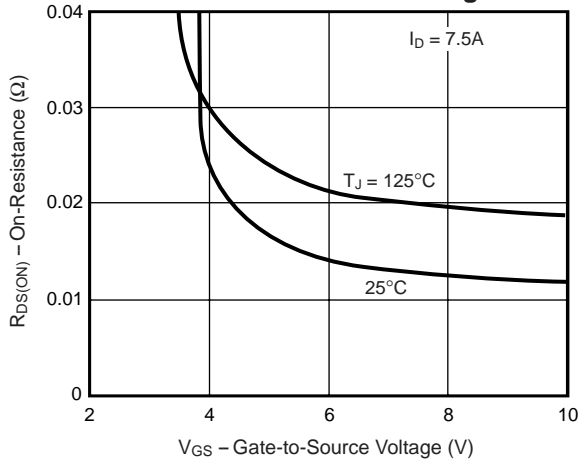


Fig. 7 – Gate Charge

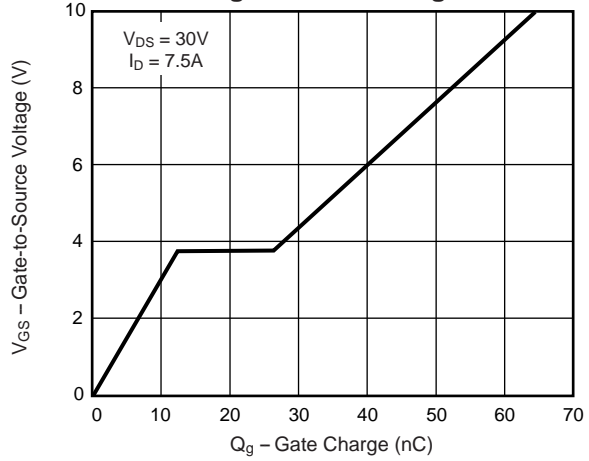


Fig. 8 – Capacitance

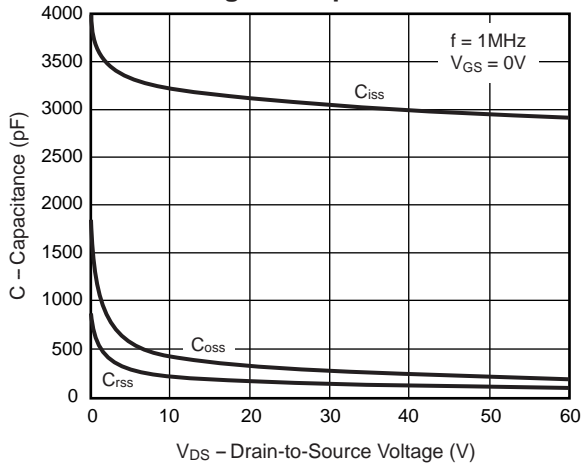
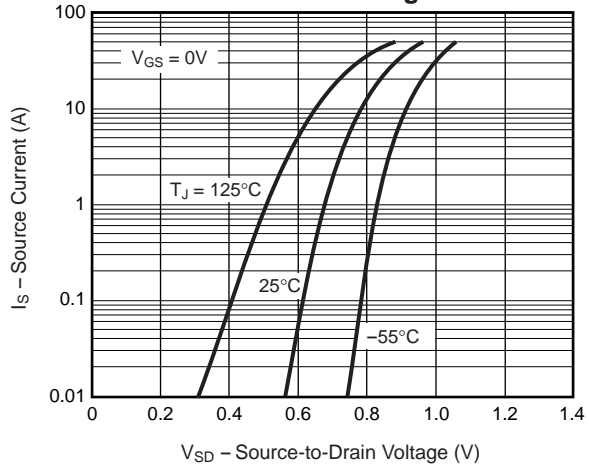


Fig. 9 – Source-Drain Diode Forward Voltage



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Fig. 10 – Breakdown Voltage vs. Junction Temperature

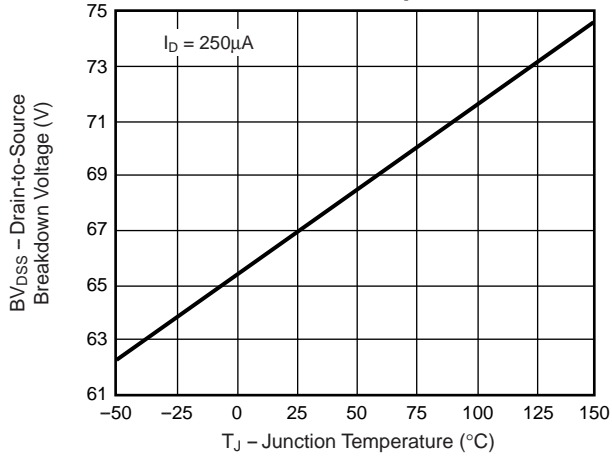


Fig. 11 – Transient Thermal Impedance

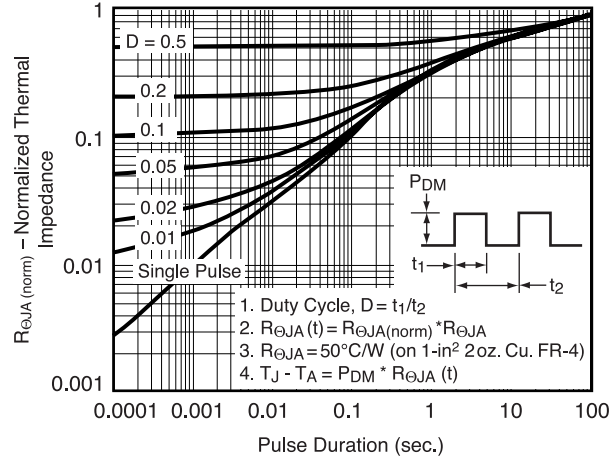


Fig. 12 – Power vs. Pulse Duration

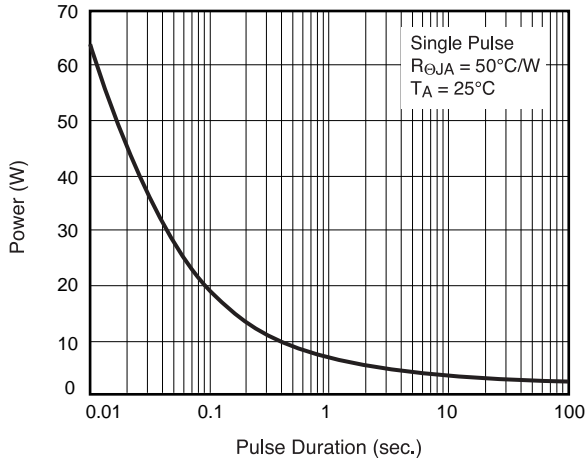


Fig. 13 – Maximum Safe Operating Area

