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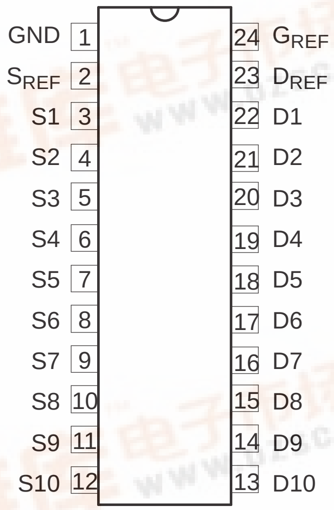
GTL2010
10-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR

SCDS221–SEPTEMBER 2006

FEATURES

- **Provides Bidirectional Voltage Translation With No Direction Control Required**
- **Allows Voltage Level Translation From 1 V up to 5 V**
- **Provides Direct Interface With GTL, GTL+, LVTTL/TTL, and 5-V CMOS Levels**
- **Low On-State Resistance Between Input and Output Pins (Sn/Dn)**
- **Supports Hot Insertion**
- **No Power Supply Required – Will Not Latch Up**
- **5-V-Tolerant Inputs**
- **Low Standby Current**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-4)**
  - **1000-V Charged-Device Model (C101)**

PW PACKAGE
(TOP VIEW)



APPLICATIONS

- **Bidirectional or Unidirectional Applications Requiring Voltage-Level Translation From Any Voltage (1 V to 5 V) to Any Voltage (1 V to 5 V)**
- **Low Voltage Processor I^2C Port Translation to 3.3-V and/or 5-V I^2C Bus Signal Levels**
- **GTL/GTL+ Translation to LVTTL/TTL Signal Levels**

DESCRIPTION/ORDERING INFORMATION

The GTL2010 provides ten NMOS pass transistors (Sn and Dn) with a common gate (G_{REF}) and a reference transistor (S_{REF} and D_{REF}). The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. With no direction control pin required, the device allows bidirectional voltage translations any voltage (1 V to 5 V) to any voltage (1 V to 5 V).

When the Sn or Dn port is LOW, the clamp is in the ON state and a low-resistance connection exists between the Sn and Dn ports. Assuming the higher voltage is on the Dn port, when the Dn port is HIGH, the voltage on the Sn port is limited to the voltage set by the reference transistor (S_{REF}). When the Sn port is HIGH, the Dn port is pulled to V_{CC} by the pullup resistors.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

All transistors in the GTL2010 have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This offers superior matching over discrete transistor voltage-translation solutions where the fabrication of the transistors is not symmetrical. With all transistors being identical, the reference transistor (S_{REF}/D_{REF}) can be located on any of the other ten matched Sn/Dn transistors, allowing for easier board layout. The translator transistors with integrated ESD circuitry provides excellent ESD protection.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tape and reel	SN74GTL2010PWR	GK2010

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	GND	Ground (0 V)
2	S_{REF}	Source of reference transistor
3–12	Sn	Ports S1–10
13–22	Dn	Ports D10–D1
23	D_{REF}	Drain of reference transistor
24	G_{REF}	Gate of reference transistor

FUNCTION TABLES(1)

HIGH-to-LOW Translation (Assuming Dn is at the Higher Voltage Level)

G_{REF}(2)	D_{REF}	S_{REF}	INPUTS D10–D1	OUTPUTS S10–S1	TRANSISTOR
H	H	0 V	X	X	Off
H	H	V_{TT}(3)	H	V_{TT}(4)	On
H	H	V_{TT}	L	L(5)	On
L	L	0 – V_{TT}	X	X	Off

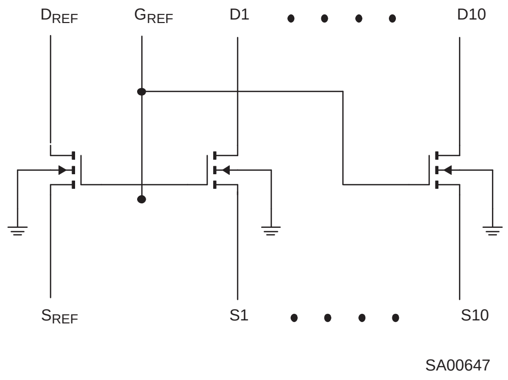
(1) H = HIGH voltage level, L = LOW voltage level, X = don't care
(2) G_{REF} should be at least 1.5 V higher than S_{REF} for best translator operation.
(3) V_{TT} is equal to the S_{REF} voltage.
(4) Sn is not pulled up or pulled down.
(5) Sn follows the Dn input LOW.

LOW-to-HIGH Translation (Assuming Dn is at the Higher Voltage Level)(1)

G_{REF}(2)	D_{REF}	S_{REF}	INPUTS D10–D1	OUTPUTS S10–S1	TRANSISTOR
H	H	0 V	X	X	Off
H	H	V_{TT}(3)	V_{TT}	H(4)	Nearly off
H	H	V_{TT}	L	L(5)	On
L	L	0 – V_{TT}	X	X	Off

(1) H = HIGH voltage level, L = LOW voltage level, X = don't care
(2) G_{REF} should be at least 1.5 V higher than S_{REF} for best translator operation.
(3) V_{TT} is equal to the S_{REF} voltage.
(4) Dn is pulled up to V_{CC} through an external resistor.
(5) Dn follows the Sn input LOW.

CLAMP SCHEMATIC



Absolute Maximum Ratings(1)(2)(3)

			MIN	MAX	UNIT
V_{SREF}	DC source reference voltage		–0.5	7	V
V_{DREF}	DC drain reference voltage		–0.5	7	V
V_{GREF}	DC gate reference voltage		–0.5	7	V
V_{Sn}	DC voltage port Sn		–0.5	7	V
V_{Dn}	DC voltage port Dn		–0.5	7	V
I_{REFK}	DC diode current on reference pins	$V_I < 0$ V		–50	mA
I_{SK}	DC diode current port Sn	$V_I < 0$ V		–50	mA
I_{DK}	DC diode current port Dn	$V_I < 0$ V		–50	mA
I_{MAX}	DC clamp current per channel	Channel in ON state		±128	mA
θ_{JA}	Package thermal impedance			88	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage (Sn, Dn)	0	5.5	V
V_{SREF}	DC source reference voltage(1)	0	5.5	V
V_{DREF}	DC drain reference voltage	0	5.5	V
V_{GREF}	DC gate reference voltage	0	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_{amb}	Operating ambient temperature range (in free air)	–40	85	°C

(1) $V_{SREF} = V_{DREF} – 1.5$ V for best results in level-shifting applications.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{OL}	Low-level output voltage	V_{DD} = 3 V, V_{SREF} = 1.365 V, V_{Sn} or V_{Dn} = 0.175 V, I_{clamp} = 15.2 mA				260	350	mV
V_{IK}	Input clamp voltage	I_I = –18 mA,	V_{GREF} = 0 V				–1.2	V
I_{IH}	Gate input leakage	V_I = 5 V,	V_{GREF} = 0 V				5	µA
$C_{I(GREF)}$	Gate capacitance	V_I = 3 V or 0 V				56		pF
$C_{IO(OFF)}$	OFF capacitance	V_O = 3 V or 0 V,	V_{GREF} = 0 V			7.4		pF
$C_{IO(ON)}$	ON capacitance	V_O = 3 V or 0 V,	V_{GREF} = 3 V			18.6		pF
r_{on}[2]	ON-state resistance	V_I = 0 V	V_{GREF} = 4.5 V	I_O = 64 mA		3.5	5	Ω
			V_{GREF} = 3 V			4.4	7	
			V_{GREF} = 2.3 V			5.5	9	
			V_{GREF} = 1.5 V			67	105	
			V_{GREF} = 1.5 V,	I_O = 30 mA		9	15	
		V_I = 2.4 V	V_{GREF} = 4.5 V	I_O = 15 mA		7	10	
			V_{GREF} = 3 V			58	80	
		V_I = 1.7 V	V_{GREF} = 2.3 V			50	70	

(1) All typical values are measured at T_{amb} = 25°C.
(2) Measured by the voltage drop between the Sn and the Dn terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (Sn or Dn) terminals.

AC Characteristics for Translator-Type Applications[1]

V_{REF} = 1.365 V to 1.635 V, V_{DD1} = 3 V to 3.6 V, V_{DD2} = 2.36 V to 2.64 V, GND = 0 V, $t_r = t_f \le 3$ ns, T_{amb} = –40°C to 85°C (see Figure 5)

PARAMETER		MIN	TYP[2]	MAX	UNIT
t_{PLH}[3]	Propagation delay (Sn to Dn, Dn to Sn)	0.5	1.5	5.5	ns

(1) $C_{ON(max)}$ of 30 pF and a $C_{OFF(max)}$ of 15 pF is specified by design.
(2) All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_{amb} = 25°C.
(3) Propagation delay specified by characterization.

AC Waveforms
Vm = 1.5 V, V_{IN} = GND to 3 V

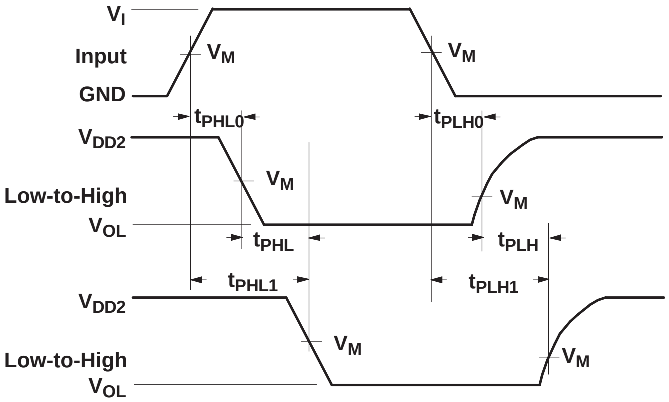


Figure 1. Input (Sn) to Output (Dn) Propagation Delays

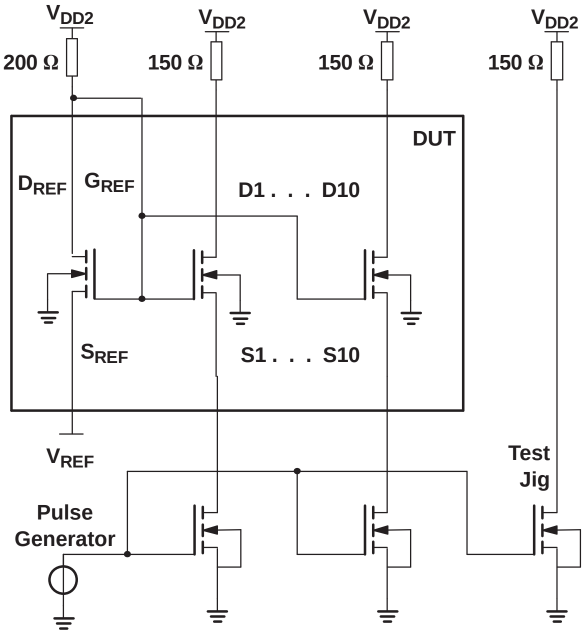


Figure 2. Load Circuit

AC Characteristics for CBT-Type Applications

GND = 0 V, t_R, C_L = 50 pF, G_{REF} = 5 V ± 0.5 V, T_{amb} = –40°C to 85°C

PARAMETER		MIN	MAX	UNIT
t_{pd}	Propagation delay(1)		250	ps

(1) This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

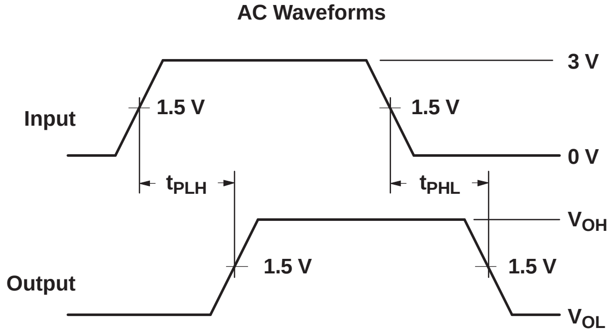
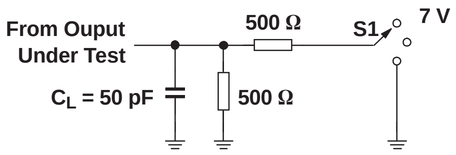


Figure 3. Input (Sn) to Output (Dn) Propagation Delays



Load Circuit

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

C_L = Load capacitance, includes jig and probe capacitance
(see *AC Characteristics* for value).

Figure 4. Load Circuit

APPLICATION INFORMATION

Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the G_{REF} input must be connected to D_{REF} and both pins pulled to HIGH-side V_{CC} through a pullup resistor (typically 200 kΩ). A filter capacitor on D_{REF} is recommended. The processor output can be totem pole or open drain (pullup resistors) and the chipset output can be totem pole or open drain (pullup resistors are required to pull the Dn outputs to V_{CC}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-statable, and the outputs must be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open drain, no direction control is needed. The opposite side of the reference transistor (S_{REF}) is connected to the processor core power-supply voltage. When D_{REF} is connected through a 200-kΩ resistor to a 3.3-V to 5.5-V V_{CC} supply and S_{REF} is set between 1 V to V_{CC} 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF}, and the output of each Dn has a maximum output voltage equal to V_{CC}.

APPLICATION INFORMATION (continued)

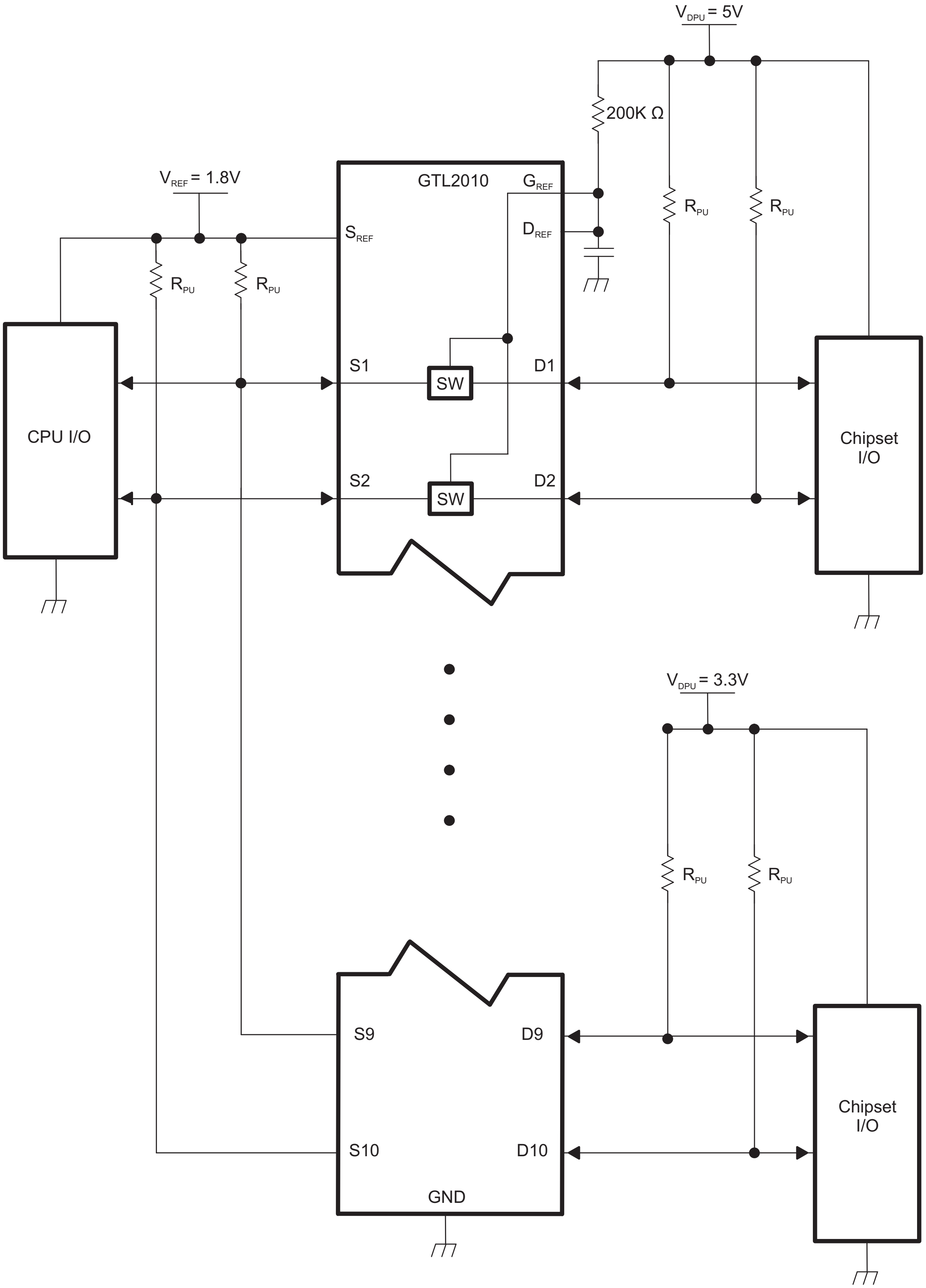


Figure 5. Bidirectional Translation to Multiple Higher Voltage Levels (Such as an I^2C or SMBus Applications)

APPLICATION INFORMATION (continued)

Unidirectional Down Translation

For unidirectional clamping (higher voltage to lower voltage), the G_{REF} input must be connected to D_{REF} and both pins pulled to the higher-side V_{CC} through a pullup resistor (typically 200 kΩ). A filter capacitor on D_{REF} is recommended. Pullup resistors are required if the chipset I/Os are open drain. The opposite side of the reference transistor (S_{REF}) is connected to the processor core power-supply voltage. When D_{REF} is connected through a 200-kΩ resistor to a 3.3-V to 5.5-V V_{CC} supply and S_{REF} is set between 1 V to V_{CC} – 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF}.

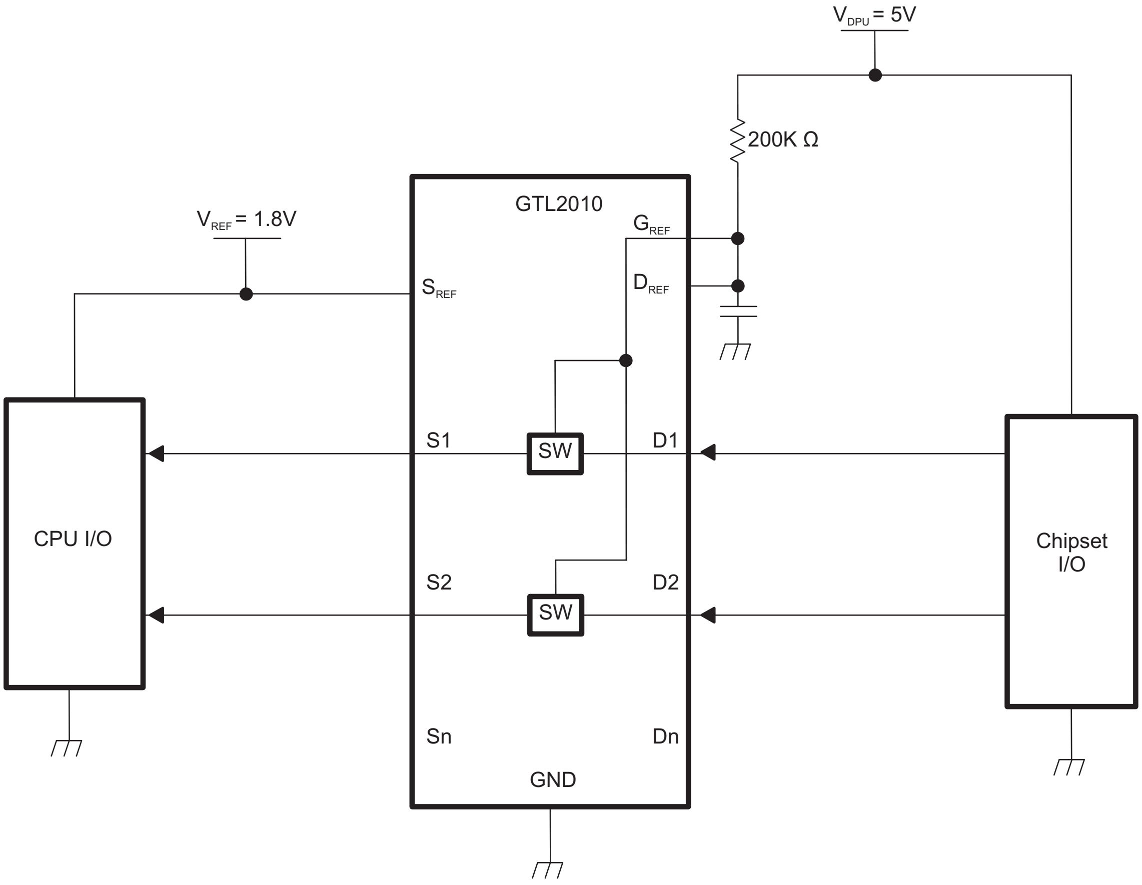


Figure 6. Unidirectional Down Translation to Protect Low-Voltage Processor Pins

APPLICATION INFORMATION (continued)

Unidirectional Up Translation

For unidirectional up translation (lower voltage to higher voltage), the reference transistor is connected the same as for a down translation. A pullup resistor is required on the higher voltage side (Dn or Sn) to get the full HIGH level, since the GTL device only passes the reference source (S_{REF}) voltage as a HIGH when doing an up translation. The driver on the lower voltage side only needs pullup resistors if it is open drain.

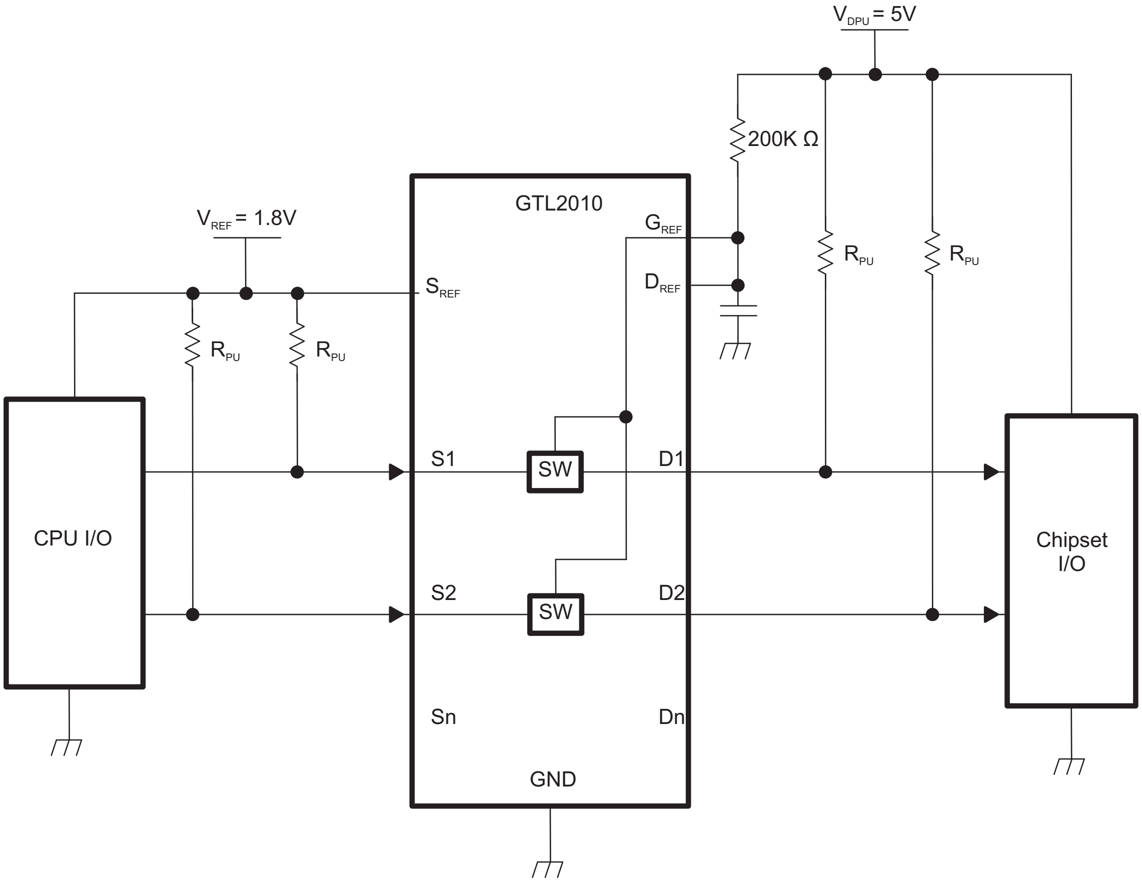


Figure 7. Unidirectional Up Translation to Higher-Voltage Chipsets

APPLICATION INFORMATION (continued)

Sizing Pullup Resistor

The pullup resistor value should limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$\text{Resistor value } (\Omega) = \frac{\text{Pullup voltage (V)} - 0.35\text{ V}}{0.015\text{ A}}$$

Table 1 shows resistor values for various reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column, or a larger value, should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the GTL device at 0.175 V, although the 15 mA only applies to current flowing through the GTL2010.

Table 1. Pullup Resistor Values(1)(2)(3)

VOLTAGE	PULLUP RESISTOR VALUE (Ω)					
	15 mA		10 mA		3 mA	
	NOMINAL	+10%	NOMINAL	+10%	NOMINAL	+10%
5.0 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

PACKAGE OPTION ADDENDUM

6-Dec-2006

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74GTL2010PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2010PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2010PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74GTL2010PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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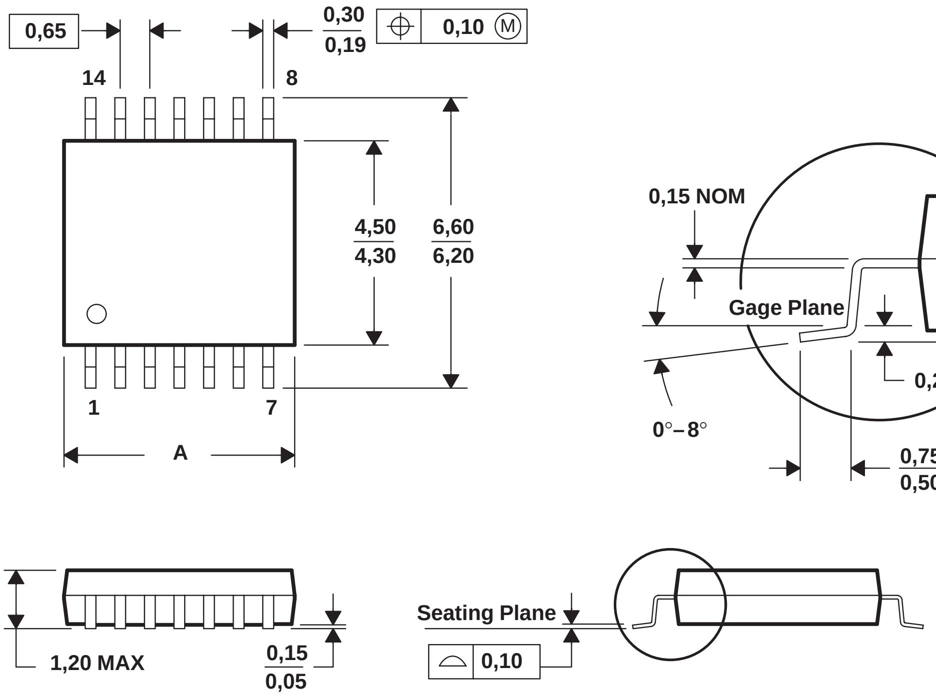
PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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