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GENNUM CORPORATION

GENLINX™ II GS9023A
Embedded Audio CODEC

DATA SHEET

KEY FEATURES

- **single chip embedded audio solution**
- **operates as an embedded audio multiplexer or demultiplexer**
- **full support for 48kHz synchronous 20/24 bit audio**
- **4 channels of audio per GS9023A**
- **cascadable architecture supports additional audio channels**
- **multiplexes and demultiplexes arbitrary ANC data packets**
- **support for 143, 177, 270, 360 and 540 Mb/s video standards**
- **full processing of audio parity, channel status and user data**
- **multiplexes and demultiplexes audio control packets**
- **EDH generation and insertion when in Multiplex Mode**
- **3.3V core with 3.3V or 5V I/O (requires 5V supply)**
- **complies with SMPTE 272M A, B, and C**

APPLICATIONS

SDI Embedded Audio

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS9023ACFY	100 pin LQFP	0°C to 70°C

BRIEF DESCRIPTION

The GS9023A is a highly integrated, single chip solution for the multiplexing/demultiplexing of digital audio channels into and out of digital video signals. The GS9023A supports the multiplexing/demultiplexing of 20 or 24-bit synchronous audio data with a 48kHz sample rate.

Audio signals with different sample rates may be sample rate converted to 48kHz before and after the GS9023A using audio sample rate converters.

Each GS9023A supports all the processing required to handle the multiplexing/demultiplexing of four digital audio channels. To simplify system design, the GS9023A seamlessly integrates with common AES/EBU digital audio receivers and transmitters. The cascadable architecture allows for the multiplexing/demultiplexing of additional audio channels with no external glue logic.

The GS9023A supports video standards with rates from 143Mb/s to 540Mb/s. When in Multiplex Mode, the GS9023A supports the generation and insertion of EDH information according to SMPTE RP165. In combination with Gennum's GS9032, the GS9023A provides a low power, highly integrated two chip solution for SDI transmit applications. In combination with Gennum's GS7005, the GS9023A provides a low power, highly integrated two chip solution for SDI receive applications.

The GS9023A requires a 3.3V power supply for internal core logic and a 3.3V or 5V power supply for device I/O.

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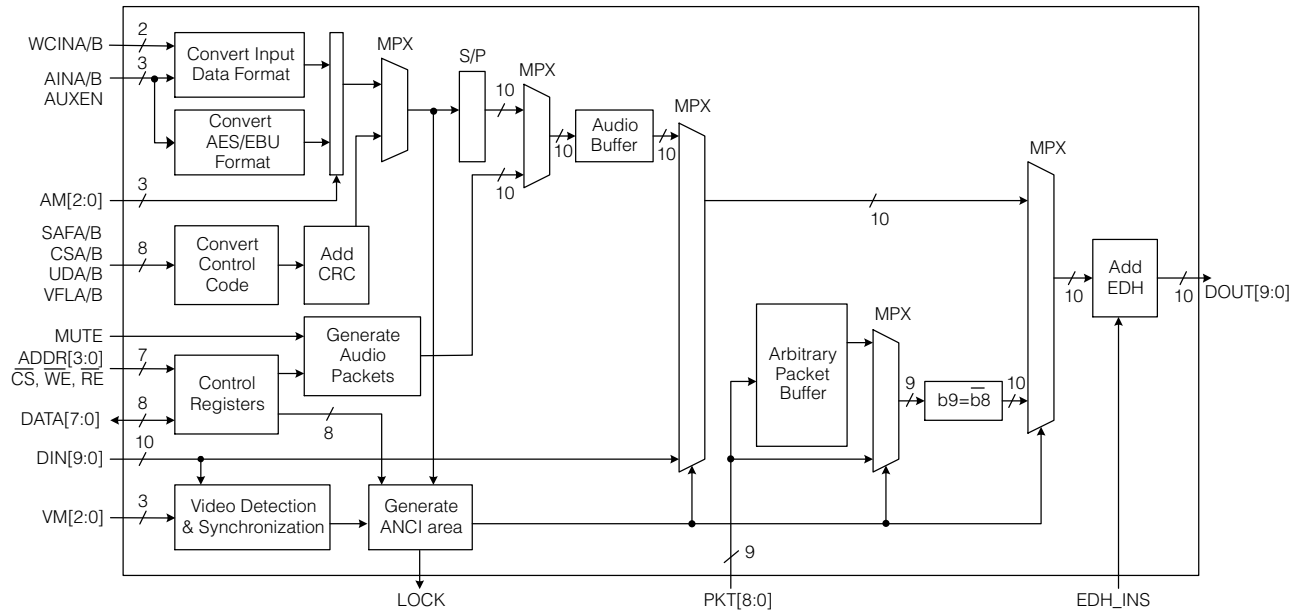
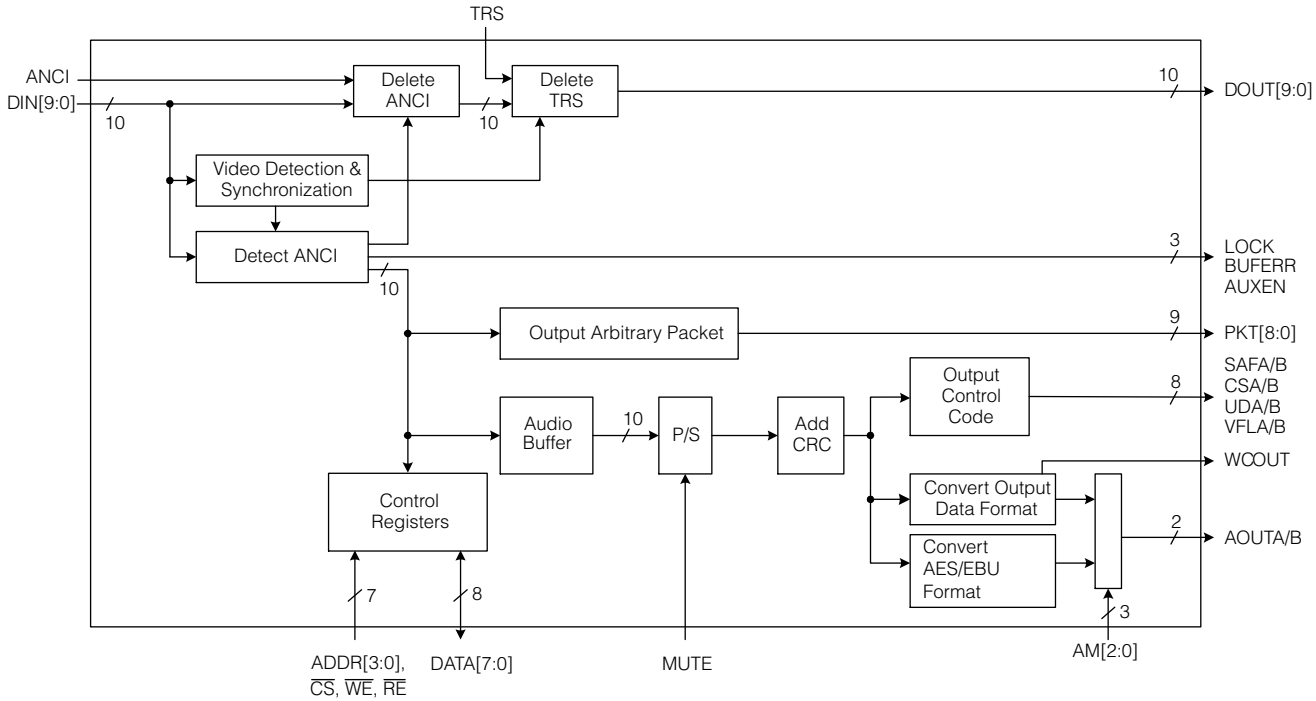


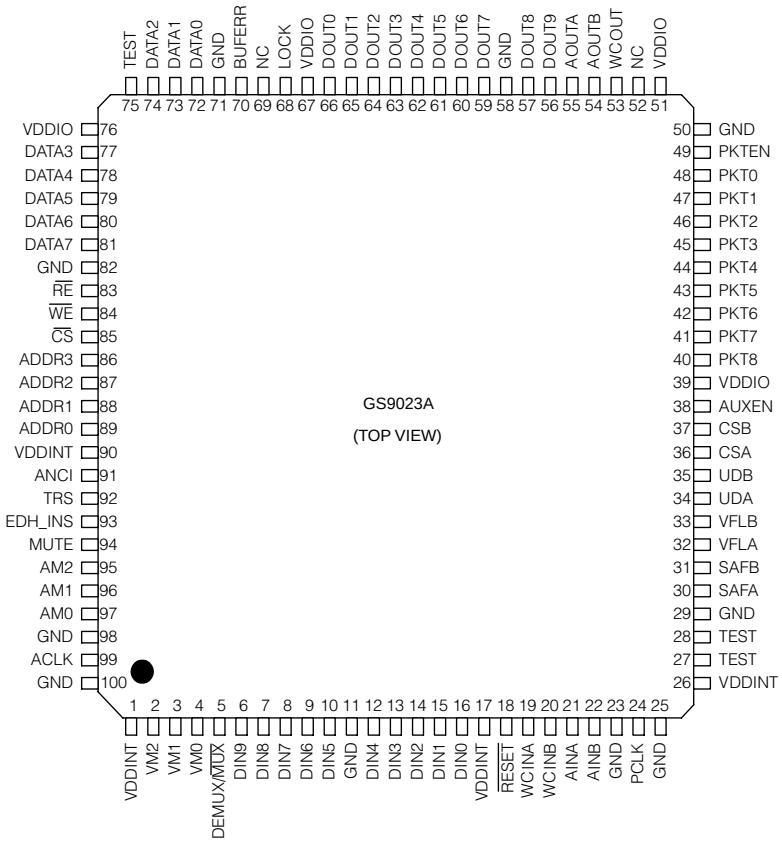
MULTIPLEX MODE BLOCK DIAGRAM



DEMULTIPLEX MODE BLOCK DIAGRAM

CONTENTS

1. PIN CONNECTIONS



NOTE: The GS9023A DOUT[9:0] MSB to LSB convention is compatible with the GS9022 but reversed with the GS9032 or GS7005.
See Interconnection with GS9032 or GS7005 section.

PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 17, 26, 90	VDDINT		+3.3V power supply pins for core logic.
2-4	VM[2:0]	I	Video standard format. Used in conjunction with the TRS pin. VM[2] is the MSB and VM[0] is the LSB. See Table 1.
5	DEMUX/$\overline{\text{MUX}}$	I	Mode of operation. When set HIGH, the GS9023A operates in Demultiplex Mode. When set LOW, the GS9023A operates in Multiplex Mode. NOTE: A device reset must be performed when switching between Multiplex and Demultiplex Modes while the device is powered up.
6-10,12-16	DIN[9:0]	I	Parallel digital video signal input. DIN[9] is the MSB and DIN[0] is the LSB. The digital video input must contain TRS information.
11, 23, 25, 29, 50, 58, 71, 82, 98, 100	GND		Device ground.
18	$\overline{\text{RESET}}$	I	Device reset. Active low. NOTE: The video input to output data path will be interrupted during device reset.

PIN DESCRIPTIONS (CONTINUED)

NUMBER	SYMBOL	TYPE	DESCRIPTION
19	WCINA	I	48kHz word clock for channels 1 and 2. Used only when operating in Multiplex Mode and when the audio source is not an AES/EBU data stream. This pin should be grounded when inputting AES/EBU digital audio data or when operating in Demultiplex Mode.
20	WCINB	I	48kHz word clock for channels 3 and 4. Used only when operating in Multiplex Mode and when the audio source is not an AES/EBU data stream. This pin should be grounded when inputting AES/EBU digital audio data or when operating in Demultiplex Mode.
21	AINA	I	Audio signal input for channels 1 and 2. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
22	AINB	I	Audio signal input for channels 3 and 4. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
24	PCLK	I	Video clock signal input.
27, 28, 75	TEST	-	Connect to ground.
30	SAFA	I/O	Start of audio frame indicator for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. SAFA is HIGH for audio frame 0 and LOW for all other audio frames. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
31	SAFB	I/O	Start of audio frame indicator for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. SAFB is set to HIGH for audio frame 0 and LOW for all other audio frames. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
32	VFLA	I/O	Validity flag for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. VFLA is HIGH when audio is invalid and LOW when audio is valid. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
33	VFLB	I/O	Validity flag for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. VFLB is HIGH when audio is invalid and LOW when audio is valid. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
34	UDA	I/O	User data for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
35	UDB	I/O	User data for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
36	CSA	I/O	Channel status for channels 1 and 2. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
37	CSB	I/O	Channel status for channels 3 and 4. Valid only for non-AES/EBU audio formats. This pin should be grounded when inputting AES/EBU audio data. In Multiplex Mode, this pin is an input and is supplied by the user. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.

PIN DESCRIPTIONS (CONTINUED)

NUMBER	SYMBOL	TYPE	DESCRIPTION
38	AUXEN	I/O	Extended audio enable. When HIGH, the GS9023A processes 24-bit audio samples. When LOW, the GS9023A processes 20-bit samples. In Multiplex Mode, this pin is an input and is supplied by the user. The setting is logical OR with the related A4ON setting in host interface register address 1h. In Demultiplex Mode, this pin is an output and is generated by the GS9023A.
39, 51, 67, 76	VDDIO		+3.3V or +5V power supply pins for device I/Os. In order for device I/O to be +5V tolerant V_{DDIO} must be +5V. Device I/O are not +5V tolerant if V_{DDIO} is +3.3V.
40-48	PKT[8:0]	I/O	Arbitrary data I/O bus. In Multiplex Mode, the user must input the arbitrary data packet words starting from the secondary data identification (SDID) to the last user data word (UDW) according to SMPTE 291M. The GS9023A internally converts the data to 10 bits by generating the inversion bit (bit 9). The checksum (CS) word is also generated internally. In Demultiplex Mode, the GS9023A outputs the arbitrary data packet words starting from the SDID to the last UDW. PKT[8] is the MSB and PKT[0] is the LSB. See Figure 11 and Figure 16.
49	PKTEN	I/O	Arbitrary data packet enable. In Multiplex Mode, PKTEN must be set HIGH one PCLK cycle before Arbitrary packet data is input to the device. In Demultiplex Mode, the output is set HIGH when outputting Arbitrary packet data. See Figure 11 and Figure 16.
52, 69	NC	N/A	No Connect. Do not connect these pins.
53	WCOUT	O	48kHz word clock for channels 1, 2, 3 and 4. Valid only when operating in Demultiplex Mode.
54	AOUTB	O	Audio signal output for channels 3 and 4. The AES/EBU digital audio output is bi-phase mark encoded. In all non-AES/EBU modes, the output is not bi-phase mark encoded.
55	AOUTA	O	Audio signal output for channels 1 and 2. The AES/EBU digital audio output is bi-phase mark encoded. In all non-AES/EBU modes, the output is not bi-phase mark encoded.
56, 57, 59-66	DOUT[9:0]	O	Parallel digital video signal output. DOUT[9] is the MSB and DOUT[0] is the LSB.
68	LOCK	O	Lock indicator. In Multiplex Mode, when HIGH, the video standard has been identified, the start of a new video frame has been detected and the device is multiplexing audio. NOTE: LOCK will not be set HIGH unless at least one of the audio channel enable bits is HIGH. See “CHACT” description in Table 14. In Demultiplex Mode, when HIGH, the video standard has been identified, the ‘lock’ process selected by “ACTSEL” has been validated and the device is demultiplexing audio. See “ACTSEL” description in Table 15. NOTE: LOCK remains active regardless of the number of audio samples in the video stream after ‘lock’ is achieved.
70	BUFERR	O	Buffer error. Indicates when an internal buffer overflow/underflow error has occurred. Valid only when the device is configured to operate in Demultiplex Mode. NOTE: If an internal buffer overflow/underflow condition occurs, the GS9023A does not mute the audio output.

PIN DESCRIPTIONS (CONTINUED)

NUMBER	SYMBOL	TYPE	DESCRIPTION
72-74, 77-81	DATA[0:7]	I/O	Host Interface data bus. DATA[7] is the MSB and DATA[0] is the LSB.
83	$\overline{RE}$	I	Read enable for Host Interface. Active LOW.
84	$\overline{WE}$	I	Write enable for Host Interface. Active LOW.
85	$\overline{CS}$	I	Chip select for Host Interface. Active LOW.
86-89	ADDR[3:0]	I	Host Interface address bus. ADDR[3] is the MSB and ADDR[0] is the LSB.
91	ANCI	I	ANCI Selection. Valid in Demultiplex Mode only. When set HIGH, each ancillary data packet with a DID corresponding to either the audio packet DID, the extended audio packet DID or the arbitrary packet DID is removed from the video signal. The data contained in the packets are output at the corresponding pins. The various DIDs are user programmable in the internal registers and are accessible via the Host Interface. NOTE: When ancillary data packets are deleted, the GS9023A does not recalculate the EDH checkwords. When set LOW, all ancillary data packets remain in the video signal.
92	TRS	I	TRS Selection. Used in conjunction with the VM[2:0] pins to select video standard format. In Multiplex Mode, when the TRS pin is HIGH, TRS is added to a composite video signal. In Demultiplex Mode, when HIGH, TRS is removed from a composite video signal. See Table 1.
93	EDH_INS	I	EDH Insert Selection. Valid in Multiplex Mode only. When set HIGH, the GS9023A performs EDH functions according to SMPTE RP165. When set LOW, EDH is not inserted. This setting is logical OR with the related EDHON setting in host interface register address 1h. NOTE: Active picture and full field data words are updated from recalculated values but error flag information is replaced with the values programmed in the internal registers via the Host Interface.
94	MUTE	I	Audio mute. In Multiplex Mode, when set HIGH, the embedded audio packets are forced to '0'. In Demultiplex Mode, when set HIGH, the output data is forced to "0". This setting is logical OR with the related MUTE setting in host interface address 4h.
95-97	AM[2:0]	I	Audio mode format. In Multiplex Mode, AM[2:0] indicates the input audio data format. In Demultiplex Mode, AM[2:0] indicates the output audio data format. AM[2] is the MSB and AM[0] is the LSB. See Table 2.
99	ACLK	I	Input audio signal clock (128 fs). Synchronous to PCLK. In non-AES/EBU audio modes, the serial audio data is sampled on both edges of ACLK.

NOTE: All unused inputs of the GS9023A should be connected to ground.

2. DETAILED DESCRIPTION

The GS9023A has two main modes of operation: Multiplex Mode and Demultiplex Mode. In Multiplex Mode, which is selected by setting the DEMUX/$\overline{\text{MUX}}$ input pin LOW, digital audio is embedded into a digital video stream. In Demultiplex Mode, which is selected by setting the DEMUX/$\overline{\text{MUX}}$ input pin HIGH, digital audio is extracted from a digital video stream. Table 14 and Table 15 contain Host Interface Register descriptions for the Multiplex and Demultiplex Modes respectively.

2.1 MULTIPLEX MODE

2.1.1 Video Clock Input

A master video clock must be supplied to the PCLK pin corresponding to the selected video standard. The supported video input standards and corresponding clock frequencies are listed in Table 1.

2.1.2 Video Data Input

The video data DIN[9:0] is clocked into the GS9023A on the rising edge of PCLK. The video clock frequency must correspond to the video input standard selected. This is done via the "VSEL" bit of Host Interface Register #0h. When "VSEL" is LOW, the video input standard is selected by the VM[2:0] and TRS input pins. When "VSEL" is HIGH, the video input standard is selected by the "VMOD[2:0]" and "D2_TRS" bits in Host Interface Register #0h. The supported video input standards are listed in Table 1.

After the user has specified the video input standard via the VM[2:0] and TRS pins or by setting Host Interface Register #0h, the GS9023A performs video standard detection to verify that the input video stream corresponds to the selected standard. The LOCK output pin and the "LOCK" bit of Host Interface Register #0h are then set HIGH if at least one of the audio channel enable bits "CHACT(4-1)" of Host Interface Register #1h is HIGH and the start of a video frame is detected.

NOTE: The user must ensure that the video input format correctly corresponds to the video format being provided to the GS9023A. For 8-bit video operation, the "8BIT_SEL" bit of the Host Interface Register #2h must be set HIGH.

TABLE 1 VIDEO INPUT FORMATS

VIDEO STANDARD	SERIAL DIGITAL DATA RATE (MBPS)	PCLK FREQUENCY (MHZ)	VM[2] OR "VMOD[2]"	VM[1] OR "VMOD[1]"	VM[0] OR "VMOD[0]"	TRS OR "D2_TRS"
525/D2 (SMPTE259M)	143	14.3	0	0	0	0
525/D2 (SMPTE244M)	143	14.3	0	0	0	1
525/D1	270	27.0	0	0	1	0
Reserved	-	-	0	0	1	1
525/16:9	360	36.0	0	1	0	0
Reserved	-	-	0	1	0	1
525/4:4:4:4 (System #1)	540	54.0	0	1	1	0
Reserved	-	-	0	1	1	1
625/D2 (with TRS)	177	17.7	1	0	0	0
625/D2 (without TRS)	177	17.7	1	0	0	1
625/D1	270	27.0	1	0	1	0
Reserved	-	-	1	0	1	1
625/16:9	360	36.0	1	1	0	0
Reserved	-	-	1	1	0	1
625/4:4:4:4 (System #2)	540	54.0	1	1	1	0
625/4:2:2P (System #4)	540	54.0	1	1	1	1

2.1.2.1 Synchronous Switch of Video Input

When a 525-line video input to the GS9023A undergoes a synchronous switch between two video sources, the two video sources may have 5-frame sequences which are not aligned. In this case, the GS9023A may not correctly detect the new 5-frame sequence, and the internal FIFO may overflow/underflow continuously. To avoid this problem, it is recommended that the user sets bits 5, 6, and 7 of Host Interface Register #2h HIGH (see bit descriptions in Table 14). Setting these bits HIGH will permit the device to reset the internal audio sample buffer when an overflow/underflow condition is detected and mute the embedded audio packets during this reset.

2.1.3 Video Data Output

The video signal is output at the DOUT[9:0] pins. The video signal is synchronized to the rising edge of PCLK. When the GS9023A is properly configured, audio packets, extended audio packets, audio control packets and arbitrary data packets are multiplexed into the output video signal. When the video signal is a 525 line or 625 line D2 format, TRS information is added to the video signal if the TRS input pin or the "D2_TRS" and "VSEL" bits of Host Interface Register #0h are HIGH. EDH packets can also be inserted into the video signal by setting the EDH_INS pin HIGH or by setting the "EDHON" bit HIGH of Host Interface Register #1h. When selected, the GS9023A inserts EDH packets according to SMPTE RP165.

NOTE: Active picture and full field data words are updated from recalculated values but error flag information is replaced with the values programmed in Host Interface Registers #Eh and #Fh.

NOTE: In the 525/4:4:4:4 video standard, EDH packets should not be inserted as this can lead to TRS signal corruption. When EDH packets are not inserted, the "EDHDEL" bit of Host Interface Register #0h controls the deletion of EDH packets. When the "EDHDEL" bit is set LOW, EDH packets are deleted from the incoming video signal. When "EDHDEL" is set HIGH, EDH packets pass through the device unchanged.

NOTE: "EDHDEL" functionality is valid only when the "CASCADE" bit of Host Interface Register #4h is LOW.

2.1.4 Audio Clock Input

A master audio clock (128 fs: 6.144MHz) must be supplied to the ACLK pin. This clock must be synchronized with the video signal input to the GS9023A. An audio word clock must also be supplied (fs: 48kHz) to the WCINA/B pins when using non-AES/EBU audio. The two 48kHz word clocks must also be synchronized to the video signal.

2.1.5 Audio Data Input

The serial audio data for channels 1 and 2 are input to the AINA pin. The serial audio data for channels 3 and 4 are input to the AINB pin. The GS9023A can multiplex 20 or 24 bit audio data samples. When the AUXEN pin or bit "A4ON" of Host Interface Register #1h is HIGH, the device processes 24 bit audio samples. When the AUXEN pin or "A4ON" register bit is LOW, the device processes 20 bit audio samples. On power up, the "A4ON" bit default is LOW.

The GS9023A offers five predefined audio data input formats, selected via the AM[2:0] pins, which are listed in Table 2 and illustrated in Figure 1. The first four predefined formats relate to non-AES/EBU audio data while the fifth format corresponds to the AES/EBU audio format. The WCINA and WCINB pins should be grounded when inputting AES/EBU audio data as they are not used.

The GS9023A supports muting of the audio data input. Multiplexed audio and extended data packets for all channels are forced to zero when the MUTE pin or "MUTE" bit of Host Interface Register #4h is set HIGH.

When inputting AES/EBU data, the CRC byte and parity bit will be recalculated and inserted automatically.

2.1.6 Control Code Input

When inputting non-AES/EBU audio data, the validity (V), user data (U) and channel status (C) bits of each audio data channel must be input to the corresponding pins (VFLA, VFLB; UDA, UDB; CSA, CSB). The signals must be updated on the rising edge of WCINA/B and remain constant for the entire word clock period (64 ACLK cycles).

When inputting non-AES/EBU audio data, the SAFA and SAFB pins must be high for one frame out of 192 frames received to indicate the start of frame condition.

When inputting AES/EBU audio data, the control code input pins should be grounded as they are not used.

TABLE 2 AUDIO INPUT FORMATS

FORMATS	WCINA/B	AM[2]	AM[1]	AM[0]
AIN-MODE 0	User Supplied	0	0	0
AIN-MODE 1	User Supplied	0	0	1
AIN-MODE 2	User Supplied	0	1	0
AIN-MODE 3	User Supplied	0	1	1
AIN-AES/EBU	Not Used	1	0	0
Not Used	-	1	0	1
Not Used	-	1	1	0
Not Used	-	1	1	1

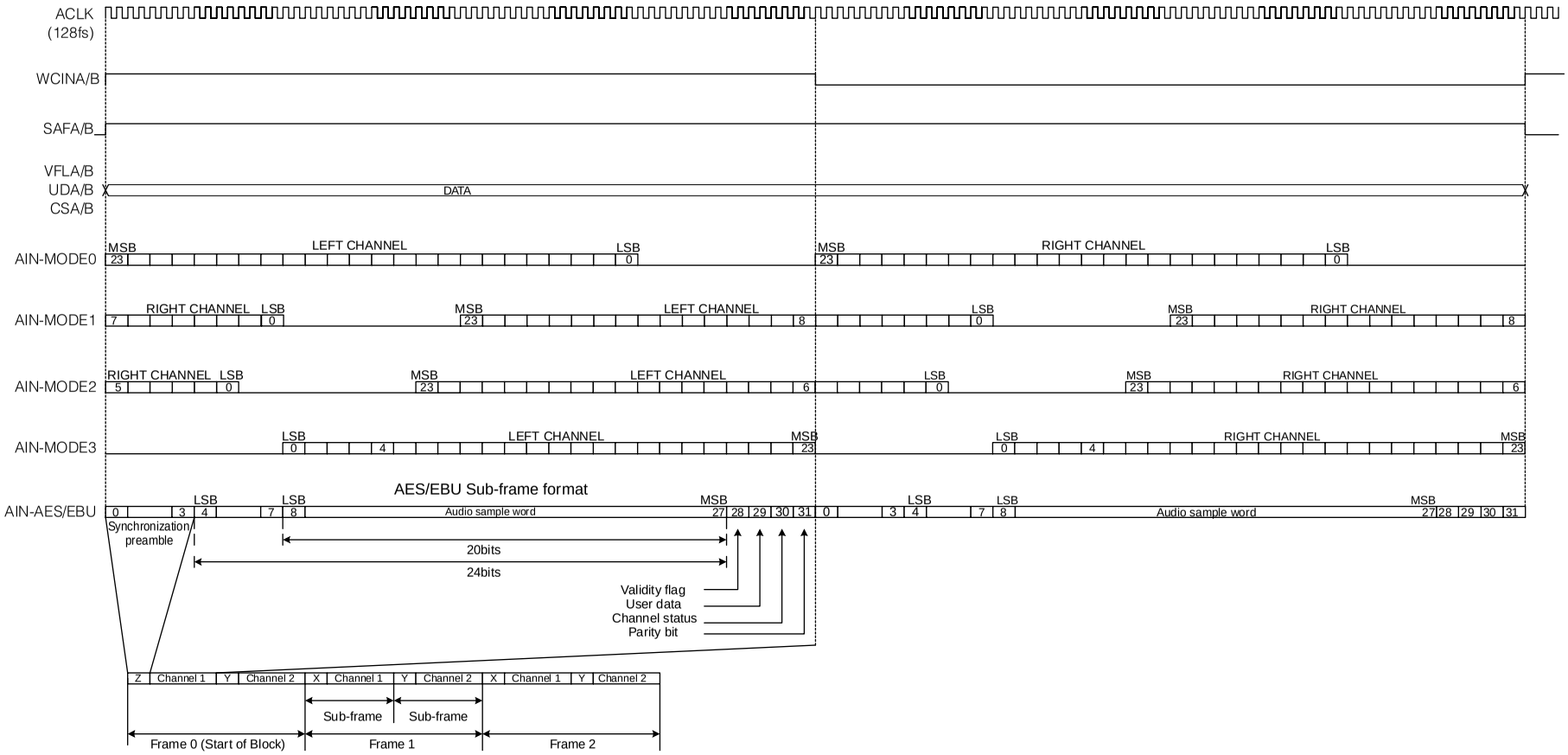


Figure 1 Audio Input Format Timing Diagram

2.1.7 Audio Data Packets

The GS9023A can multiplex up to four audio channels. The channels are selectable via the “CHACT(4-1)” bits of Host Interface Register #1h. The audio group (Audio packet data ID) for each device is configured in “AD20ID[3:0]” of Host Interface Register #3h. On power up, the four audio channels and audio group 1 are selected by default.

By setting all the “CHACT(4-1)” bits in Host Interface Register #1h to zero, the GS9023A will be in bypass mode whereby any existing audio data packets, with the same audio group ID or otherwise, will pass through the device unchanged and no new audio data packets will be embedded.

NOTE: Do not rely on default value. Reprogram on power up or reset.

The “CASCADE” bit in Host Interface Register #4h controls the manner in which multiplexing is performed. When “CASCADE” is LOW, the GS9023A deletes all existing ancillary packets. New packets are multiplexed at the first location after the end of active video (EAV) in the horizontal ancillary space (HANC). See Figure 2.

When “CASCADE” is HIGH, the GS9023A multiplexes packets at the first free location in the horizontal ancillary (HANC) space after the end of active video (EAV) if there is sufficient space remaining to insert the packet. The GS9023A does not check if existing audio group samples are present in the video signal. Use caution in applications where the video signal contains existing audio packets to avoid adding identical group samples. See Figure 3.

The GS9023A assumes that the ancillary space from the first free location is empty to the start of active video (SAV). Existing ancillary data packets (inserted by previous devices) in the video signal must be contiguous from the beginning of the HANC space or the insertion of a new audio data packet may overwrite existing data. See Figure 4.

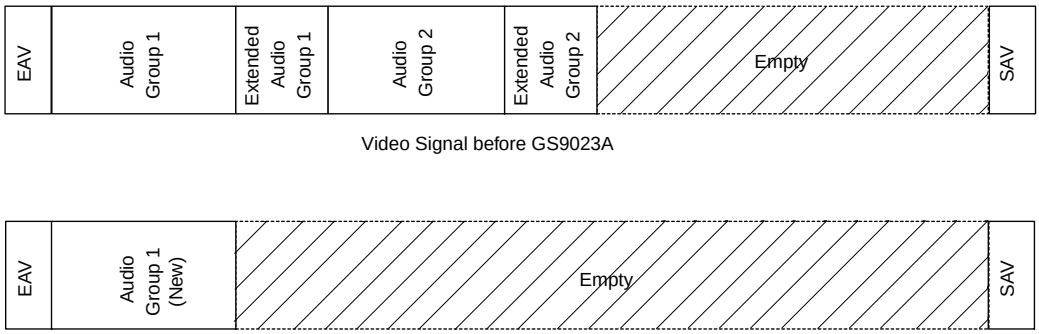


Figure 2

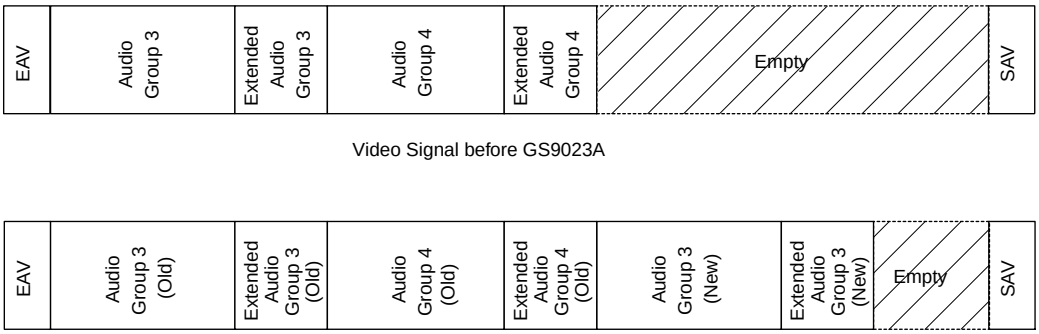


Figure 3

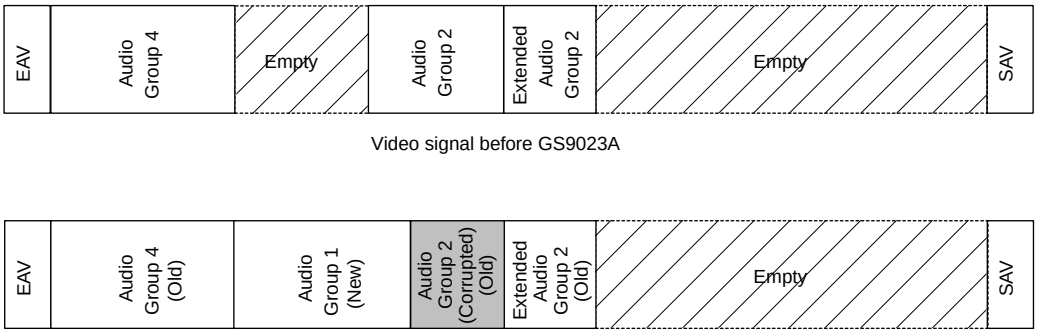


Figure 4

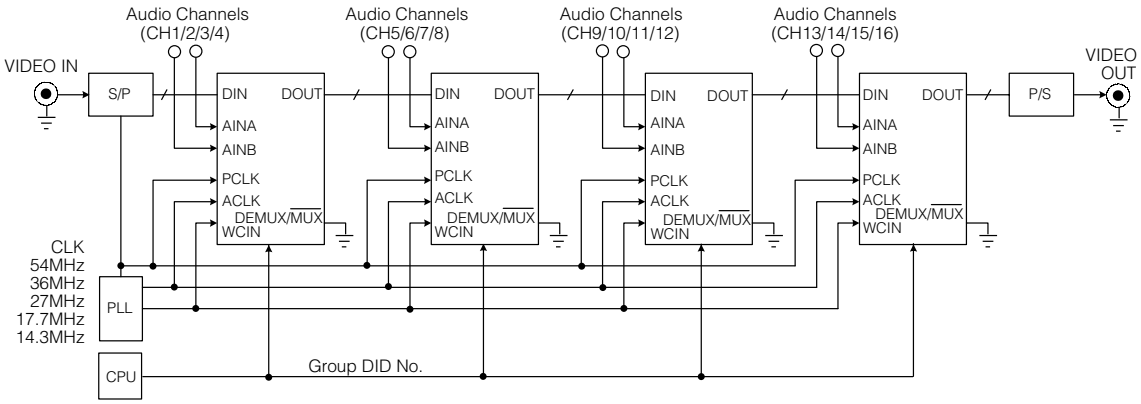


Figure 5 Multiplex Mode Cascadable Architecture

In cases where an audio data packet does not fit inside the remaining HANC space, the audio packet is discarded. In this case, the “ADERR” bit of Host Interface Register #7h is HIGH indicating an audio packet multiplexing error. The error bit is cleared once accessed by the Host Interface.

By cascading four GS9023A devices, it is possible to multiplex up to 16 audio channels (according to SMPTE 272) in a component video signal as shown in Figure 5.

NOTE 1: In the 525/D1 video format, only 15 channels of 24 bit audio can be multiplexed.

NOTE 2: In cascade mode, audio samples embedded by the first GS9023A may be delayed by up to one audio sample with respect to the audio embedded by cascaded devices.

NOTE 3: When multiplexing audio data into a 525-line video signal at 29.97fps, the GS9023A establishes a 5-frame sequence based on the relationship between the incoming audio and the input video timing. When multiple GS9023As are used to multiplex several audio channels, the video signal will undergo a processing delay of 13 video clock cycles through each device. This may affect the timing relationship between the devices such that a different 5-frame sequence may be established in a subsequent GS9023A. For example, Figure 6 shows two GS9023As cascaded to multiplex eight audio channels. The video signal will be delayed 13 video clock cycles in the first encoder. This timing discrepancy may cause the second GS9023A to establish a different 5-frame sequence from the first.

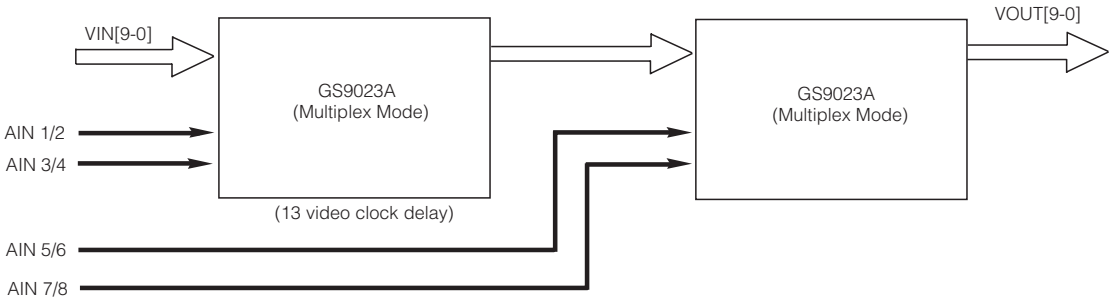
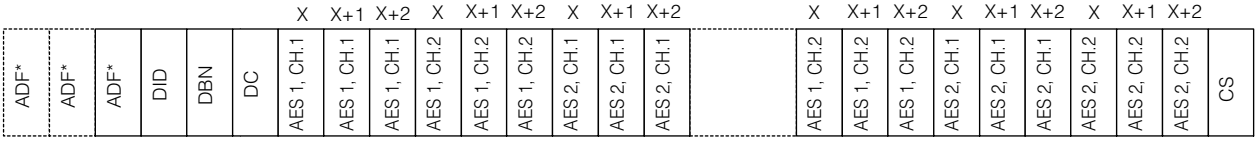


Figure 6 Multiplexing 2 Audio Groups using 2 GS9023As



* The ancillary data flag, ADF, is one word in composite systems (ANSI/SMPTE 259M) and three words in component systems (ANSI/SMPTE 125M).

Figure 7 Audio Data Packet Structure with 4 Audio Channels, 1 Audio Group

Cascade operation is not recommended with a composite video signal, as there is insufficient HANC space for more than four channels of audio. Audio packet insertion is not guaranteed in this case.

The audio data packet structure as described in SMPTE 272M is shown in Figure 7.

The audio data packets words are defined as follows:

ADF: Ancillary Data Flag. The ancillary data flag marks the beginning of an ancillary packet and is automatically generated by the GS9023A.

DID: Data ID. Audio data packets corresponding to an audio group are selected by programming “A20ID[3:0]” of Host Interface Register #3h for audio groups 1 to 4 as follows:

Group 1: Fh (2FFh)

Group 2: Dh (1FDh)

Group 3: Bh (1FBh)

Group 4: 9h (2F9h)

NOTE: The six most significant bits of the DID are internally generated by the GS9023A.

DBN: Data Block Number. The data block number is used when data blocks within a common data ID are to be linked or to distinguish consecutive data blocks within a common data ID. The data block number continuously increments from 1 to 255 and is generated automatically by the GS9023A.

DC: Data Count. The data count represents the number of user data words to follow (maximum of 255 words). The data count is automatically generated by the GS9023A.

CS: Checksum. The checksum consists of nine bits. The checksum is used to determine the validity of the words data ID through user data. It is the sum of the nine least significant bits of the words data ID through user data. The checksum is automatically generated by the GS9023A.

The serial audio data samples, are mapped into three contiguous ancillary data words (X, X+1, X+2) as shown in Table 3.

TABLE 3 AUDIO PACKET DATA SAMPLE STRUCTURE

BIT	WORD X	WORD X+1	WORD X+2
b9	not b8	not b8	not b8
b8	aud 5	aud 14	P
b7	aud 4	aud 13	C
b6	aud 3	aud 12	U
b5	aud 2	aud 11	V
b4	aud 1	aud 10	aud 19 (MSB)
b3	aud 0 (LSB)	aud 9	aud 18
b2	ch 1 (MSB)	aud 8	aud 17
b1	ch 0 (LSB)	aud 7	aud 16
b0	Z	aud 6	aud 15

TABLE 4 CHANNEL IDENTIFICATION WITHIN THE AUDIO GROUPS

CH 1	CH 0	GROUP 1	GROUP 2	GROUP 3	GROUP 4
0	0	Channel 1	Channel 5	Channel 9	Channel 13
0	1	Channel 2	Channel 6	Channel 10	Channel 14
1	0	Channel 3	Channel 7	Channel 11	Channel 15
1	1	Channel 4	Channel 8	Channel 12	Channel 16

The audio packet data sample bits are defined as follows:

Z: The Z flag is set HIGH at the same sample coincident with the beginning of a new AES channel status block (frame 0) and is otherwise set LOW. In non-AES/EBU data input formats this bit is set to the value of the SAFA/B input pins at the rising edge of WCINA/B.

ch[1:0]: Identification of the channels in an audio group as shown in Table 4.

aud[19:0]: Twos complement linearly represented audio data. The audio data is input from the AINA and AINB pins.

V: AES/EBU sample validity bit. If the audio sample is valid the bit is set LOW. If the audio sample is invalid, the bit is set HIGH. In non-AES/EBU data input formats, this bit is set to the value of the VFLA/B input pins at the rising edge of WCINA/B.

U: AES/EBU user bit. In non-AES/EBU data input formats, this bit is set to the value of the UDA/B input pins at the rising edge of WCINA/B.

C: AES/EBU audio channel status bit. In non-AES/EBU data input formats this bit is set to the value of the CSA/B input pins at the rising edge of WCINA/B.

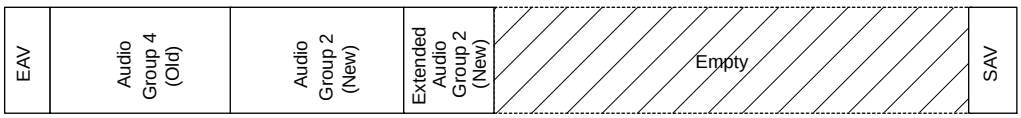
P: Even parity for the 26 previous bits in the audio data sample (excludes b9 in the first and second words).

NOTE: The P bit is not the same as the AES/EBU parity bit. This bit is automatically generated by the GS9023A.

2.1.8 Extended Audio Data Packets

The GS9023A can multiplex 20 or 24 bit audio samples. For 24 bit audio samples, the 20 MSBs of a 24 bit audio sample are contained in the audio data packets and the 4 LSBs are contained in an extended audio data packet as defined in SMPTE 272. The extended audio data packet is multiplexed immediately following the corresponding audio data packet. See Figure 8.

Video signal before GS9023A



Video signal after GS9023A Insertion of Audio Group 2 & Extended Audio Group 2 ("CASCADE" = HIGH)

Figure 8

* The ancillary data flag, ADF, is one word in composite systems (ANSI/SMPTE 259M) and three words in component systems (ANSI/SMPTE 125M).

Figure 9 Extended Audio Data Packet Structure

To select 24 bit audio operation, the user must set the AUXEN pin or the "A4ON" bit of Host Interface Register #1h HIGH. When the AUXEN pin or "A4ON" bit is HIGH, the GS9023A does not multiplex the audio data packet and the associated extended audio data packet if there is insufficient room for both in the HANC space. In this case, the "ADERR" bit of Host Interface Register #7h is set HIGH, indicating an audio packet multiplexing error. The error bit is cleared when accessed by the Host Interface. The audio group (Extended packet data ID) for each device is configured in "AD4ID[3:0]" of Host Interface Register #3h. On power up, audio group 1 is selected by default.

By cascading four GS9023A devices, it is possible to multiplex up to 16 audio channels (according to SMPTE 272) in a component video signal as shown in Figure 5.

NOTE: In the 525/D1 video format, only 15 channels of 24 bit audio can be multiplexed in the cascade configuration.

The extended audio data packet structure as described in SMPTE 272M is shown in Figure 9.

The extended audio data packets words are defined as follows:

ADF: Ancillary Data Flag. The ancillary data flag marks the beginning of an ancillary packet and is automatically generated by the GS9023A.

DID: Data ID. Extended audio data packets corresponding to an audio group are selected by programming "A4ID[3:0]" of Host Interface Register #3h for audio groups 1 to 4 as follows:

Group 1: Eh (1FEh)

Group 2: Ch (2FCh)

Group 3: Ah (2FAh)

Group 4: 8h (1F8h)

NOTE: The six most significant bits of the DID are automatically generated by the GS9023A.

DBN: Data Block Number. The data block number is used when data blocks within a common data ID are to be linked or to distinguish consecutive data blocks within a common data ID. The data block number continuously increments from 1 to 255 and is generated automatically by the GS9023A.

DC: Data Count. The data count represents the number of user data words to follow (maximum of 255 words). The data count is automatically generated by the GS9023A.

DATA WORDS: The extended audio data samples are mapped into ancillary data words as shown in Table 5.

TABLE 5 EXTENDED AUDIO PACKET DATA SAMPLE STRUCTURE

BIT	ANC DATA WORD
b9	not b8
b8	a
b7	y3 (MSB)
b6	y2
b5	y1
b4	y0 (LSB)
b3	x3 (MSB)
b2	x2
b1	x1
b0	x0 (LSB)

The extended audio packet data sample bits are defined as follows:

x[3:0]: Auxiliary data from subframe 1.

y[3:0]: Auxiliary data from subframe 2.

a: Address pointer. LOW for channels 1 and 2, and HIGH for channels 3 and 4. This bit is internally generated by the GS9023A.

CS: Checksum. The checksum consists of nine bits. The checksum is used to determine the validity of the words data ID through user data. It is the sum of the nine least significant bits of the words data ID through user data. The checksum is automatically generated by the GS9023A.

2.1.9 Audio Control Packets

The audio control packet structure is detailed in SMPTE 272M. The audio group (Audio control packet data ID) for each device is configured in “ACID[3:0]” of Host Interface Register #4h. The Audio control parameters are configured in Host Interface Registers #Ah, #Bh, #Ch and #Dh. The audio control packet multiplexing positions for the various video standards are listed in Table 6. In a component video signal, a maximum of 4 audio control packets can be multiplexed in a cascade connection. On power up, audio group 1 is selected by default.

The GS9023A determines if multiplexing is possible by searching for the first free location in the HANC space after the signal EAV and calculates if there is sufficient remaining space to insert the audio packet. Existing ancillary data packets (inserted by previous devices) in the video signal must be contiguous from the beginning of the HANC space or the insertion of a new audio data packet may overwrite existing data. In cases where an audio control data packet does not fit inside the remaining HANC space, the audio control packet is discarded. In this case, the “ACERR” bit of Host Interface Register #7h is HIGH indicating an audio control packet multiplexing error. The error bit is cleared when accessed by the Host Interface.

The audio control packet structure as described in SMPTE 272M is shown in Figure 10.

TABLE 6 MULTIPLEXING POSITIONS FOR AUDIO CONTROL PACKETS

VIDEO STANDARD	MULTIPLEXING LINES	HORIZONTAL STARTING POSITION	HORIZONTAL ENDING POSITION
525/D2	12/275	795	849
525/D1	12/275	1444	1711
525/16:9	12/275	1924	2283
525/4:4:4:4	12/275	2884	3427
625/D2	8/321	972	1035
625/D1	8/321	1444	1723
625/16:9	8/321	2277	2299
625/4:4:4:4	8/321	2884	3451
625/4:2:2P	15/641	1444	1723

* The ancillary data flag, ADF, is one word in composite systems (ANSI/SMPTE 259M) and three words in component systems (ANSI/SMPTE 125M).

Figure 10 Audio Control Packet Structure

The audio control packets words are defined as follows:

ADF: Ancillary Data Flag. The ancillary data flag marks the beginning of an ancillary packet and is automatically generated by the GS9023A.

DID: Data ID. Audio control packets corresponding to an audio group are selected by programming “ACID[3:0]” of Host Interface Register #4h for audio groups 1 to 4 as follows:

Group 1: Fh (1EFh)

Group 2: Eh (2EEh)

Group 3: Dh (2EDh)

Group 4: Ch (1ECh)

NOTE: The six most significant bits of the DID are automatically generated by the GS9023A.

DBN: Data Block Number. The data block number is used when data blocks within a common data ID are to be linked or to distinguish consecutive data blocks within a common data ID. The data block number continuously increments from 1 to 255 and is generated automatically by the GS9023A.

DC: Data Count. The data count represents the number of data words to follow. The data count has a fixed value of 212h and is automatically generated by the GS9023A.

AF1-2: Audio frame number for channels 1 and 2.

AF3-4: Audio frame number for channels 3 and 4.

For an audio sampling frequency of 48kHz, the audio frame numbers are sequenced from one to five for 525 line video standards and fixed at one for 625 line video standards. The audio frame numbers, AF1-2 and AF3-4, are automatically generated by the GS9023A and set to the same value. The sequence count is started at one at the first frame after ‘lock’ is achieved.

RATE: Sampling frequency. The GS9023A operates at a fixed sampling frequency of 48kHz. The audio control packet RATE word structure is shown in Table 7.

TABLE 7 AUDIO CONTROL PACKET RATE WORD STRUCTURE

BIT	RATE WORD
b9	not b8
b8	not used (fixed to 0)
b7	y2 (MSB, fixed to 0)
b6	y1 (fixed to 0)
b5	y0 (LSB, fixed to 0)
b4	bsync
b3	x2 (MSB, fixed to 0)
b2	x1 (fixed to 0)
b1	x0 (LSB, fixed to 0)
b0	async

The audio control packet RATE word bits are defined as follows:

x[2:0], y[2:0]: Audio sampling rate for subframe 1 and 2 respectively. Fixed at 48kHz.

async, bsync: Set LOW when each audio channel pair is operating synchronously and set HIGH when operating asynchronously. Forced LOW due to synchronous operation.

ACT: The ACT word indicates the active group channels. The audio control packet ACT word structure is shown in Table 8.

TABLE 8 AUDIO CONTROL PACKET ACT WORD STRUCTURE

BIT	ACT WORD
b9	not b8
b8	p
b7	reserved (set to 0)
b6	reserved (set to 0)
b5	reserved (set to 0)
b4	reserved (set to 0)
b3	a4
b2	a3
b1	a2
b0	a1

The audio control packet ACT word bits are defined as follows:

p: Even parity for bits b0 to b7.

a(4-1): Individual active channel status indicator. The bits correspond directly to the "CHACT(4-1)" bits of Host Interface Register #1h. The bits are set HIGH for each active channel in a given audio group. The correlation of the active channels for the four active audio groups is shown in Table 9.

TABLE 9 AUDIO CONTROL PACKET ACTIVE CHANNEL CONFIGURATION

	GROUP1	GROUP2	GROUP3	GROUP4
CHACT 1	Channel 1	Channel 5	Channel 9	Channel 13
CHACT 2	Channel 2	Channel 6	Channel 10	Channel 14
CHACT 3	Channel 3	Channel 7	Channel 11	Channel 15
CHACT 4	Channel 4	Channel 8	Channel 12	Channel 16

DELx(0-2): Indicates the amount of accumulated audio processing delay relative to video, measured in audio sample intervals for each of the channels. Positive values indicate that the video leads the audio. The audio control packets delay word structure is shown in Table 10.

TABLE 10 AUDIO CONTROL PACKET DELAY STRUCTURE

BIT	DELX0	DELX1	DELX2
b9	not b8	not b8	not b8
b8	dela/b 7	dela/b 16	dela/b 25 (Sign)
b7	dela/b 6	dela/b 15	dela/b 24 (MSB)
b6	dela/b 5	dela/b 14	dela/b 23
b5	dela/b 4	dela/b 13	dela/b 22
b4	dela/b 3	dela/b 12	dela/b 21
b3	dela/b 2	dela/b 11	dela/b 20
b2	dela/b 1	dela/b 10	dela/b 19
b1	dela/b 0 (LSB)	dela/b 9	dela/b 18
b0	e	dela/b 8	dela/b 17

The audio control packet delay word bits are defined as follows:

e: Indicates valid audio delay data when set HIGH. Corresponds to the "ACDLY" bit of Host Interface Register #Dh.

dela/b[25:0]: The audio channel pair delay is programmed in bits "DELA/B[25:0]" of Host Interface Register #Ah, #Bh, #Ch and #Dh. DELA[25:0] corresponds to the delay for channels 1 and 2. "DELB[25:0]" corresponds to the delay for channels 3 and 4.

RSRV: Reserved. The word is fixed at 200h and is automatically generated by the GS9023A.

CS: Checksum. The checksum consists of nine bits. The checksum is used to determine the validity of the words data ID through user data. It is the sum of the nine least significant bits of the words data ID through user data. The checksum is automatically generated by the GS9023A.

2.1.10 Arbitrary Data Packets

The GS9023A is capable of multiplexing arbitrary data packets according to SMPTE 291M. Typically, this consists of linear time code data (LTC), vertical interval time code data (VITC) or other data which is multiplexed once per field. The user must input the 9 LSBs starting from the secondary data identification (SDID) word to the last user data word (UDW) of the ancillary data packet containing arbitrary data. The CS word and bit 10 of all words in the packet are internally generated.

The arbitrary data packet data ID is configured in "PKTID[7:0]" of Host Interface Register #5h. To process arbitrary data, the user must set the "PKON" bit of Host Interface Register #1h. Also, the user must specify the line number in "PKTLINE[7:0]" in Host Interface Register #9h. This value corresponds to the line in video field 1 in which the user wants the arbitrary data packet to be multiplexed. The corresponding line in field 2 is automatically selected for arbitrary data packet multiplexing. Arbitrary data is typically multiplexed during the active portion of the line in the vertical blanking interval (VBI). Care should be taken to avoid selecting a line in the active picture. Table 11 lists recommended multiplexing lines according to the video standard.

NOTE: In field #1, the line number is offset by one from the value configured in "PKTLINE[7:0]".Arbitrary data is input to the GS9023A as shown in Figure 11. The data is stored in an internal arbitrary data packet buffer which is cleared at the end of every field. Arbitrary data must be written to the buffer before the line number specified in "PKTLINE[7:0]" is reached in order for the packet to be multiplexed. Data is input to the PKT[8:0] pins and clocked in on the rising edge of PCLK. PKTEN must be set HIGH one PCLK cycle before the data at the PKT[8:0] inputs is valid. PKTEN must go LOW one PCLK cycle before the last user data word (UDW) is input to the PKT[8:0] inputs. Parity (bit 8) for each UDW can be enabled by setting the "PKTPRTY" bit of Host Interface Register #8h to HIGH. When "PKTPRTY" is HIGH, data input at PKT[8] is overwritten by the parity bit.

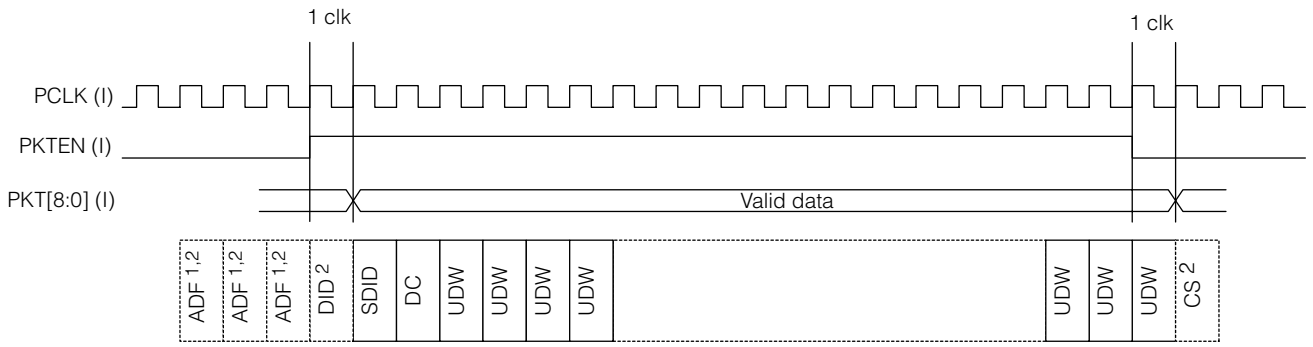
Up to 255 words (253 UDWs + SDID + DC) can be input and multiplexed once per field.

The arbitrary data packet structure as described in SMPTE 291M is shown in Figure 11.

TABLE 11 MULTIPLEX POSITION FOR ARBITRARY DATA PACKET

VIDEO STANDARD	RECOMMENDED MULTIPLEX LINE	HORIZONTAL STARTING POSITION (WORD #)	HORIZONTAL ENDING POSITION (WORD #)
525/D2	9/272	340	360
525/D1	14/277	0	1439
525/16:9	14/277	0	1919

NOTE: 525/4:4:4:4 and all 625 line video standards are not supported.
* Horizontal Starting Position 0 is the first word of the active picture.



NOTE: 1 - The ancillary data flag, ADF, is one word in composite systems (ANSI/SMPTE 259M) and three words in component systems (ANSI/SMPTE 125M).
2 - The ADF, DID and CHKSUM words are automatically generated by the GS9023A.

Figure 11 Arbitrary Data Packet Input Timing Diagram

The arbitrary data packet words are defined as follows:

ADF: Ancillary Data Flag. The ancillary data flag marks the beginning of an ancillary packet and is automatically generated by the GS9023A.

DID: Data ID. Configured in "PKTID[7:0]" of Host Interface Register #5h. The two most significant bits are internally generated by the GS9023A.

SDID: Secondary Data ID. The Secondary Data ID is handled as user input data.

DC: Data Count. The data count represents the number of user data words to follow, up to a maximum of 255 words. The data count is handled as user input data. For the GS9023A the maximum data count is 253 since the total number of words that can be input is 255 less the SDID and DC words.

UDW: User Data Word.

CS: Checksum. The checksum consists of nine bits. The checksum is used to determine the validity of the words data ID through user data. It is the sum of the nine least significant bits of the words data ID through user data. The checksum is automatically generated by the GS9023A.

2.1.11 Error Detection

The GS9023A provides error status information in Host Interface Register #7h as described in Table 14. All errors are cleared when Host Interface Register #7h is read.

2.2 DEMULTIPLEX MODE

2.2.1 Video Clock Input

A master video clock must be supplied to the PCLK pin corresponding to the selected video signal. The supported video input standards and corresponding clock frequencies are listed in Table 1.

2.2.2 Video Data Input

The video data DIN[9:0] is clocked in to the GS9023A on the rising edge of PCLK. The video clock frequency must correspond to the video input standard selected. This can be done with the VM[2:0] and TRS input pins or selected via the "VSEL" bit of Host Interface Register #0h. When "VSEL" is set HIGH, the video input standard is selected by "VMOD[2:0]" and "D2_TRS" in Host Interface Register #0h. The supported video input standards are listed in Table 1.

After the user has specified the video input standard via the VM[2:0] and TRS pins or in Host Interface Register #0h, the GS9023A performs video standard detection to verify that the input video stream corresponds to the selected standard. The GS9023A then performs a 'lock' procedure, as selected by the "ACTSEL" bit of Host Interface Register #4h, to determine if the audio is synchronous to the video. When "ACTSEL" is LOW, the GS9023A counts the number of audio samples present in a frame or multiple frames, depending on the video standard selected. 'Lock' is achieved if the required number of samples are detected for 48kHz synchronous audio. When "ACTSEL" is HIGH, the GS9023A 'locks' by detecting the presence of an audio control packet corresponding to the DID configured in "ACID[3:0]" of Host Interface Register #4h and occurring at the expected line and position as listed in Table 6. If the video signal does not contain audio control packets, 'lock' will not occur. Once 'lock' is achieved the LOCK output pin and the "LOCK" bit of Host Interface Register #0h are set HIGH and audio demultiplexing begins. The LOCK output pin and the "LOCK" bit stay active regardless of the number of samples in the video stream after 'lock' is achieved. The GS9023A drops out of 'lock' when there are no more packets detected in the video stream.

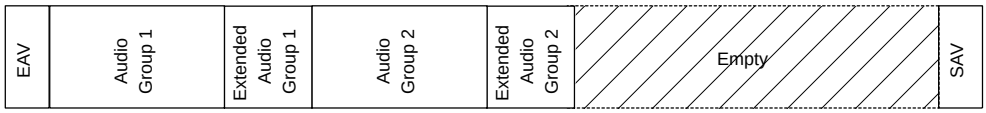
2.2.3 Video Data Output

The video signal is output at the $D_{OUT[9:0]}$ pins. The video signal is synchronized to the rising edge of PCLK. The GS9023A is capable of removing audio, extended audio, arbitrary and audio control packets from the video stream. To remove packets, the user must set the ANCI pin HIGH or set the “VSEL” and “ADEL” bits of Host Interface Register #0h HIGH. The GS9023A then removes each packet having a DID corresponding to either the audio DID, the extended audio DID or the arbitrary data DID stored in the Host Interface Registers from the video stream. See Figure 12.

NOTE: The GS9023A passes EDH packets through unchanged in the Demultiplex Mode. If any audio, extended audio, arbitrary or audio control packets are deleted by the GS9023A, the EDH CRC words become invalid.

When the ANCI pin or “ADEL” bit is LOW, all ancillary data packets remain in the video signal. See Figure 13.

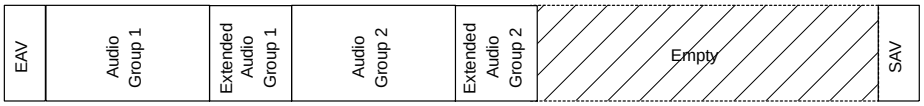
TRS can also be removed from a 525/625 D2 video signal when the TRS pin is set HIGH or the “VSEL” and “D2_TRS” bits of Host Interface Register #0h are set HIGH.



Video signal before GS9023A

Video signal after GS9023A Removal of Audio Group 1 & Extended Audio Group 1 (ANCI = HIGH or "VSEL" and "ADEL" = HIGH)

Figure 12



Video signal before GS9023A

Video signal after GS9023A Removal of Audio Group 1 & Extended Audio Group 1 (ANCI = LOW or "VSEL" = HIGH and "ADEL" = LOW)

Figure 13

2.2.4 Audio Clock Input

The user must input a master audio clock (128 fs: 6.144MHz) at the ACLK clock terminal. This clock must be synchronized with the video signal input to the GS9023A. The audio word clock inputs WC_{INA} and WC_{INB} must be grounded.

NOTE: The long term jitter present on the ACLK must be less than half the audio clock period.

2.2.5 Audio Data Output

The serial audio data for channels 1 and 2 are output at the A_{OUTA} pin. The serial audio data for channels 3 and 4 are output at the A_{OUTB} pin. Both outputs are synchronized to the rising edge of ACLK.

The GS9023A can demultiplex 20 or 24 bit audio data samples. When 24 bit audio samples are detected, the AUXEN pin and bit "A4ON" of Host Interface Register #1h are set HIGH. When 20 bit audio samples are detected the AUXEN pin and "A4ON" register bit are set LOW. When AUXEN and "A4ON" are LOW, bits 4-7 of the AES/EBU output data format are set to "0". In the non-AES/EBU formats, bits 0-3 are set to "0". See Figure 14.

The GS9023A offers five predefined audio data output formats, selected via the AM[2:0] pins, which are listed in Table 12 and illustrated in Figure 14. The first four predefined formats relate to non-AES/EBU audio data while the fifth format corresponds to the AES/EBU audio format. During reset, the audio outputs are forced LOW.

The GS9023A supports muting of the audio data outputs. The output serial audio samples are forced to zero when the MUTE pin or "MUTE" bit of Host Interface Register #4h are set HIGH. The audio data outputs are also muted when there is no video input signal.

TABLE 12 AUDIO OUTPUT FORMATS

FORMATS	WCOUT	AM[2]	AM[1]	AM[0]
AOUT-MODE 0	Active 48kHz	0	0	0
AOUT-MODE 1	Active 48kHz	0	0	1
AOUT-MODE 2	Active 48kHz	0	1	0
AOUT-MODE 3	Active 48kHz	0	1	1
AOUT-AES/EBU	-	1	0	0
Not Used	-	1	0	1
Not Used	-	1	1	0
Not Used	-	1	1	1

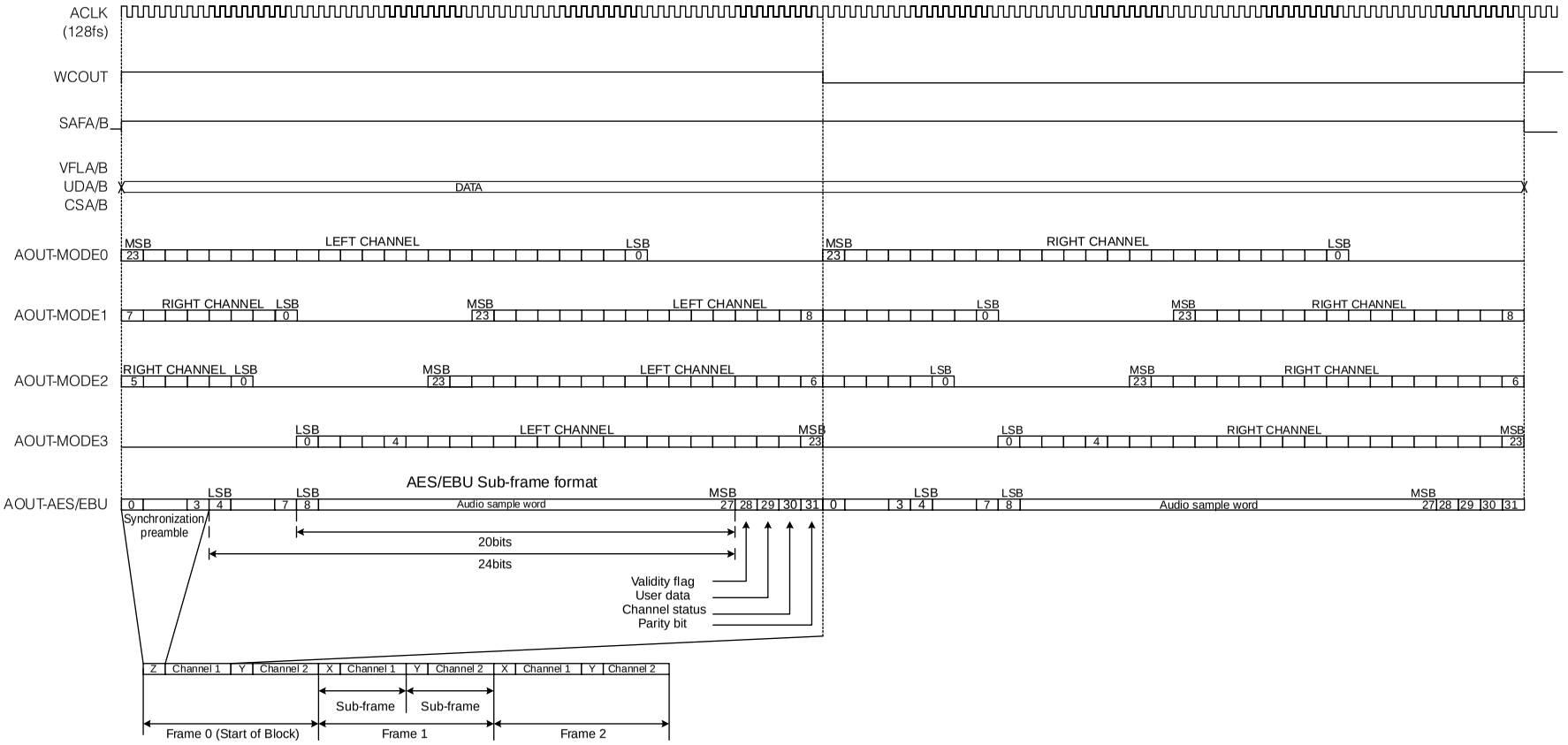


Figure 14 Audio Data Output Formats

2.2.6 Control Code Output

In the non-AES/EBU output formats, the V, U and C bits are output separately from the audio data stream. The bits are output respectively to the VFLA/B, UDA/B and CSA/B pins according to the channel pair to which they belong and change state on the rising edge of WCOUT. The SAFA/B output pins are set to HIGH for one audio frame out of 192 frames to mark the start of a block. In the AES/EBU audio output format, the respective pins are not used.

2.2.7 Detection of Audio Packets

The GS9023A can demultiplex up to four audio channels of an audio group. The audio group (Audio packet data ID) for each device is configured in "AD20ID[3:0]" of Host Interface Register #3h. When the corresponding audio packets are found on the active video line, the GS9023A sets the respective "CHACT(4-1)" bits of Host Interface Register #1h.

NOTE: When multiple audio groups are embedded in the video stream, the status bits "CHACT(4-1)" are only valid if the audio group being extracted immediately follows the EAV. If the audio group does not immediately follow the EAV, the device will still de-embed the audio correctly, however, the "CHACT(4-1)" bits will be invalid.

If no corresponding audio packets are found on the active video line, the "CHACT(4-1)" bits are set LOW.

By connecting four GS9023A devices in parallel, it is possible to demultiplex up to 16 audio channels in a component video signal as shown in Figure 15. On power up, audio group 1 is selected by default.

NOTE: When more than two channels of audio are embedded in an incoming audio data packet, audio samples from channel 1 must be embedded in either the 1st or 2nd sample position after the start of the audio data packet. Please refer to SMPTE 272M for details of the audio data packet formatting.

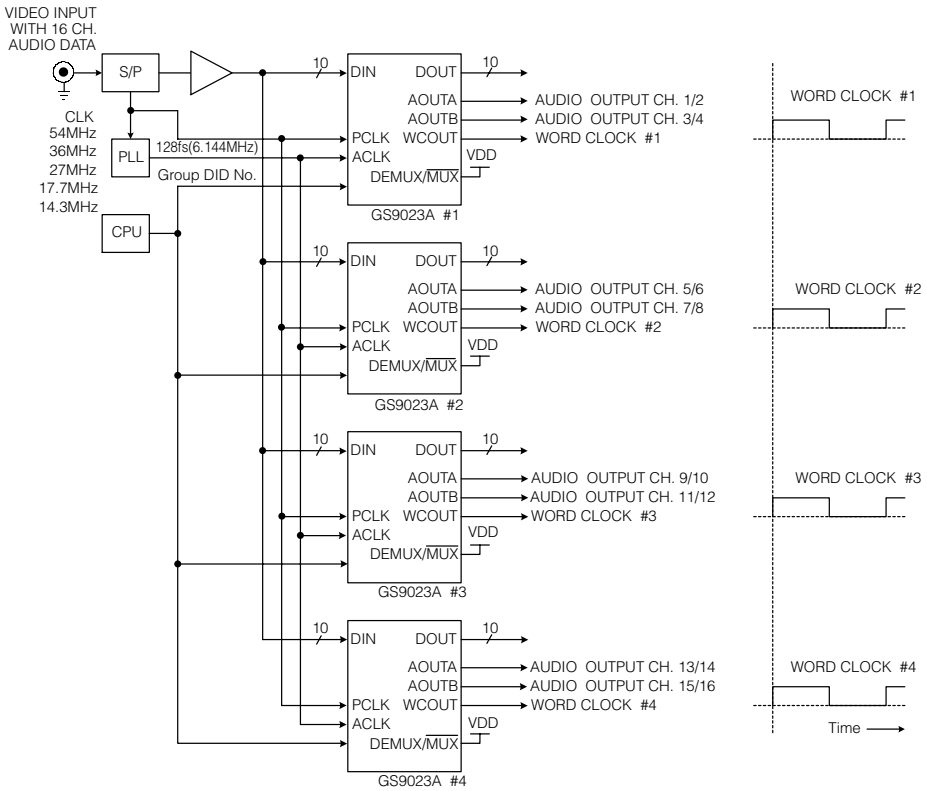


Figure 15 Demultiplex Mode Parallel Architecture

2.2.8 Detection of Extended Audio Packets

The GS9023A can demultiplex 20 or 24 bit audio samples. For 24 bit audio samples, the 20 MSBs of a 24 bit audio sample are contained in the audio data packets and the 4 LSBs are contained in an extended audio data packet as defined in SMPTE 272. The audio group (Extended packet data ID) for each device is configured in "AD4ID[3:0]" of Host Interface Register #3h. When the corresponding extended audio packets are detected on the active video stream, the GS9023A sets the AUXEN pin and the "A4ON" bit of Host Interface Register #1h to HIGH. If no corresponding extended audio packets are found on the active video line, the AUXEN pin and "A4ON" bit are set to LOW. On power up, audio group 1 extended audio packets are selected by default.

2.2.9 Detection of Audio Control Packets

The audio group (Audio control packet data ID) for each device is configured in "ACID[3:0]" of Host Interface Register #4h. When the configured ID is detected on the designated video lines (see Table 6), the "ACON" bit of Host Interface Register #1h is set. The corresponding Audio control parameters are stored in Host Interface Registers #Ah, #Bh, #Ch and #Dh. If an audio control packet is not detected or found in non-designated video lines, "ACON" is set to LOW. However, the information in the audio control packets found in non-designated lines is considered valid and is stored in Host Interface Registers #Ah, #Bh, #Ch and #Dh. On power up, audio group 1 audio control packets are selected by default.

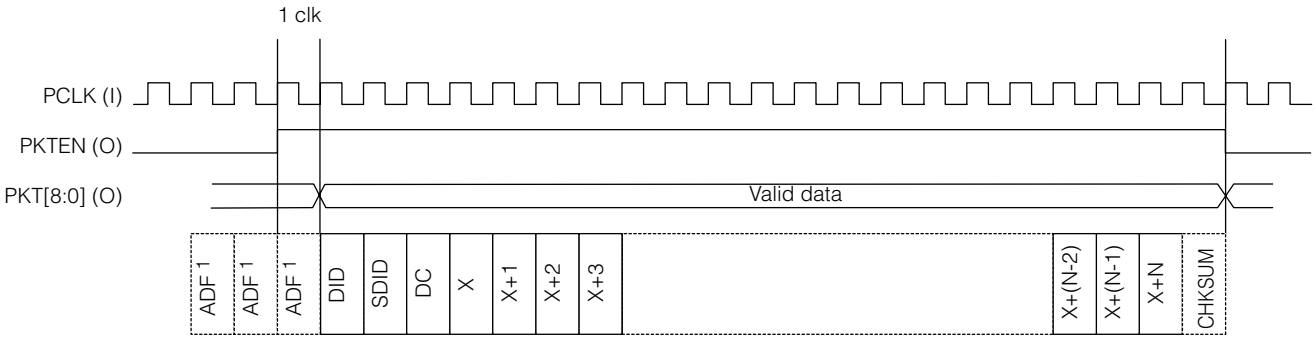
2.2.10 Detection and Output of Arbitrary Data Packets

The GS9023A is capable of demultiplexing arbitrary data packets according to SMPTE 291M. There are no limitations on the number of packets that can be demultiplexed and the packets can be located outside of the vertical blanking interval (VBI).

The arbitrary data packet data ID is configured in PKTID[7:0] of Host Interface Register #5h. When the configured ID is detected in the active video or HANC area, data on the PKT[8:0] pins is clocked out on the rising edge of PCLK. The GS9023A sets the PKTEN output pin HIGH, when the data at the PKT[8:0] outputs is valid. PKTEN is set LOW when the last user data word (UDW) is output from PKT[8:0]. Figure 16 shows the output timing.

2.2.11 Error Detection

The GS9023A provides error status information in Host Interface Registers #7h, #8h and #9h as described in Table 15. Register #7 contains error information on audio sampling and CRC conditions. Register #8 contains error information on audio packet data block number and data count. Register #9 contains error information on Control packets. Errors are cleared when the respective Host Interface Register is read.



NOTE: 1 - The ancillary data flag, ADF, is one word in composite systems (ANSI/SMPTE 259M) and three words in component systems (ANSI/SMPTE 125M).

Figure 16 Arbitrary Data Output Timing Diagram

2.3 MULTIPLEX AND DEMULTIPLEX MODES

2.3.1 Delay of Video and Audio

The GS9023A can be configured for various audio sample delays with respect to the video signal. The audio sample delay is selected in "BUFSEL[1:0]" of Host Interface Register #6h. Table 13 lists the various audio sample delays.

2.3.2 Non-Standard Sample Distributions

Gennum Corporation has made every effort to maximize compatibility of the GS9023A with other Embedded Audio data streams. Unfortunately, due to variations in implementations (i.e. non-standard sample distributions) Gennum cannot guarantee compatibility with all Embedded Audio data streams.

2.3.3 Host Interface

The Host Interface Registers allow for device configuration and provide status information. The GS9023A contains sixteen internal registers that are accessible through the Host Interface. Based on the mode of operation the registers have different functionality. In Multiplex Mode the registers are defined in Table 14 and in Demultiplex Mode the registers are defined in Table 15.

The asynchronous Host Interface consists of a 4 bit address bus (ADDR[3:0]), 8 bit data bus (DATA[7:0]), read enable ($\overline{RE}$), write enable ($\overline{WE}$) and chip select ($\overline{CS}$). The Host Interface access is independent of the PCLK or ACLK inputs. Read and write cycle timing is detailed in Figure 19.

In a read cycle, $\overline{CS}$ is driven LOW t_{AS} seconds after a valid address. $\overline{RE}$ is then driven LOW after t_{ACS} seconds for a minimum of t_{RD} seconds. After t_{GQV} seconds, the address register contents are output on the data bus. After a minimum of t_{RDH} seconds, $\overline{CS}$ is driven HIGH to end the cycle.

Similarly, in a write cycle, $\overline{CS}$ is driven LOW t_{AS} seconds after a valid address. $\overline{WE}$ is then driven low after t_{ACS} seconds for a minimum of t_{WD} seconds. Valid data must be present for a minimum of t_{DS} seconds before $\overline{WE}$ is driven HIGH again. After a minimum of t_{WDH} seconds, $\overline{CS}$ is driven HIGH to end the cycle.

2.3.4 Reset

Reset timing is detailed in Figure 20. Setting the $\overline{RESET}$ pin to LOW for a period of t_{RESET} seconds forces the audio outputs LOW and re-initializes the internal control circuitry including returning all Host Interface Register values to their original default values. The $\overline{RESET}$ pin can be used for synchronizing multiple devices.

2.3.5 Interconnection with GS9032 or GS7005

The user should pay special attention when laying out the GS9023A to operate with the GS9032 or GS7005. The MSB to LSB convention is consistent between the GS9023A and GS9022 but reversed with respect to the GS9032 or GS7005. Layout complexity can be minimized by placing the GS9023A and the GS9032 or GS7005 on opposite sides of the printed circuit board (PCB).

2.3.6 Audio Clock and Video Clock Stability in Multiplex Mode

Once the GS9023A is locked and processing audio, it is recommended that the audio clock frequency (ACLK at 128fs) remains stable and locked to video clock (VCLK). If VCLK is periodically switched or momentarily unstable, the audio clock phase locked loop circuit external to the GS9023A may be disrupted, causing ACLK to be at some arbitrary frequency. Under these conditions, operation of the GS9023A cannot be guaranteed and may result in corrupted audio. This is due to possible overflow/underflow condition occurring in the GS9023A internal FIFO, which is caused by the unstable audio clock input. If an overflow/underflow condition occurs, the "BUFSTAT" bit in Host Interface Register #2h will be set HIGH. The internal FIFO can be reset automatically by setting the "BUFCTRL" bit in Host Interface Register #2h HIGH.

2.3.7 Interconnection with GS9020

The TRS_INSERT function of the GS9020 should be disabled when operating with the GS9023A. This is controlled through the Host Interface of the GS9020 and through the CLIP_TRS pin. If enabled this may cause the GS9020 to continue outputting valid TRS codes even when the input signal is removed.The GS9023A may not detect this loss of video input and could remain locked. When a valid video signal is re-applied to the GS9020, the GS9023A's internal audio buffers may not have been reset and will therefore be in an overflow or underflow condition.

TABLE 13 AUDIO VIDEO DELAY

"BUFSEL[1:0]"	MODE	MULTIPLEX (US)	DEMULTIPLEX (US)	MULTIPLEX/DEMULTIPLEX CONNECTION (US)
0	(70 Sample)	875	541	1416
1	(26 Sample - Default)	250	312	563
2	(20 Sample)	187	250	437

1. NOTE: When the video signal is in D2 format, the delay is fixed at 70 samples (1416 us).

3. HOST INTERFACE TABLES

3.1 MULTIPLEX MODE

TABLE 14 MULTIPLEX MODE HOST INTERFACE REGISTERS

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
0h	2-0	VMOD[2:0]	Video standard selection. See Table 1. Valid when “VSEL” is HIGH. Used in conjunction with “D2_TRS”. “VMOD[2]” is the MSB and “VMOD[0]” is the LSB.	R/W	0
	3	LOCK	Lock indicator. Same functionality as the LOCK pin. When set HIGH, the video standard has been identified, the start of a new video frame has been detected and the device is ready to multiplex audio. NOTE: LOCK will not be set HIGH unless at least one of the “CHACT(4-1)” bits (Address #1h) is HIGH.	R	0
	4	EDHDEL	EDH data delete. When set LOW, existing EDH packets are removed from the video stream. When set HIGH, existing EDH packets are passed through unless overwritten via the EDH_INS pin or the “EDHON” bit. Valid only when “CASCADE” (Address #4h bit 7) is LOW.	R/W	0
	5	RSV	Not used.	–	–
	6	D2_TRS	TRS select. Same functionality as the TRS pin. Used to select video standard format.When set HIGH, TRS is added to a composite video signal. Valid only when “VSEL” is HIGH. Used in conjunction with “VMOD[2:0]”.	R/W	0
	7	VSEL	Video input format (external pin/internal register) configuration select. When set LOW, the video input format is configured via the VM[2:0] and TRS pins. When set HIGH, the video input format is configured via the “VMOD[2:0]” and “D2_TRS” bits.	R/W	0
1h	3-0	CHACT(4-1)	Audio channel enable. When set HIGH, the corresponding audio channel is multiplexed into the video signal. “CHACT(4)” is the MSB and “CHACT(1)” is the LSB. When set LOW, the GS9023A will not insert audio packets. NOTE: Do not rely on default value. Reprogram on power up or reset.	R/W	Fh
	4	ACON	Audio Control packet enable. When HIGH, the audio control packet is multiplexed in the video signal.	R/W	0
	5	EDHON	EDH packet enable. Same functionality as the EDH_INS pin. When set HIGH, the GS9023A performs EDH functions according to SMPTE RP165. NOTE: Active picture and full field data words are updated from recalculated values but error flag information is replaced with the values programmed in Host Interface Registers #Eh and #Fh.	R/W	0
	6	A4ON	Extended audio packet enable. Same functionality as the AUXEN pin. When set HIGH, the extended audio packet is multiplexed in the video signal (24 bit audio).	R/W	0
	7	PKON	Arbitrary data packet enable. When set HIGH, an arbitrary data packet is multiplexed in the video signal.	R/W	0

TABLE 14 MULTIPLEX MODE HOST INTERFACE REGISTERS (CONTINUED)

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
2h	0	REVISION	Device revision. When set HIGH, indicates the device is a GS9023A revision.	R	1
	1	BUFSTAT	Internal buffer status. When set HIGH, indicates that the internal audio sample buffer is in an overflow/underflow condition.	R	0
	2	VDET_MODE	Video detect mode. When set HIGH, the GS9023A will check the interval between the TRS on every line. If the interval is not consistent, the GS9023A assumes the input video has been switched and the internal audio sample buffer will be reset. Valid only when "RSEL" is set HIGH.	R/W	0
	3	8BIT_SEL	8-bit input selection. When set HIGH, the GS9023A will accept an 8-bit video input where DIN[9] is the MSB and DIN[2] is the LSB. DIN[1:0] should be set LOW. Valid only when "RSEL" is set HIGH.	R/W	0
	4	RSV	Not used.	-	
	5	MUTE_$\overline{A}$/M	Mute on buffer error mode. When set LOW, the GS9023A will automatically set the embedded audio packets to zero (MUTE) when BUFSTAT is HIGH. When set HIGH, the user is required to set the MUTE function on detection of BUFSTAT set HIGH. Valid only when "RSEL" is set HIGH. It is recommended that this bit is kept HIGH whenever the video input to the device may undergo a synchronous switch (see Section 2.1.2.1).	R/W	0
	6	BUFCTRL	Internal buffer control mode. When set HIGH, the GS9023A will automatically reset the internal audio sample buffer when an overflow/underflow condition is detected. When set LOW, the internal audio sample buffer will not be reset unless the user asserts a device RESET. Valid only when "RSEL" is set HIGH. It is recommended that this bit is kept HIGH whenever the video input to the device may undergo a synchronous switch (see Section 2.1.2.1).	R/W	0
	7	RSEL	Register select. When set HIGH, bits 2-6 of Host Interface register address #2h are valid.	R/W	0
3h	3-0	AD20ID[3:0]	Designates the 4 LSBs of the audio data packet DID word. The 6 MSBs are internally generated. “AD20ID[3]” is the MSB and “AD20ID[0]” is the LSB.	R/W	Fh
	7-4	AD4ID[3:0]	Designates the 4 LSBs of the extended audio data packet DID word. The 6 MSBs are internally generated. “AD4ID[3]” is the MSB and “AD4ID[0]” is the LSB.	R/W	Eh
4h	3-0	ACID[3:0]	Designates the 4 LSBs of the audio control packet DID word. The 6 MSBs are internally generated. “ACID[3]” is the MSB and “ACID[0]” is the LSB.	R/W	Fh
	4	RSV	Not used.	-	
	5	MUTE	Audio mute enable. Same functionality as the MUTE pin. When set HIGH, the multiplexed audio and extended data packets are forced to zero.	R/W	0
	6	AC34/12	Audio control packet channel pair select. When set HIGH, audio control packet delay data for audio channels 3 and 4 is captured in registers Ah, Bh, Ch and Dh. When set LOW, audio control packet delay data for audio channels 1 and 2 is captured in registers #Ah, #Bh, #Ch and #Dh.	R/W	0
	7	CASCADE	Cascade select. When set HIGH, the GS9023A device is part of a cascaded architecture. New packets are multiplexed into the video signal starting at the first free location of the HANC space if there is sufficient remaining space to insert the packet. When set LOW, new packets are multiplexed into the video signal starting after EAV. Existing ancillary data packets are overwritten and the remaining ancillary space is cleared.	R/W	0
5h	7-0	PKTID[7:0]	Designates the 8 LSBs of the arbitrary data packet DID word. The 2 MSBs are internally generated. “PKTID[7]” is the MSB and “PKTID[0]” is the LSB.	R/W	0
6h	1-0	BUFSEL[1:0]	Video/audio delay mode. “BUFSEL[1]” is the MSB and “BUFSEL[0]” is the LSB. See Table 13.	R/W	1h
	7-2	RSV	Not used.	-	
7h	0	ADERR	Audio data packet multiplexing error. The packet will not be multiplexed because of insufficient room in the HANC space. Error is cleared when read.	R	0
	1	ACERR	Audio control packet multiplexing error. The packet will not be multiplexed because of insufficient room in the HANC space. Error is cleared when read.	R	0
	7-2	RSV	Not used.	-	

TABLE 14 MULTIPLEX MODE HOST INTERFACE REGISTERS (CONTINUED)

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
8h	0	RSV	Not used.	-	
	1	PKTPRTY	Arbitrary data packet parity select. When set HIGH, a parity bit is generated for every user data word (UDW) of an arbitrary data packet. This overwrites any data input at the PKT[8] pin.	R/W	0
	5-2	RSV	Not used.	-	
	6	AXST1/2	Audio CH1/2 detection flag. When set HIGH, an audio signal has been detected.	R	0
	7	AXST3/4	Audio CH3/4 detection flag. When set HIGH, an audio signal has been detected.	R	0
9h	7-0	PKTLINE[7:0]	Arbitrary data packet insertion line. Designates the horizontal line on which the GS9023A can multiplex arbitrary data packets in the video signal.	R/W	0
Ah	7-0	DELA/B[7:0]	Audio control packet delay. Designates the audio control packet delay data as specified in the SMPTE 272M standard. “DELA” corresponds to audio channels 1 and 2, while “DELB” corresponds to audio channels 3 and 4. “DELA/B[25]” is the MSB and “DELA/B[0]” is the LSB.	R/W	0
Bh	7-0	DELA/B[15:8]		R/W	0
Ch	7-0	DELA/B[23:16]		R/W	0
Dh	1-0	DELA/B[25:24]		R/W	0
	2	ACSYNCA/B	Audio control packet synchronization data. Designates the sync mode bits (asx, asy), as defined in SMPTE 272M (Section 14.5), of channels 1/2 or 3/4 of the audio control packet. The bits are selected by “AC34/12” in register #4h.	R/W	0
	3	ACDLY	Audio control packet delay active. Designates the ‘e’ bit of word “DELx0” of an audio control packet as defined in SMPTE 272 (Section 14.7). When set HIGH indicates valid audio delay data.	R/W	0
	7-4	RSV	Not used.	-	
Eh	0	ANCI_EDH	EDH packet ancillary error flag. Error detected here.	R/W	0
	1	ANCI_EDA	EDH packet ancillary error flag. Error detected already.	R/W	0
	2	ANCI_IDH	EDH packet ancillary error flag. Internal error detected here.	R/W	0
	3	ANCI_IDA	EDH packet ancillary error flag. Internal error detected already.	R/W	0
	4	ANCI_UES	EDH packet ancillary error flag. Unknown error status.	R/W	0
	7-5	RSV	Not used.	-	
Fh	0	CRCEDH_A/B	EDH packet error flag. “CRCEDH_A” represents Full Field information. “CRCEDH_B” represents Active Picture information. *See “FF/AP_A/B” (bit 7).*	R/W	0
	1	CRCEDA_A/B	EDH packet error flag. “CRCEDA_A” represents Full Field information. “CRCEDA_B” represents Active Picture information. *See “FF/AP_A/B” (bit 7).*	R/W	0
	2	CRCIDH_A/B	EDH packet error flag. “CRCIDH_A” represents Full Field information. “CRCIDH_B” represents Active Picture information. *See “FF/AP_A/B” (bit 7).*	R/W	0
	3	CRCIDA_A/B	EDH packet error flag. “CRCIDA_A” represents Full Field information. “CRCIDA_B” represents Active Picture information. *See “FF/AP_A/B” (bit 7).*	R/W	0
	4	CRCUES_A/B	EDH packet error flag. “CRCUES_A” represents Full Field information. “CRCUES_B” represents Active Picture information. *See “FF/AP_A/B” (bit 7).*	R/W	0
	5	CRCVLD_A/B	EDH packet CRC valid flag. “CRCVLD_A” represents Full Field information. “CRCVLD_B” represents Active Picture information. *See “FF/AP_A/B” (bit 7).*	R/W	0
	6	RSV	Not used.	-	
	7	FF/AP_A/B	Full Field/Active Picture select. When set HIGH, the FF (Full Field) information is displayed in the above mentioned bits. When set LOW, the AP (Active Picture) information is displayed.	R/W	0

3.2 DEMULTIPLEX MODE

TABLE 15 DEMULTIPLEX MODE HOST INTERFACE REGISTERS

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
0h	2-0	VMOD[2:0]	Video standard selection. See Table 1. Valid when “VSEL” is HIGH. Used in conjunction with “D2_TRS”. “VMOD[2]” is the MSB and “VMOD[0]” is the LSB.	R/W	0
	3	LOCK	Lock indicator. Same functionality as the LOCK pin. When set HIGH, the video standard has been identified, the ‘lock’ process selected by “ACTSEL” has been validated and the device is ready to demultiplex audio. *See “ACTSEL” description.*	R	0
	4	ADEL	Ancillary data delete. Same functionality as the ANCI pin. When set HIGH, each ancillary data packet with a DID corresponding to either the audio packet DID, the extended audio packet DID or the arbitrary packet DID is removed from the video signal. When the “ADEL” bit is LOW, all ancillary data packets remain in the video signal. Valid only when “VSEL” is HIGH.	R/W	0
	5	RSV	Not used.	–	–
	6	D2_TRS	TRS select. Same functionality as the TRS pin. Used to select video standard format. When set HIGH, TRS is removed from a composite video signal. Valid only when “VSEL” is HIGH. Used in conjunction with “VMOD[2:0]”.	R/W	0
	7	VSEL	Video input format (external pin/internal register) configuration select. When set LOW, the video input format is configured via the VM[2:0] and TRS pins. When set HIGH, the video input format is configured via the “VMOD[2:0]” and “D2_TRS” bits.	R/W	0
1h	3-0	CHACT(4-1)	Active audio channel flags. When set HIGH, the corresponding audio packets have been detected on the active video line. When set LOW, no corresponding audio packets have been detected on the active video line. The flags are updated on every frame. NOTE: When multiple audio groups are embedded in a video signal, the GS9023A will only indicate the presence of the first audio group. All audio groups will be properly demultiplexed, but the indicators for multiple groups will not be set correctly.	R	0
	4	ACON	Audio Control packet flag. When set HIGH, the audio control packet has been detected in the video signal.	R	0
	5	EDHON	EDH flag. When set HIGH, EDH data has been detected in the video signal.	R	0
	6	A4ON	Extended audio packet flag. When set HIGH, the extended audio packet has been detected on the active video line (24 bit audio). When set LOW, no extended audio packet has been detected on the active video line (24 bit audio).	R	0
	7	RSV	Not used.	-	
2h	0	REVISION	Device revision. When set HIGH, indicates the device is a GS9023A revision.	R	1
	1	RSV	Not used.	-	
	2	VDET_MODE	Video detect mode. When set HIGH, the GS9023A will check the interval between the TRS on every line. If the interval is not consistent, the GS9023A assumes the input video has been switched and the internal audio sample buffer will be reset. Valid only when "RSEL" is set HIGH.	R/W	0
	3	RSV	Not used.	-	
	4	RSV	Not used.	-	
	5	RSV	Not used.	-	
	6	RSV	Not used.	-	
	7	RSEL	Register select. When set HIGH, bit 2 of Host Interface register address #2h is valid.	R/W	0

TABLE 15 DEMULTIPLEX MODE HOST INTERFACE REGISTERS (CONTINUED)

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
3h	3-0	AD20ID[3:0]	Designates the 4 LSBs of the audio data packet DID word. The 6 MSBs are internally generated. “AD20ID[3]” is the MSB and “AD20ID[0]” is the LSB.	R/W	Fh
	7-4	AD4ID[3:0]	Designates the 4 LSBs of the extended audio data packet DID word. The 6 MSBs are internally generated. “AD4ID[3]” is the MSB and “AD4ID[0]” is the LSB.	R/W	Eh
4h	3-0	ACID[3:0]	Designates the 4 LSBs of the audio control packet DID word. The 6 MSBs are internally generated. “ACID[3]” is the MSB and “ACID[0]” is the LSB.	R/W	Fh
	4	RSV	Not used.	-	
	5	MUTE	Audio mute enable. Same functionality as the MUTE pin. When set HIGH, the demultiplexed audio and extended packet data are forced to zero.	R/W	0
	6	ACTSEL	Audio lock process select. When set HIGH, the GS9023A ‘locks’ by detecting the presence of an audio control packet corresponding to the DID configured in “ACID[3:0]” and occurring at the expected line and position as listed in Table 6. When set LOW, the GS9023A ‘locks’ by counting the number of audio samples in a frame or multiple frames and validating the number of samples detected based on the video standard.	R/W	0
	7	RSV	Not used.	-	
5h	7-0	PKTID[7:0]	Designates the 8 LSBs of the arbitrary data packet DID word. The 2 MSBs are internally generated. “PKTID[7]” is the MSB and “PKTID[0]” is the LSB.	R/W	0
6h	1-0	BUFSEL[1:0]	Video/audio delay mode. “BUFSEL[1]” is the MSB and “BUFSEL[0]” is the LSB. See Table 13.	R/W	1h
	2	CRCADD	AES/EBU CRC select. When set HIGH, the C bit (channel status information) of each audio sample contains CRC information as defined in the AES3-1992 standard.	R/W	0
	7-3	RSV	Not used.	-	
7h	4-0	RSV	Not used.	-	
	5	SAMPERR	Sample error. Incorrect number of audio samples detected. 8008 audio samples (48kHz) in 5 video frames for a 525 line video format. 1920 audio samples (48kHz) in 1 video frame for a 625 line video format.	R	0
	6	ACRCERR1/2	Audio channel 1/2 CRC error.	R	0
	7	ACRCERR3/4	Audio channel 3/4 CRC error.	R	0
8h	0	A20DBNERR	Audio packet DBN error. A DBN discontinuity was detected.	R	0
	1	A20DCERR	Audio packet DC error. The number of UDW indicated does not match the number of words found in the data packet.	R	0
	2	RSV	Not used.	-	
	3	A20B9ERR	Audio packet inversion bit error. An incorrect bit 9 inversion of bit 8 was detected in the audio packet.	R	0
	7-4	RSV	Not used.	-	

TABLE 15 DEMULTIPLEX MODE HOST INTERFACE REGISTERS (CONTINUED)

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
9h	0	ACCDBNERR	Audio control packet DBN error. A DBN discontinuity was detected. NOTE: When a DBN discontinuity is detected, the VFLA/B pins remain valid (LOW).	R	0
	1	ACCDCERR	Audio control packet DC error. The number of UDW indicated does not match the number of words found in the audio control packet.	R	0
	3-2	RSV	Not used.	-	
	4	ACCB9ERR	Audio control packet inversion bit error. An incorrect bit 9 inversion of bit 8 was detected in the audio control packet.	R	0
	6-5	RSV	Not used.	-	
	7	A4B9ERR	Extended audio packet inversion bit error. An incorrect bit 9 inversion of bit 8 was detected in the extended audio packet.	R	0
Ah	7-0	DELA/B[7:0]	Audio control packet delay. Designates the audio control packet delay data as specified in the SMPTE 272M standard. DELA corresponds to audio channels 1 and 2, while DELB is the corresponds to audio channels 3 and 4. “DELA/B[25]” is the MSB and “DELA/B[0]” is the LSB.	R	0
Bh	7-0	DELA/B[15:8]		R	0
Ch	7-0	DELA/B[23:16]		R	0
Dh	1-0	DELA/B[25:24]		R	0
	2	ACSYNCA/B	Audio control packet synchronization data. Designates the sync mode bits (asx, asy) as defined in SMPTE 272M (section 14.5) of channels 1/2 or 3/4 of the audio control packet. The bits are selected by “AC34/12”.	R	0
	3	ACDLY	Audio control packet delay active. Designates the ‘e’ bit of word “DELx0” of an audio control packet as defined in SMPTE 272 (section 14.7). When HIGH indicates valid audio delay data.	R	0
	4	ACT1/2	Active channel 1/2 flag. Demultiplexed from the audio control packet, when present.	R	0
	5	ACT3/4	Active channel 3/4 flag. Demultiplexed from the audio control packet, when present.	R	0
	6	RSV	Not used.	-	
	7	AC34/12	Audio control packet and channel status channel pair select. When set LOW, the audio control packet delay data for audio channels 1 and 2 is captured in registers #Ah, #Bh, #Ch and #Dh. Registers #Eh and #Fh will display the channel status information for channels 1 and 2 respectively. When set HIGH, the audio control packet delay data for audio channels 3 and 4 is captured in registers #Ah, #Bh, #Ch and #Dh. Registers #Eh and #Fh will display the channel status information for channels 3 and 4 respectively.	R/W	0

TABLE 15 DEMULTIPLEX MODE HOST INTERFACE REGISTERS (CONTINUED)

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
Eh	0	CONPRO1/3	If AC34/12 bit of #Dh is set LOW AES/EBU channel 1 Consumer/Professional status. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 3 Consumer/Professional status. *See AES-3 1992 standard.*	R	0
	1	AUDMOD1/3	If AC34/12 bit of #Dh is set LOW AES/EBU channel 1 normal/non-audio status. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 3 normal/non-audio status. *See AES-3 1992 standard.*	R	0
	4-2	EMPH1/3[2:0]	If AC34/12 bit of #Dh is set LOW AES/EBU channel 1 emphasis status. “EMPH1/3[2]” is the MSB and “EMP1/3[0]” is the LSB. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 3 emphasis status. “EMPH1/3[2]” is the MSB and “EMP1/3[0]” is the LSB. *See AES-3 1992 standard.*	R	0
	5	SYNC1/3	If AC34/12 bit of #Dh is set LOW AES/EBU channel 1 sync status. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 3 sync status. *See AES-3 1992 standard.*	R	0
	7-6	FSEL1/3[1:0]	If AC34/12 bit of #Dh is set LOW AES/EBU channel 1 frequency select status. “FSEL1/3[1]” is the MSB and “FSEL1/3[0]” is the LSB. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 3 frequency select status. “FSEL1/3[1]” is the MSB and “FSEL1/3[0]” is the LSB. *See AES-3 1992 standard.*	R	0

TABLE 15 DEMULTIPLEX MODE HOST INTERFACE REGISTERS (CONTINUED)

ADDRESS	BIT	NAME	FUNCTION	R/W	DEFAULT
Fh	0	CONPRO2/4	If AC34/12 bit of #Dh is set LOW AES/EBU channel 2 Consumer/Professional status. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 4 Consumer/Professional status. *See AES-3 1992 standard.*	R	0
	1	AUDMOD2/4	If AC34/12 bit of #Dh is set LOW AES/EBU channel 2 normal/non-audio status. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 4 normal/non-audio status. *See AES-3 1992 standard.*	R	0
	4-2	EMPH2/4[2:0]	If AC34/12 bit of #Dh is set LOW AES/EBU channel 2 emphasis status. “EMPH2/4[2]” is the MSB and “EMP2/4[0]” is the LSB. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 4 emphasis status. “EMPH2/4[2]” is the MSB and “EMP2/4[0]” is the LSB. *See AES-3 1992 standard.*	R	0
	5	SYNC2/4	If AC34/12 bit of #Dh is set LOW AES/EBU channel 2 sync status. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 4 sync status. *See AES-3 1992 standard.*	R	0
	7-6	FSEL2/4[1:0]	If AC34/12 bit of #Dh is set LOW AES/EBU channel 2 frequency select status. “FSEL2/4[1]” is the MSB and “FSEL2/4[0]” is the LSB. If AC34/12 bit of #Dh is set HIGH AES/EBU channel 4 frequency select status. “FSEL2/4[1]” is the MSB and “FSEL2/4[0]” is the LSB. *See AES-3 1992 standard.*	R	0

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
I/O Supply Voltage	-0.3 to 7.0V
Internal Supply Voltage	-0.3 to 4.0V
Input Voltage (any input)	-0.3 to V_{DDIO} + 0.5V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	230°C

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Supply Voltage	V_{DDIO}	5V Operating range	4.75	5.00	5.25	V
I/O Supply Current	I_{DDIO}	V_{DDIO} = 5V; PCLK = 54.0 MHz		25		mA
I/O Supply Current	I_{DDIO}	V_{DDIO} = 5V; PCLK = 27.0 MHz		18		mA
I/O Supply Voltage	V_{DDIO}	3.3V Operating range	3.00	3.30	3.60	V
Internal Supply Voltage	V_{DDINT}		3.00	3.30	3.60	V
Internal Supply Current	I_{DDINT}	PCLK = 54.0 MHz		67		mA
Internal Supply Current	I_{DDINT}	PCLK = 27.0 MHz		37		mA
Input Current	I_{IN}		-1	-	1	µA
Hi-Z Output Leakage Current	I_{OZ}		-1	-	1	µA
Output Voltage, Logic High	V_{OH}	I_{OH} = -3mA	V_{DDIO} - 0.4	-	-	V
Output Voltage, Logic Low	V_{OL}	I_{OL} = 3mA	-	-	0.4	V
Input Voltage, Logic High	V_{IH}	V_{DDIO} = Max (5.25V or 3.6V)	2.0	-	-	V
Input Voltage, Logic Low	V_{IL}	V_{DDIO} = Min. (4.75V or 3.0V)	-	-	0.8	V
Input Capacitance	C_I	f = 1MHz, V_{DDIO} = 0V	-	-	10	pF
Output Capacitance	C_O	f = 1MHz, V_{DDIO} = 0V	-	-	10	pF
I/O Capacitance	C_{IO}	f = 1MHz, V_{DDIO} = 0V	-	-	10	pF

AC ELECTRICAL CHARACTERISTICS

V_{DDIO} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Video Clock Frequency			-	-	54	MHz
Video Clock Pulse Width Low	t_{PWL}		7.4	-	-	ns
Video Clock Pulse Width High	t_{PWH}		7.4	-	-	ns
Video Input Data Setup Time	t_S		3	-	-	ns
Video Input Data Hold Time	t_H		1	-	-	ns
Video Output Data Delay Time	t_{OD}	with 10 pF loading	-	-	13	ns
Video Output Data Hold Time	t_{OH}	with 10 pF loading	3	-	-	ns
Audio Clock Frequency			-	-	6.144	MHz
Audio Input Data Setup Time	t_s		3	-	-	ns
Audio Input Data Hold Time	t_H		1	-	-	ns
Audio Output Data Hold Time	t_{OH}	with 10pF loading	3	-	-	ns
Audio Output Data Delay Time	t_{OD}	with 10pF loading	-	-	13	ns
Address set up time	t_{AS}		3	-	-	ns
Chip select set up time	t_{ACS}		3	-	-	ns
Read data access time	t_{GQV}		-	-	10	ns
Read data enable time	t_{GQLZ}		1	-	-	ns
Read data hold time	t_{RDH}		1	-	-	ns
Read pulse width	t_{RD}		20	-	-	ns
Read cycle time	t_{RC}		30	-	-	ns
Write data set up time	t_{DS}		3	-	-	ns
Write data hold time	t_{WDH}		1	-	-	ns
Write pulse width	t_{WD}		20	-	-	ns
Write cycle time	t_{WC}		30	-	-	ns
Reset Pulse Width	t_{RESET}		1	-	-	us
Device Latency		Multiplexer Mode Demultiplexer Mode	13 10	13 10	13 10	PCLKs

NOTE: The following signals have the same AC electrical characteristics as the audio inputs and outputs: WCINA, WCINB, SAFA, SAFB, VFLA, VFLB, UDA, UDB, CSA, CSB, WCOUTA, WCOUTB.

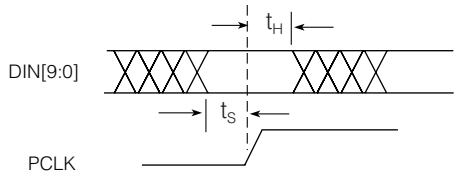


Figure 17 Video Data Input Setup & Hold Times

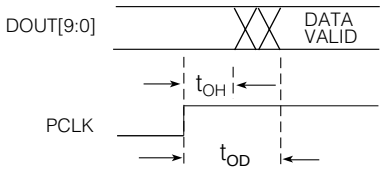


Figure 18 Video Data Output Delay & Hold Times

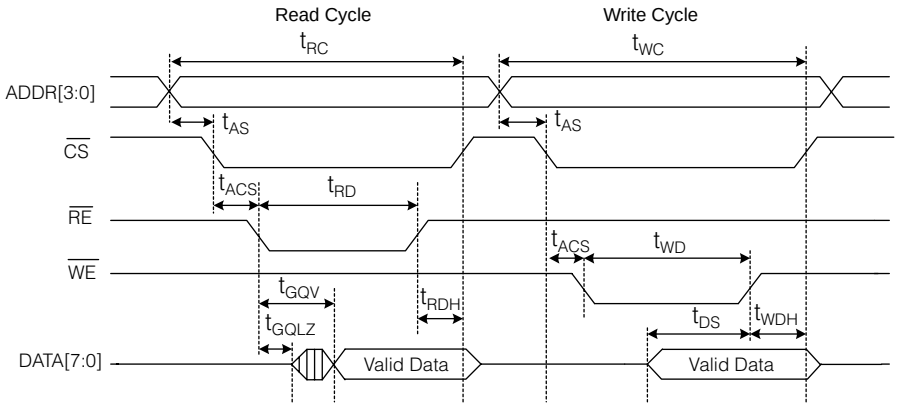


Figure 19 Host Interface Timing Diagram

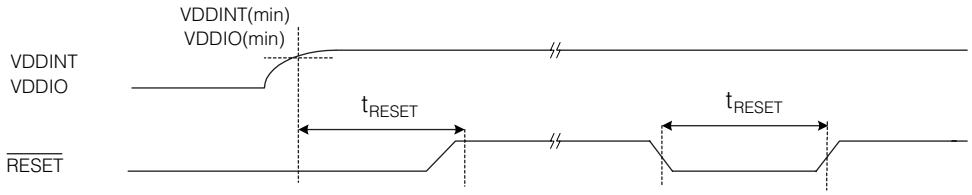
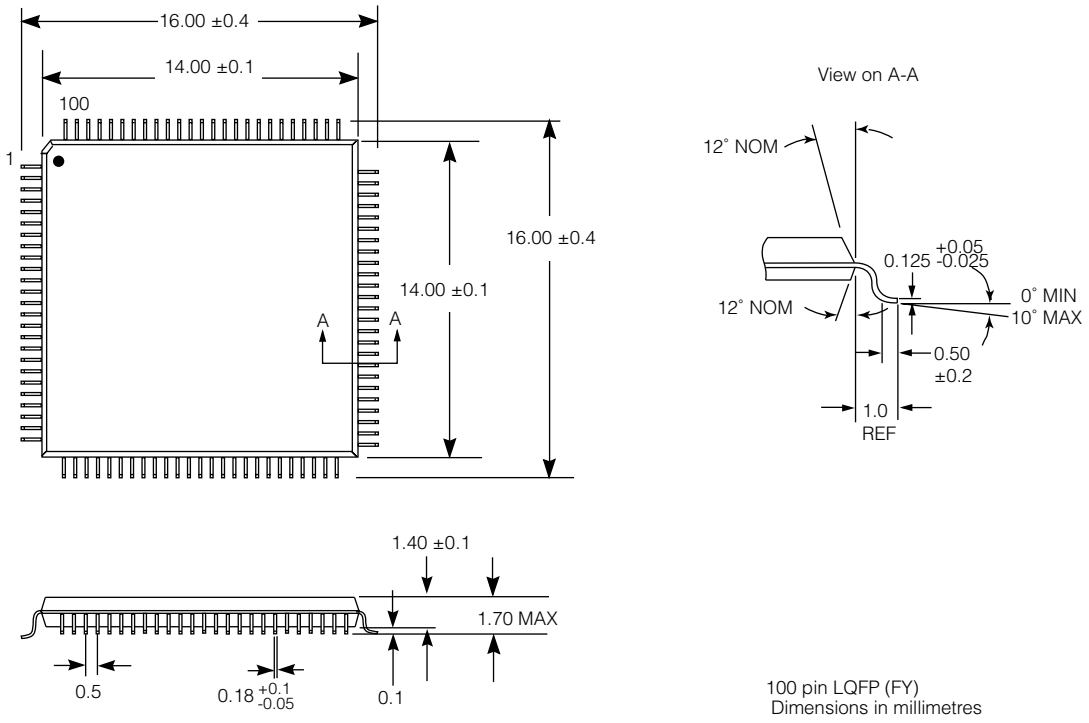


Figure 20 Reset Timing Diagram

4. PACKAGING INFORMATION



100 pin LQFP (FY)
Dimensions in millimetres

5. REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
5	131679	September 2003	Added Section 2.1.2.1. Added Section 5. Discussed possible timing discrepancy when using multiple GS9023As to multiplex several audio channels. Expanded description of 'CHACT(4-1)' bits in demultiplex mode. Modified host interface register #Dh, #Eh, and #Fh descriptions (demultiplex mode only).
6	133575	May 2004	Removed VXST bit from register Oh of the host interface.Modified Section 2.1.5 and Section 2.2.7.

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