GENNUM

GS9092A GenLINX® III 270Mb/s Serializer for SDI and DVB-ASI

GS9092A Data Sheet

Key Features

- SMPTE 259M-C compliant scrambling and NRZI to NRZ encoding (with bypass)
- DVB-ASI sync word insertion and 8b/10b encoding
- Integrated Cable Driver
- Integrated line-based FIFO for data alignment/delay, clock phase interchange, DVB-ASI data packet insertion, and ancillary data packet insertion
- User selectable additional processing features including:
  - ANC data checksum, and line number calculation and insertion
  - TRS and EDH packet generation and insertion
  - illegal code remapping
- Enhanced Gennum Serial Peripheral Interface (GSPI)
- JTAG test interface
- +1.8V internal cable driver and core power supply
- Optional +1.8V or +3.3V digital I/O power supply
- Small footprint (8mm x 8mm)
- Low power operation (typically 200mW)
- Pb-free and RoHS compliant

Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS9092A is a 270Mb/s serializer with an internal FIFO and an integrated cable driver. It contains all the necessary blocks to realize a transmit solution for SD-SDI and DVB-ASI applications.

In addition to serializing the input data stream, the GS9092A performs NRZI-to-NRZ encoding and scrambling as per SMPTE 259M-C when operating in SMPTE mode. When operating in DVB-ASI mode, the device will insert K28.5 sync characters and 8b/10b encode the data prior to serialization.

Parallel data inputs are provided for 10-bit multiplexed formats at SD signal rates. A 27MHz parallel clock input signal is also required.

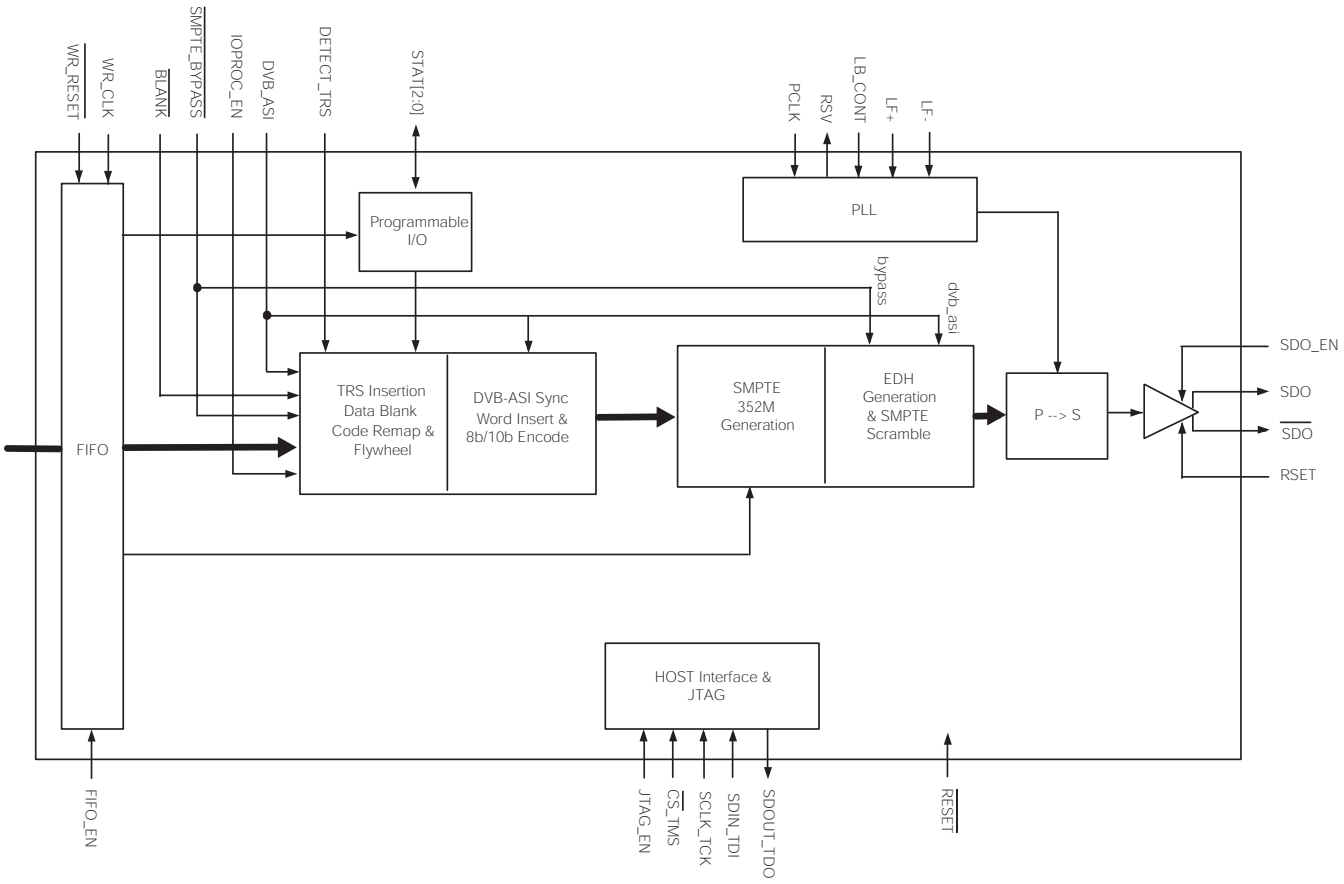
The integrated cable driver features an adjustable signal swing and common mode operating point offering fully compliant SMPTE 259M-C cable driver connectivity.

The GS9092A includes a range of data processing functions such as automatic standards detection and EDH support. The device can also insert TRS signals, re-map illegal code words, and generate and insert SMPTE 352M payload identifier packets. All processing features are optional and may be enabled/disabled via external control pin(s) and/or host interface programming.

The GS9092A also incorporates a video line-based FIFO. This FIFO may be used in four user-selectable modes to carry out tasks such as data delay, clock phase interchange, MPEG packet insertion and clock rate interchange, and ancillary data packet insertion.

The device may also be used as a low-latency parallel-to-serial converter where the SMPTE scrambling block will be the only processing feature enabled.

The GS9092A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS compliant).



GS9092A Functional Block Diagram

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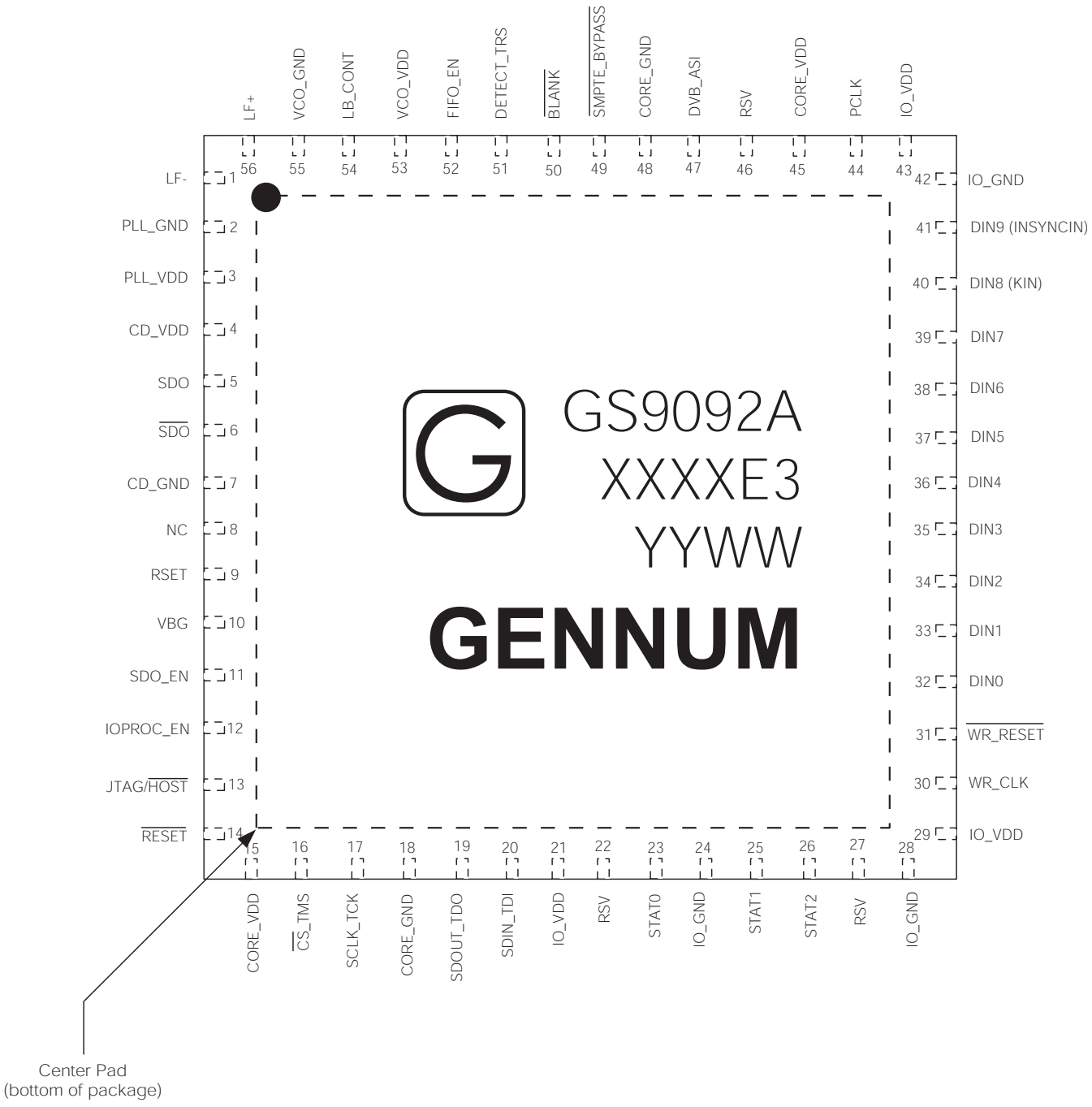
1. Pin Out

1.1 Pin Assignment



1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	LF-	Analog	Input	Loop filter component connection. Connect to LF+ through a capacitor. See Typical Application Circuit on page 56.
2	PLL_GND	Analog	Input Power	Ground connection for phase-locked loop. Connect to GND.
3	PLL_VDD	Analog	Input Power	Power supply connection for phase-locked loop. Connect to +1.8V DC.
4	CD_VDD	Analog	Input Power	Power supply connection for serial digital cable driver. Connect to +1.8V DC
5, 6	SDO, $\overline{\text{SDO}}$	Analog	Output	Serial digital differential output pair. NOTE: these output signals will be forced into a mute state if $\overline{\text{RESET}}$ is LOW.
7	CD_GND	Analog	Input Power	Ground connection for serial digital cable driver. Connect to GND.
8	NC	–	–	No connect.
9	RSET	Analog	Input	An external 1% resistor connected between this input and CD_VDD is used to set the SDO / $\overline{\text{SDO}}$ output amplitude.
10	VBG	Analog	Input	Bandgap filter capacitor. Connect as shown in the Typical Application Circuit on page 56
11	SDO_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible Used to enable or disable the serial digital output. When set LOW by the application layer, the serial digital output signals SDO and $\overline{\text{SDO}}$ are muted. When set HIGH by the application layer, the serial digital output signals are enabled. SDO and $\overline{\text{SDO}}$ outputs will also be high impedance when the $\overline{\text{RESET}}$ pin is LOW.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
12	IOPROC_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal Levels are LVCMOS / LVTTL compatible. Used to enable or disable the I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • SMPTE 352M Payload Identifier Packet Generation and Insertion • Illegal Code Remapping • EDH Generation and Insertion • Ancillary Data Checksum Insertion • TRS Generation and Insertion To enable a subset of these features, keep the IOPROC_EN pin HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When this pin is set LOW, the device will enter low-latency mode. NOTE: When the internal FIFO is configured for video mode or ancillary data insertion mode, the IOPROC_EN pin must be set HIGH.
13	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.
14	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to reset the internal operating conditions to default setting or to reset the JTAG test sequence. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): When asserted LOW, all functional blocks will be set to default conditions ,SDO and $\overline{\text{SDO}}$ are muted, and all input signals become high impedance with the exception of the STAT pins which will be driven LOW. When set HIGH, normal operation of the device resumes 10usec after the LOW-to-HIGH transition of the $\overline{\text{RESET}}$ signal. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes. NOTE: For power on reset requirements please see Device Power Up on page 55.
15, 45	CORE_VDD	Non Synchronous	Input Power	Power supply for digital logic blocks. Connect to +1.8V DC. NOTE: For power sequencing requirements please see Device Power Up on page 55.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
16	$\overline{CS}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{HOST}$ = LOW): $\overline{CS}$/TMS operates as the host interface chip select, $\overline{CS}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): $\overline{CS}$/TMS operates as the JTAG test mode select, TMS, and is active HIGH. NOTE: If this pin is unused it should be pulled up to VCC_IO.
17	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Clock / Test Clock. All JTAG / Host Interface address and data is shifted into / out of the device synchronously with this clock. Host Mode (JTAG/$\overline{HOST}$ = LOW): SCLK_TCK operates as the host interface serial data clock, SCLK. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): SCLK_TCK operates as the JTAG test clock, TCK. NOTE: If this pin is unused it should be pulled up to VCC_IO.
18, 48	CORE_GND	Non Synchronous	Input Power	Ground connection for digital logic blocks. Connect to GND.
19	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{HOST}$ = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.
20	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Input / Test Data Input Host Mode (JTAG/$\overline{HOST}$ = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): SDIN_TDI operates as the JTAG test data input, TDI. NOTE: If this pin is unused it should be pulled up to VCC_IO.
21, 29, 43	IO_VDD	Non Synchronous	Input Power	Power supply for digital I/O. For a 3.3V tolerant I/O, connect pins to either +1.8V DC or +3.3V DC. For a 5V tolerant I/O, connect pins to a +3.3V DC. NOTE: For power sequencing requirements please see Device Power Up on page 55.
22, 27	RSV	–	–	Reserved. Do Not Connect.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
23, 25, 26	STAT[2:0]	Synchronous with PCLK or WR_CLK	Input/Output	MULTI FUNCTION I/O PORT Signal levels are LVCMOS / LVTTL compatible. Programmable multi-function I/O. By programming the bits in the IO_CONFIG register, each pin can act as an output for one of the following signals: • H • V • F • FIFO_FULL • FIFO_EMPTY Each pin may also act as an input for an external H, V, or F signal if the DETECT_TRS pin is set LOW by the application layer These pins are set to certain default values depending on the configuration of the device and the internal FIFO mode selected. See Programmable Multi-function I/O on page 48 for details.
24, 28, 42	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O. Connect to GND.
30	WR_CLK		Input	FIFO WRITE CLOCK Signal levels are LVCMOS / LVTTL compatible. The application layer clocks the parallel data into the device on the rising edge of WR_CLK when the internal FIFO is configured for video mode or DVB-ASI mode. NOTE: If this pin is unused it should be pulled up to GND.
31	WR_RESET	Synchronous with WR_CLK	Input	FIFO WRITE RESET Signal levels are LVCMOS / LVTTL compatible. Valid input only when the device is in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH, DVB-ASI = LOW) and the internal FIFO is configured for video mode (Video Mode on page 23). A HIGH to LOW transition will reset the FIFO write pointer to address zero of the memory. NOTE: If this pin is unused it should be pulled up to GND.
32 - 41	DIN[9:0]	Synchronous with WR_CLK or PCLK	Input	PARALLEL VIDEO DATA BUS Signal levels are LVCMOS / LVTTL compatible. When the internal FIFO is enabled and configured for either video mode or DVB-ASI mode, parallel data will be clocked into the device on the rising edge of WR_CLK. When the internal FIFO is in bypass mode, parallel data will be clocked into the device on the rising edge of PCLK. DIN9 is the MSB and DIN0 is the LSB.
44	PCLK		Input	PIXEL CLOCK INPUT Signal levels are LVCMOS / LVTTL compatible. 27MHz parallel clock input.
46	RSV	–	–	Reserved. Do Not Connect.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
47	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH by the application layer, the device will be configured for the transmission of DVB-ASI data.The setting of the $\overline{\text{SMPTE\_BYPASS}}$ pin will be ignored. When set LOW by the application layer, the device will not support the encoding of DVB-ASI data.
49	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When set LOW, the device will not support the scrambling, encoding or packet insertion of received SMPTE data. No I/O processing features will be available and the device will enter a low-latency mode.
50	BLANK	Synchronous with PCLK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Functional only when chip is in SMPTE mode. When set LOW by the application layer, the luma and chroma input data is set to the appropriate blanking levels (TRS words will be unaltered at all times) When set HIGH by the application layer, the input data will pass into the device unaltered.
51	DETECT_TRS	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select external H,V, and F timing mode or TRS extraction timing mode. When set LOW by the application layer, the device will extract all internal timing from the supplied H, V, and F timing signals. When set HIGH by the application layer, the device will extract all internal timing from the TRS signals embedded in the supplied video stream. The H, V, and F signals will become outputs that can be accessed via the STAT[2:0] pins. Both 8-bit and 10-bit TRS code words will be identified by the device.
52	FIFO_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable / disable the internal FIFO. When FIFO_EN is HIGH, the internal FIFO will be enabled. Data will be clocked into the device on the rising edge of the WR_CLK input pin if the FIFO is in video mode or DVB-ASI mode. When FIFO_EN is LOW, the internal FIFO is bypassed and parallel data is clocked into the device on the rising edge of the PCLK input.
53	VCO_VDD	Analog	Input Power	Power supply connection for Voltage-Controlled-Oscillator. Connect to +1.8V DC.
54	LB_CONT	Analog	Input	CONTROL SIGNAL INPUT Control voltage to fine-tune the loop bandwidth of the PLL.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
55	VCO_GND	Analog	Input Power	Ground connection for Voltage-Controlled-Oscillator. Connect to GND.
56	LF+	Analog	Input	Loop filter component connection. Connect to LF- through a capacitor. See Typical Application Circuit on page 56.
–	Center Pad	–	Power	Connect to GND following recommendations in Recommended PCB Footprint on page 58.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +3.47V
Input Voltage Range (any input)	-2.0V to +5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
ESD protection on all pins (see Note 1)	500 V

NOTES:

1. HBM, per JESDA - 114B

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Operating Temperature Range	T_A	–	0	25	70	°C	1
Core power supply voltage	CORE_VDD	–	1.71	1.8	1.89	V	–
Digital I/O Buffer Power Supply Voltage	IO_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	IO_VDD	3.3V Operation	3.13	3.3	3.47	V	–
PLL Power Supply Voltage	PLL_VDD	–	1.71	1.8	1.89	V	–
VCO Power Supply Voltage	VCO_VDD	–	1.71	1.8	1.89	V	–
Serial Cable Driver Power Supply Voltage	CD_VDD	–	1.71	1.8	1.89	V	–
Typical System Power	P_D	CORE_VDD = 1.80V IO_VDD = 1.80V	–	200	–	mW	–
Max. System Power	P_D	CORE_VDD = 1.89V IO_VDD = 3.47V	–	–	300	mW	–
Digital I/O							
Input Voltage, Logic LOW	V_{IL}	1.8V or 3.3V Operation	–	–	0.35 x IO_VDD	V	–
Input Voltage, Logic HIGH	V_{IH}	1.8V or 3.3V Operation	0.65 x IO_VDD	–	–	V	–
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 8mA @ 3.3V, 4mA @ 1.8V	–	–	0.4	V	–
Output Voltage, Logic HIGH	V_{OH}	I_{OL} = -8mA @ 3.3V, -4mA @ 1.8V	IO_VDD - 0.4	–	–	V	–
Serial Digital Outputs							
Output Common Mode Voltage Range	V_{CMOUT}	1.8V Pull-Up Reference Voltage	–	CD_VDD - V_{ODIFF}	–	V	–
Serial Driver Output Voltage Swing	V_{SDO}	1.8V Pull-up Reference Voltage, Single Ended 75Ω load	0	–	850	mV_{p-p}	2

Table 2-1: DC Electrical Characteristics (Continued)

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Output Voltage Variation From Nominal	–	Over cable driver voltage supply range. RSET = 281Ω (800mV$_{p-p}$ single ended output)	-8.5	–	+8.5	%	–
	–	Output voltage variation from nominal (at 1.8V). RSET = 281Ω (800mV$_{p-p}$ single ended output)	-5	–	+5	%	–

NOTES

1. All DC and AC electrical parameters within specification.
2. Set by the value of the RSET resistor.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Output High Impedance Response Time	t_{RHIGHZ}	SDO_EN = HIGH to LOW	–	20	–	ns	–
Digital I/O							
Input Data Setup Time	t_{SU}	50% PCLK vs. V_{IL}/V_{IH} data	3.0	–	–	ns	1
Input Data Hold Time	t_{IH}	50% PCLK vs. V_{IL}/V_{IH} data	1.0	–	–	ns	1
Output Data Hold Time	t_{OH}	With 15pF load	3.0	–	–	ns	2
Output Delay Time	t_{OD}	With 15pF load	–	–	11.0	ns	2

Table 2-2: AC Electrical Characteristics (Continued)

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Serial Digital Output							
Serial Output Data Rate	BR_{SDO}		–	270	–	Mb/s	–
Serial Output Additive Jitter		270Mb/s, V_{SDO} = 800mV, 75Ω load including rise/fall mismatch	–	360	555	ps pk-pk	3
Serial Output Rise Time (20% ~ 80%)	SDO_{TR}	Return loss compensation recommended circuit - SMPTE 259M signal	400	500	1000	ps	–
Serial Output Fall Time (20% ~ 80%)	SDO_{TF}	Return loss compensation recommended circuit - SMPTE 259M signal	400	500	1000	ps	–
Mismatch in Rise/Fall Time	–	V_{ODIFF} = 1600mV, 100Ω differential load	–	–	30	ps	–
Serial Output Overshoot	–	V_{ODIFF} = 1600mV, 100Ω differential load	–	0	8	%	–
Output Return Loss	ORL	@ 270Mb/s Using Gennum Evaluation board. Measured at the BNC with matching network.	15	–	–	dB	4, 5
Output Capacitance	C_{OUT}	Including pin and bonding parasitics	–	–	5	pF	–
GSPI							
GSPI Input Clock Frequency	f_{GSPI}	–	–	–	54.0	MHz	–
GSPI Clock Duty Cycle	DC_{GSPI}	–	40	–	60	%	–
GSPI Setup Time	t_{GS}	–	1.5	–	–	ns	–
GSPI Hold Time	t_{GH}	–	–	–	1.5	ns	–

NOTES

1. Timing includes the following inputs: DIN[9:0], H, V, F, WR_CLK, $\overline{\text{WR\_RESET}}$, $\overline{\text{BLANK}}$. When the FIFO is enabled, the following signals are measured with respect to WR_CLK: $\overline{\text{WR\_RESET}}$, DIN[9:0], INSSYNCIN, KIN.
2. Refers to when H, V, and F are output pins
3. Measured using pseudorandom bit sequence (2^{23}-1) over full input voltage range.
4. 5MHz to 270MHz.
5. See 'Output Return Loss Measurement" on page 46.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1. The recommended standard eutectic reflow profile is shown in Figure 2-2.

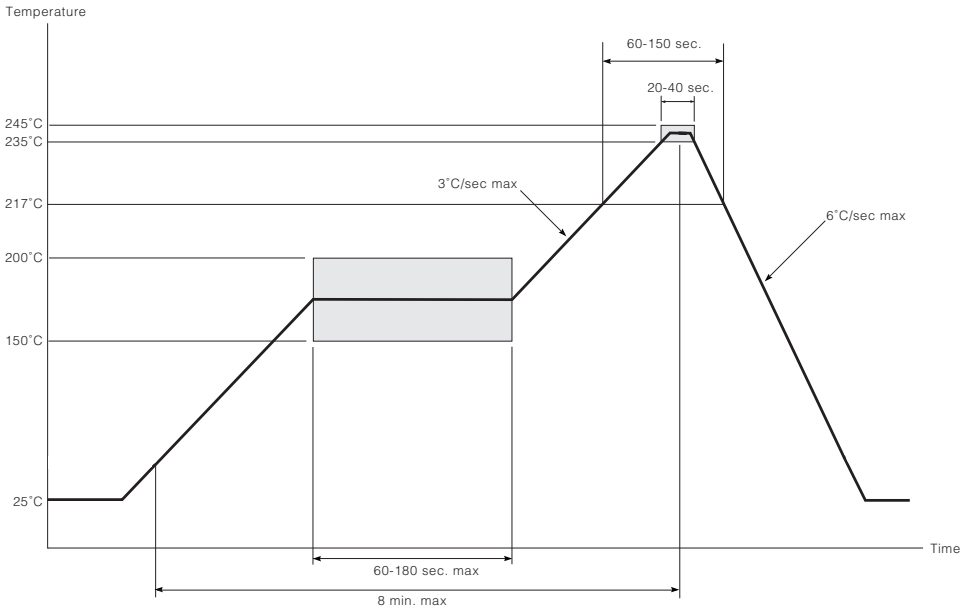


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

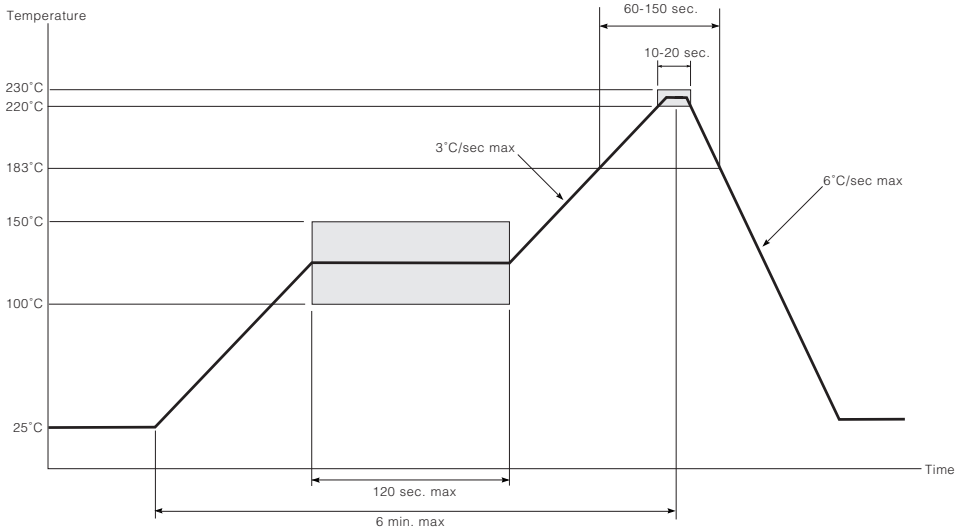


Figure 2-2: Standard Pb Solder Reflow Profile (Pb-free package)

2.5 Host Interface Maps

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANC_WORDS[10:0]	28h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_2[10:0]	27h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_1[10:0]	26h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	25h																
FF_PIXEL_END_F1[12:0]	24h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4[10:0]	14h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_B	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_A	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
ANC_LINE_B[10:0]	09h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h	Not Used	Not Used	ANC_ DATA_ RDBACK	ANC_ FIFO_ READY	ANC_ DATA_ REPLACE	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	ANC_SAV	ANC_ DATA_ SWITCH	Not Used	Not Used	Not Used	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
VIDEO_STANDARD	04h	Not Used	Not Used	Not Used	Not Used	EDH_CRC_U PDATE	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	STD_ LOCK	Not Used	Not Used	Not Used	Not Used
	03h																
EDH_FLAG	02h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	01h																
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	ANC_PKT_ INS	FIFO_ MODE b1	FIFO_ MODE b0	H_ CONFIG	352M_ CALC	352M_ INS	ILLEGAL_ REMAP	EDH_CRC_ INS	ANC_ CSUM_ INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. These registers may be written to in Ancillary Data Insertion mode (see Section 3.3.3)

2.5.1 Host Interface Map (Read only registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28h																
	27h																
	26h																
	25h																
	24h																
	23h																
	22h																
	21h																
	20h																
	1Fh																
	1Eh																
	1Dh																
	1Ch																
	1Bh																
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
RASTER_STRUCTURE4[10:0]	14h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	10h																
	0Fh																
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
	09h																
	08h																
	07h																
FIFO_EMPTY_OFFSET	06h				ANC_ FIFO_ READY												
	05h																
VIDEO_STANDARD	04h												STD_ LOCK				
	03h																
	02h																
	01h																
	00h																

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. These registers may be written to in Ancillary Data Insertion mode (see Section 3.3.3)

2.5.2 Host Interface Map (R/W configurable registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANC_WORDS[10:0]	28h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_2[10:0]	27h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_1[10:0]	26h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	25h																
FF_PIXEL_END_F1[12:0]	24h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	14h																
	13h																
	12h																
	11h																
VIDEO_FORMAT_B	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_A	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
ANC_LINE_B[10:0]	09h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_EMPTY_OFFSET	06h			ANC_ DATA_ RDBACK		ANC_ DATA_ REPLACE		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	ANC_SAV	ANC_ DATA_ SWITCH	Not Used	Not Used	Not Used	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
VIDEO_STANDARD	04h	Not Used	Not Used	Not Used	Not Used	EDH_CRC_U PDATE	Not Used	Not Used									
	03h																
EDH_FLAG	02h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	01h																
IOPROC_DISABLE	00h							ANC_PKT_ INS	FIFO_ MODE b1	FIFO_ MODE b0	H_ CONFIG	352M_ CALC	352M_ INS	ILLEGAL_ REMAP	EDH_CRC_ INS	ANC_ CSUM_ INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. These registers may be written to in Ancillary Data Insertion mode (see Section 3.3.3).

3. Detailed Description

3.1 Functional Overview

The GS9092A is a 270Mb/s serializer with an internal FIFO and a programmable multi-function I/O port. The device has 3 different modes of operation which must be set by the application layer through external device pins.

When SMPTE mode is enabled, the device will accept 10-bit multiplexed SMPTE compliant data at 27MHz. The device's additional processing features are also enabled in this mode.

In DVB-ASI mode, the GS9092A will accept an 8-bit parallel DVB-ASI compliant transport stream. The serial output data stream will be 8b/10b encoded and padded with K28.5 fill characters.

The GS9092A's third mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams.

The serial digital outputs feature a high impedance mode and adjustable signal swing.

In the digital signal processing core, several data processing functions are implemented including SMPTE 352M and EDH data packet generation and insertion, and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

The provided programmable multi-function I/O pins may be configured to input and output various status signals including H, V, and F timing, a FIFO_FULL, and a FIFO_EMPTY pulse. The internal FIFO supports 4 modes of operation, which may be used for data delay, MPEG packet insertion, or ancillary data insertion.

Finally, the GS9092A contains a JTAG interface for boundary scan test implementations.

3.2 Parallel Data Inputs

Data inputs enter the device on the rising edge of either PCLK or WR_CLK, depending on the configuration of the internal FIFO.

When the internal FIFO is bypassed or in ancillary data insertion mode (see Ancillary Data Insertion Mode on page 28), data enters the device on the rising edge of PCLK as shown in Figure 3-1. When the internal FIFO is configured for video mode, data enters the device on the rising edge of WR_CLK (see Video Mode on page 23).

The input data format is defined by the setting of the external $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins (Table 3-1). Input data must be presented in 10-bit format.

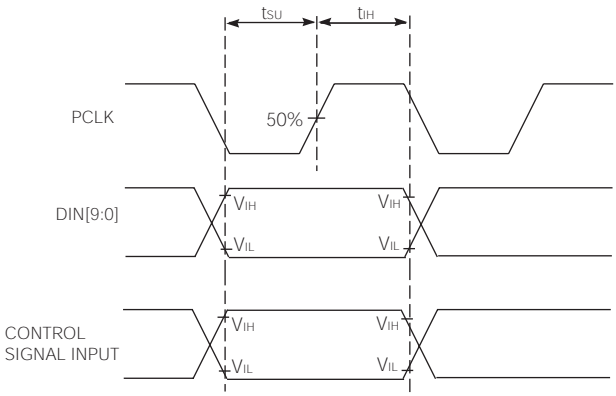


Figure 3-1: PCLK to Input Data Timing

NOTE: For a SMPTE compliant serial output, the jitter on the input PCLK across the frequency spectrum should not exceed 350ps.

3.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode (see SMPTE Mode on page 32), SD data is presented to the input bus in 10-bit multiplexed format. The input data format must be word aligned, multiplexed luma and chroma data.

NOTE: When operating the device in an 8-bit SMPTE system, the 2 LSBs (DIN [1:0]) must be set to 0.

Table 3-1: Input Data Format Selection

		Pin Settings	
Input Data Format	**DIN[9:0]**	**$\overline{\text{SMPTE\_BYPASS}}$**	**DVB_ASI**
10-bit Data	DATA	LOW	LOW
10-bit Multiplexed SD	Luma/Chroma	HIGH	LOW
10-bit DVB-ASI	DVB-ASI data	X	HIGH

3.2.2 Parallel Input in DVB-ASI Mode

When operating in DVB-ASI mode (see DVB-ASI Mode on page 33), the device will accept 8-bit data words on DIN[7:0] such that DIN7 = HIN is the most significant bit of the encoded transport stream data and DIN0 = AIN is the least significant bit.

In addition, DIN9 and DIN8 will be configured as the DVB-ASI control signals INSSYNCIN and K_IN respectively. See Control Signal Inputs on page 33 for a description of these DVB-ASI specific input signals.

3.2.3 Parallel Input in Data-Through Mode

When operating in Data-Through mode (see Data-Through Mode on page 34), the GS9092A passes data presented to the parallel input bus to the serial output without performing any encoding, scrambling, or word-alignment.

3.2.4 I/O Buffers

The parallel data bus, status signal outputs, and control signal input pins are all connected to high-impedance buffers. These buffers use either +1.8V or +3.3V DC, supplied at the IO_VDD and IO_GND pins. For a +3.3V tolerant I/O, the IO_VDD pins can be connected to either +1.8V or +3.3V. For a +5V tolerant I/O, the IO_VDD pins must be supplied with +3.3V.

While $\overline{\text{RESET}}$ is LOW, STAT output pins are muted and all other output pins become high impedance.

3.3 Internal FIFO Operation

The GS9092A contains an internal video line-based FIFO, which can be programmed by the application layer to work in any of the following modes:

1. Video Mode
2. DVB-ASI Mode
3. Ancillary Data Insertion Mode
4. Bypass Mode

The FIFO can be configured to one of the four modes by setting the FIFO_MODE[1:0] bits of the IOPROC_DISABLE register via the host interface (see Table 3-4 in Packet Generation and Insertion on page 35). The setting of these bits is shown in Table 3-2. To enable the FIFO, the application layer must also set the FIFO_EN pin HIGH. Additionally, if the FIFO is configured for video mode or ancillary data insertion mode, the IOPROC_EN pin must be set HIGH.

The FIFO is fully asynchronous, allowing simultaneous read and write access. It has a depth of 2048 words, and can store up to 1 full line of SD video for both 525 and 625 standards.

NOTE: The F, V, and H signals will be ignored when the FIFO is configured for DVB-ASI mode or bypass mode.

Table 3-2: FIFO Configuration Bit Settings

FIFO Mode	FIFO_MODE[1:0] Register Setting	FIFO_EN Pin Setting	IOPROC_EN Pin Setting
Video Mode	00b	HIGH	HIGH
DVB-ASI Mode	01b	HIGH	X
Ancillary Data Insertion Mode	10b	HIGH	HIGH
Bypass Mode	11b	X	X

NOTE: 'X' signifies 'don't care'. The pin is ignored and may be set HIGH or LOW.

3.3.1 Video Mode

The internal FIFO is in video mode under the following conditions:

- the FIFO_EN and IOPROC_EN pins are set HIGH,
- the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register (Table 3-4) are configured to 00b,
- the DETECT_TRS pin is set LOW; and
- TRS insertion, EDH correction/insertion, illegal code re-mapping, and SMPTE packet insertion are all disabled (i.e. bits 0, 2, 3, and 4 of the IOPROC_DISABLE register are set HIGH).

NOTE: The FIFO will still enter video mode if any of bits 0, 2, 3, or 4 of the IOPROC_DISABLE register are LOW; however, the output video data will contain errors.

By default, the FIFO_MODE[1:0] bits are set to 00b by the device whenever the $\overline{\text{SMPTE\_BYPASS}}$ pin is set HIGH and the DVB_ASI and DETECT_TRS pins are set LOW.

In video mode, the H, V, and F pins become input signals that must be supplied by the user.

Figure 3-2 shows the input and output signals of the FIFO when it is configured for video mode.

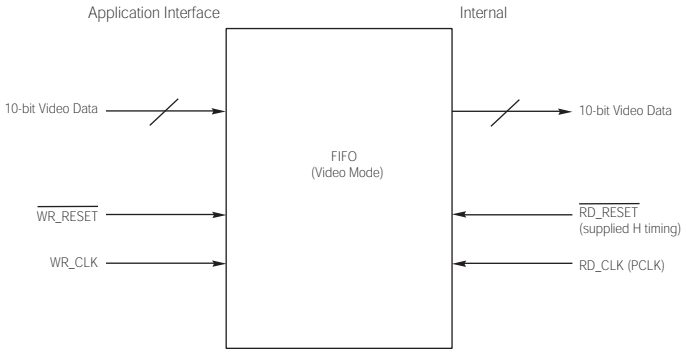


Figure 3-2: FIFO in Video Mode

When operating in video mode, the GS9092A will read data sequentially from the FIFO, starting with the first active pixel in location zero of the memory. In this mode, it is possible to use the FIFO for clock phase interchange and data delay.

The device will ensure read-side synchronization is maintained, according to the supplied PCLK and supplied H, V, and F timing information.

Full write-control of the FIFO is made available to the application interface such that data is clocked into the FIFO on the rising edge of the externally provided WR_CLK. The FIFO write pointer will be reset to position zero of the memory when there is a HIGH-to-LOW transition at the $\overline{\text{WR\_RESET}}$ pin.

The application layer must start writing the first active pixel of the line into location zero of memory. Therefore, the user should use the $\overline{\text{WR\_RESET}}$ pin to reset the FIFO write pointer prior to writing to the device.

NOTE: The $\overline{\text{BLANK}}$ signal must not be asserted in video mode.

3.3.2 DVB-ASI Mode

The internal FIFO is in DVB-ASI mode when the application layer sets the FIFO_EN pin HIGH and the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 01b. By default, the FIFO_MODE[1:0] bits are set to 01b by the device whenever the DVB_ASI pin is set HIGH (i.e. the device is in DVB-ASI mode); however, the application layer may program the FIFO_MODE[1:0] bits as required.

Figure 3-3 shows the input and output signals of the FIFO when it is configured for DVB-ASI Mode.

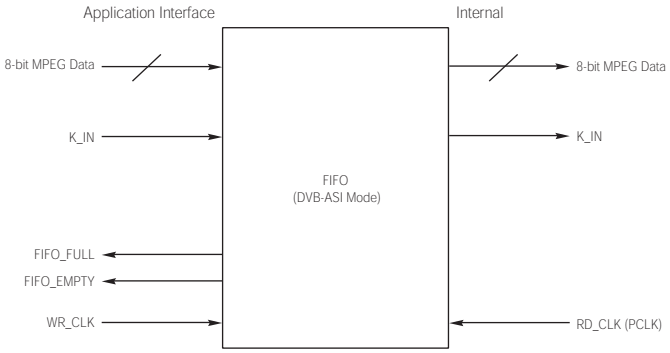


Figure 3-3: FIFO in DVB-ASI Mode

When operating in DVB-ASI mode, the GS9092A's FIFO can be used for clock rate interchange operation. 8-bit MPEG data as well as a K_IN control signal must be written to the FIFO by the application layer. The MPEG data and control signal can be simultaneously clocked into the FIFO at any rate using the rising edge of the WR_CLK pin.

The 8-bit MPEG data stream may consist of only MPEG packets, or both MPEG packets and special characters (such as the K28.5 stuffing characters). The application layer must set K_IN HIGH whenever a special character is present in the data stream, otherwise it should be LOW. The GS9092A uses the K_IN signal to determine whether or not a given byte in the FIFO is an MPEG packet that needs 8b/10b encoded.

The INSSYNCIN pin should be grounded while operating the FIFO in DVB-ASI mode.

The GS9092A internally reads the data out of the FIFO at the PCLK rate and adds the necessary number of stuffing characters based on the FIFO status flags.

3.3.2.1 FIFO Status Flags

The FIFO contains internal read and write pointers used to designate which spot in the FIFO the MPEG data will be read from or written to. These internal pointers control the status flags FIFO_FULL and FIFO_EMPTY, which are available for output on the multi-function I/O pins if so programmed (see Programmable Multi-function I/O on page 48).

In the case where the write pointer is originally ahead of the read pointer, the FIFO_EMPTY flag will be set HIGH when both pointers arrive at the same address (see box A of Figure 3-6). When the FIFO_EMPTY flag goes HIGH, the device will insert K28.5 stuffing data bytes.

To allow larger K28.5 packet sizes to be inserted, a write pointer offset can be programmed into the FIFO_EMPTY_OFFSET[9:0] register of the host interface. If an offset value is programmed in this register, the FIFO_EMPTY flag is set HIGH when the read and write pointers of the FIFO are at the same address, and will remain HIGH until the write pointer reaches the programmed offset. While the FIFO_EMPTY flag is HIGH, the device will continue to insert stuffing characters. Once the pointer offset has been exceeded, the FIFO_EMPTY flag will go LOW and the device will begin reading MPEG data out of the FIFO (see box B of Figure 3-6).

In the case where the read pointer is originally ahead of the write pointer, the FIFO_FULL flag will be set HIGH when both pointers arrive at the same address (see box C of Figure 3-6). The application layer can use this flag to determine when to write to the device.

A read and write pointer offset may also be programmed in the FIFO_FULL_OFFSET[9:0] register of the host interface. If an offset value is programmed in this register, the FIFO_FULL flag will be set HIGH when the read and write pointers of the FIFO are at the same address, and will remain set HIGH until the read pointer reaches the programmed offset. Once the pointer offset has been exceeded, the FIFO_FULL flag will be cleared (see box D of Figure 3-6).

NOTE: When the FIFO is configured for DVB-ASI mode, the INSSYNCIN pin is unused, as synchronization characters are inserted based on the FIFO status flags. The pin should be grounded. When the internal FIFO is bypassed in DVB-ASI mode, the INSSYNCIN input assumes normal operation as described in Control Signal Inputs on page 33.

Gating the WR_CLK Using the FIFO_FULL Flag

Using the asynchronous FIFO_FULL flag to gate the WR_CLK requires external clock gating circuitry to generate a clean burst clock (see Figure 3-4). An example circuit for this application is shown in Figure 3-5.

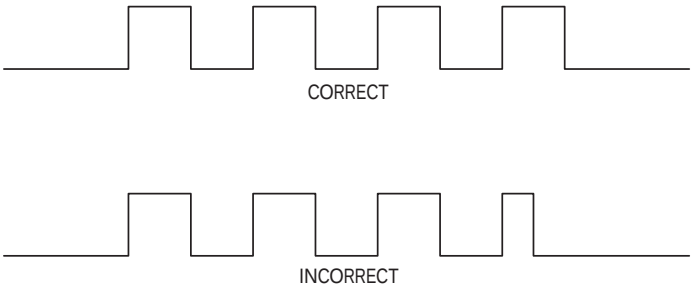


Figure 3-4: Burst Clock

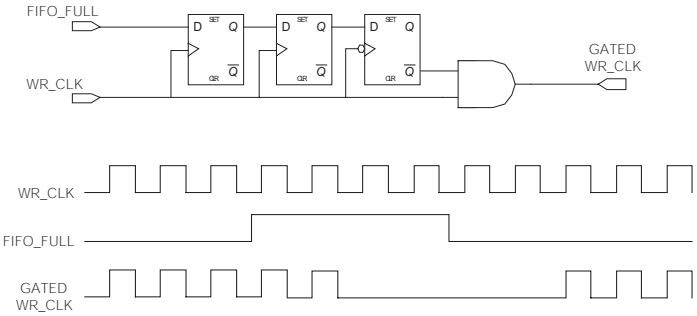


Figure 3-5: Example Circuit to Gate WR_CLK Using the FIFO_FULL Flag

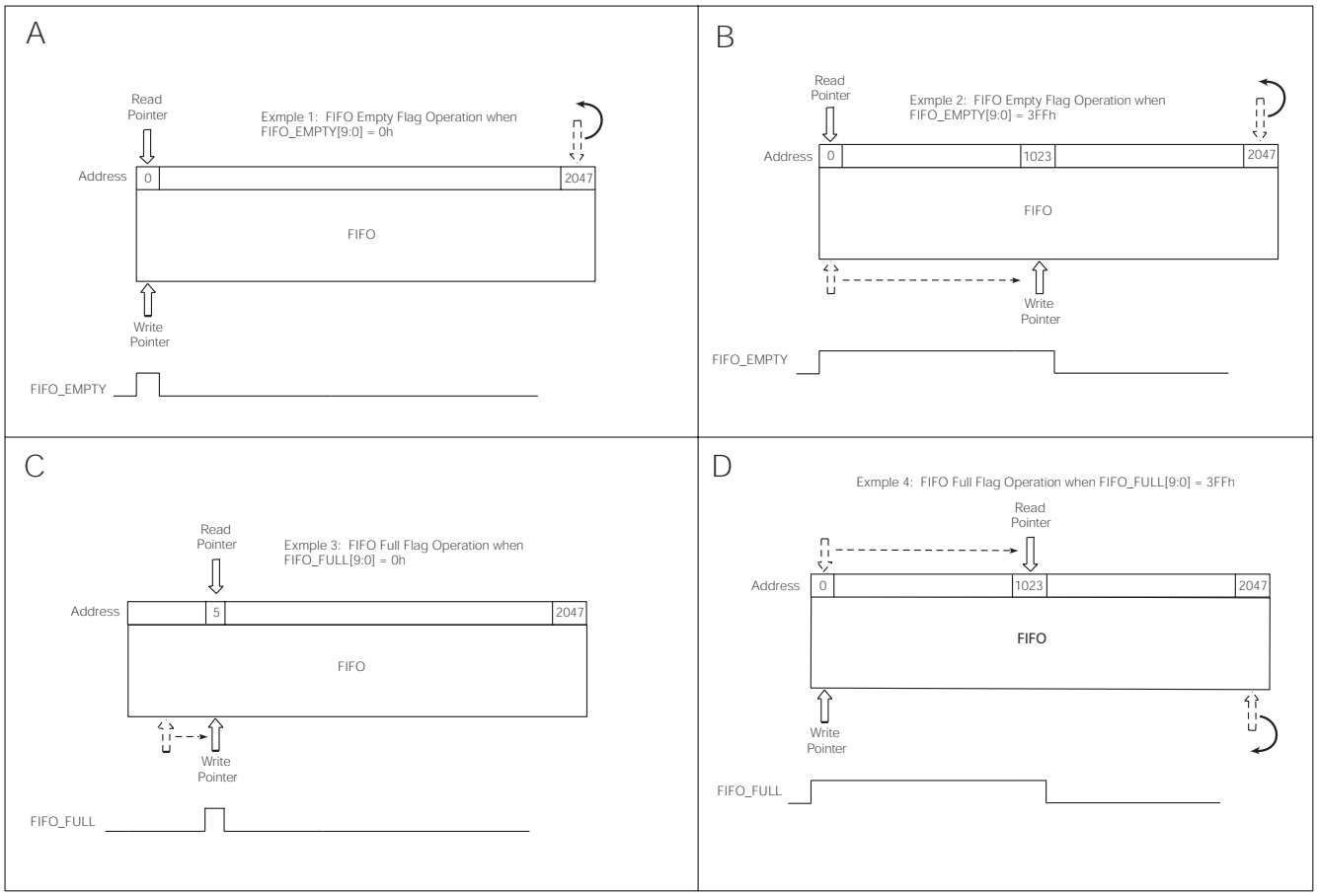


Figure 3-6: FIFO Status Flag Operation in DVB-ASI Mode

3.3.3 Ancillary Data Insertion Mode

The internal FIFO is in ancillary data insertion mode when the application layer sets the FIFO_EN and IOPROC_EN pins HIGH, and the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 10b.

In this mode, the FIFO is divided into two separate blocks of 1024 words each. To insert ancillary data into the video stream, the internal PLL must be locked to the input PCLK.

Once the FIFO enters ancillary data insertion mode, there is a 2200 PCLK cycle (82us) initialization period before the application layer may write ancillary data into the FIFO. The device will set the ANC_FIFO_READY bit HIGH (bit 12 of address 06h) once this initialization period has passed.

The following steps, which may be completed in any order, are required before ancillary data is inserted into the data stream:

1. Starting at the first address of the FIFO (address 02Ch), the application layer must program the contents of the ancillary data packets to be inserted into the FIFO via the host interface. A maximum of 1024 8-bit words are allowed. The entire packet, including the ancillary data flag (ADF), data identification (DID), secondary data identification (SDID) if applicable, data count (DC), and checksum word must be written into memory. The user may write an arbitrary value (FFh for example) for the checksum word, which will act as a place holder. The actual checksum will be calculated and inserted by the device prior to insertion into the data stream. The GS9092A will also generate bit 8 and 9 for all words in the FIFO (as described in SMPTE 291M) prior to insertion. Note that no ancillary data can be written to the FIFO until the device has set the ANC_FIFO_READY bit HIGH.
2. The number of words to be inserted (i.e. the number of words written into the FIFO), must be programmed in the ANC_WORDS[10:0] register by the application layer. If the total number of words to be inserted exceeds the available space, the ancillary data will be inserted up to the point where the available space is filled.
3. The line(s) in which the packets are to be inserted must be programmed into the ANC_LINE_A[10:0] and/or ANC_LINE_B[10:0] registers. Up to two lines per frame may have ancillary data packets inserted in them. If only one line number register is programmed, ancillary data packets will be inserted in one line per frame only. The GS9092A will insert ancillary data into the designated line(s) during every frame.
4. The application layer must set the ANC_SAV bit of the IO_CONFIG register (address 05h) either HIGH or LOW. By default, the ANC_SAV bit will be LOW and the ancillary data will be inserted into the horizontal ancillary data space at the first available location after the EAV. If the ANC_SAV bit is set HIGH, the ancillary data is written instead immediately after the SAV on the line programmed. If an active video line is programmed into the ANC_LINE_A[10:0] or ANC_LINE_B[10:0] register, the active video data will be overwritten when ANC_SAV is set HIGH.

Once the above steps are completed, the application layer may set the ANC_PKT_INS bit of the IOPROC_DISABLE register HIGH (see Table 3-4 in Packet Generation and Insertion on page 35) to enable insertion of the prepared ancillary packets into the video data stream. Ancillary data packets will be inserted in the following frame after the ANC_PKT_INS bit has been set HIGH.

NOTE: When inserting ancillary data into the blanking region, the total number of words cannot exceed the size of the blanking region, and the data count value in the packet must be correct.

3.3.3.1 Ancillary Data Insertion

Once the ANC_PKT_INS bit is set HIGH, the device will start reading the user programmed ancillary packets out of the FIFO and insert them into the video stream. Subsequent ancillary packets programmed by the application layer will continue to be placed into the first half of the FIFO until the ANC_DATA_SWITCH bit is toggled (see block A of Figure 3-7).

By default, the ANC_DATA_SWITCH bit of the IO_CONFIG register is set LOW. When ANC_DATA_SWITCH is toggled from LOW to HIGH, any new ancillary data the application layer programs will be placed in the second half of the FIFO. The device will continue to insert ancillary data from the first half of the FIFO into the video stream (see block B of Figure 3-7).

Once the ancillary data in the first half of the FIFO has been inserted into the video stream, ANC_DATA_SWITCH may be toggled again. This will clear the first half of the FIFO and begin insertion of ancillary data from the second half of the FIFO. The application layer may continue programming ancillary data into the second half of the FIFO (see block C of Figure 3-7).

If the ANC_DATA_SWITCH bit is toggled again, any new data the application layer programs will be placed into the first half of the FIFO. The device will continue to insert ancillary data from the second half of the FIFO into the video stream (see block D of Figure 3-7).

Toggling ANC_DATA_SWITCH again will clear the second half of the FIFO and restore the read and write pointers to the situation shown in block A. The switching process (shown in blocks A to D in Figure 3-7) will continue with each toggle of the ANC_DATA_SWITCH bit.

NOTE: At least 1100 PCLK cycles (41us) must pass between toggles of the ANC_DATA_SWITCH bit.

The GS9092A will insert the ancillary data programmed in the FIFO into each video frame at the designated line(s) programmed in ANC_LINE_A[10:0] and/or ANC_LINE_B[10:0].

Clearing the ANC_PKT_INS bit will not automatically disable ancillary data insertion. To disable ancillary data insertion, switch the FIFO into bypass mode by setting FIFO_MODE[1:0] = 11b. 2200 PCLK cycles after the device re-enters ancillary data insertion mode, data extraction will commence immediately if ANC_PKT_INS is HIGH.

When there are existing ancillary data packets present in the video data stream, the device will append the ancillary data to the existing data only when the ANC_SAV bit is set LOW. In this case, all existing ancillary data must be contiguous after the EAV. If data is not contiguous, the ancillary data to be inserted will be written at the first available space where the video is set to blanking levels. When ANC_SAV is set HIGH, any data present after the SAV will be overwritten.

To overwrite existing ancillary data, the ANC_DATA_REPLACE bit of the FIFO_EMPTY_OFFSET register must be set HIGH. When this bit is set HIGH, existing ancillary data will be replaced with the data to be inserted and the remainder of the line will be set to blanking levels. The device will replace ancillary data on the line of insertion only. Existing ancillary data on other lines will not be replaced with blanking levels.

NOTE: If the ANC_SAV and ANC_DATA_REPLACE bits are both set HIGH, and if ancillary data is inserted on an active picture line, the remainder of the active line will be set to blanking levels.

Ancillary Data Readback Mode

By default, when the FIFO is in ancillary data insertion mode, the application layer can only write ancillary data into the FIFO. However, if ANC_DATA_RDBACK is set HIGH (bit 13 of address 06h), the GS9092A will discontinue inserting ancillary data into the data stream and the host interface may read the ancillary data programmed into that half of the FIFO.

3.3.3.2 Clearing the ANC Data FIFO

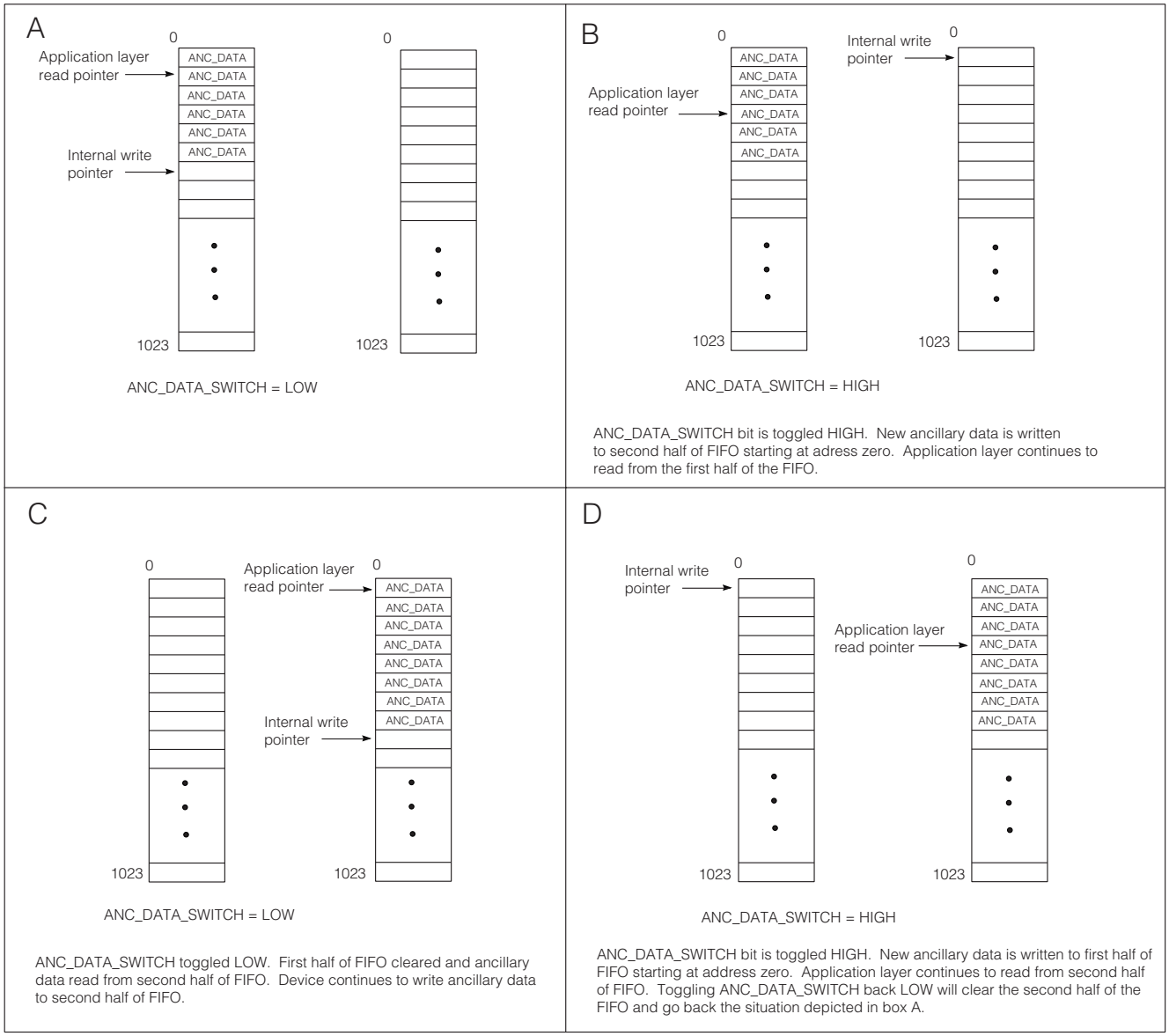
When switching to ANC FIFO mode, the user must follow one of the 2 methods below to ensure that the FIFO is fully cleared.

Clearing ANC FIFO Method 1:

1. Enable ANC FIFO mode (write 10b into the FIFO_MODE register).
2. Wait for ANC_FIFO_READY bit to be asserted.
3. Toggle (LOW-to-HIGH-to-LOW) ANC_DATA_SWITCH bit (bit 12 of IO_CONFIG register) twice.

Clearing ANC FIFO Method 2:

1. Power on device.
2. Set FIFO_EN pin HIGH.
3. Enable ANC FIFO mode (write 10b into the FIFO_MODE register).
4. Set FIFO_EN pin LOW.
5. Set FIFO_EN pin HIGH.



NOTE: At least 1100 PCLK cycles must pass between toggles of the ANC_DATA_SWITCH bit.

Figure 3-7: Ancillary Data Insertion

3.3.4 Bypass Mode

The internal FIFO is in bypass mode when the application layer sets the FIFO_EN or IOPROC_EN pin LOW, or the FIFO_MODE[1:0] bits in the IOPROC_DISABLE register are configured to 11b. By default, the FIFO_MODE[1:0] bits are set to 11b by the device whenever both the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins are LOW; however, the application layer may program the FIFO_MODE[1:0] bits as required.

In bypass mode, the FIFO is not inserted into the video path and data is presented to the input of the device synchronously with the PCLK input. The FIFO will be disabled and placed in static mode to save power.

3.4 SMPTE Mode

The GS9092A enters SMPTE mode when the $\overline{\text{SMPTE\_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW.

In this mode, the parallel data will be scrambled according to SMPTE 259M and NRZ-to-NRZI encoded prior to serialization.

3.4.1 I/O Status Signals

When DETECT_TRS is LOW, the device will be locked to the externally supplied H, V, and F signals. When DETECT_TRS is HIGH, the device will be locked to the embedded TRS signals in the parallel input data. The H, V, and F pins become output status signals, and their timing will be based on embedded TRS words.

3.4.2 HVF Timing Signal Inputs

As discussed above, the GS9092A's internal flywheel may be locked to externally provided H, V, and F signals when DETECT_TRS is set LOW by the application layer.

The H signal timing may be configured via the H_CONFIG bit of the internal IOPROC_DISABLE register as either active line-based blanking or TRS-based blanking (see Table 3-4 in Packet Generation and Insertion on page 35).

The default setting of this bit (after $\overline{\text{RESET}}$ has been asserted) is LOW.

Active line-based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing assumed by the device.

When H_CONFIG is set HIGH, TRS-based blanking is enabled. In this case, the H input should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the associated TRS words.

The timing of these signals is shown in Figure 3-8.

When the DETECT_TRS pin is set HIGH, the output timing on the H pin can be selected as either active line-based or TRS-based.

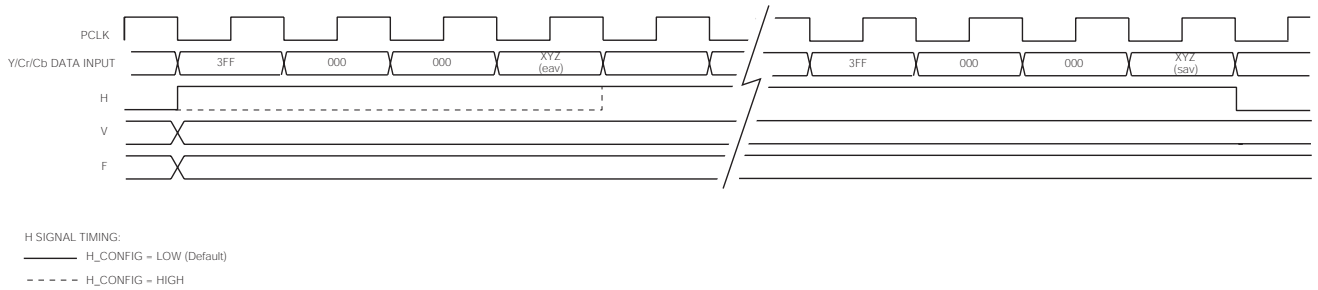


Figure 3-8: H, V, and F Input Timing

3.5 DVB-ASI Mode

The GS9092A enters DVB-ASI mode when the application layer sets the DVB_ASI pin HIGH.

In this mode, all SMPTE processing functions are disabled, and the 8-bit transport stream data will be 8b/10b encoded prior to serialization.

3.5.1 Control Signal Inputs

In DVB-ASI mode, the DIN9 and DIN8 will be configured as DVB-ASI control signals INSSYNCIN and K_IN respectively.

When INSSYNCIN is set HIGH, the device will insert K28.5 sync characters into the data stream. This function is used to assist system implementations where the GS9092A's internal FIFO is disabled (FIFO_EN = LOW), and the device is preceded by an external FIFO. Parallel data may be clocked into the external FIFO at some rate less than 27MHz. The INSSYNCIN input may then be connected to the FIFO empty signal, thus providing a means of padding up the data transmission rate to 27MHz.

NOTE 1: If the internal FIFO is enabled (FIFO_EN = HIGH), the INSSYNCIN pin should be grounded (see DVB-ASI Mode on page 24).

NOTE 2: In DVB-ASI mode, 8b/10b encoding will take place after K28.5 sync character insertion.

K_IN should be set HIGH whenever the parallel data input is to be interpreted as any special character (including the K28.5 sync character), defined by the DVB-ASI standard. This pin should be set LOW when the input is to be interpreted as data.

3.6 Data-Through Mode

The GS9092A may be configured by the application layer to operate as a simple parallel-to-serial converter. In this mode, the device presents data to the output buffer without performing any scrambling, encoding, or word-alignment.

Data-through mode is enabled only when both the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins are set low by the application layer.

3.7 Additional Processing Functions

The GS9092A contains an additional data processing block which is available in SMPTE mode only (see SMPTE Mode on page 32).

3.7.1 Input Data Blank

The GS9092A can crop the video input data, where the cropped region is set to blanking levels. All input video and ancillary data will be set to blanking levels by the device, however, the TRS will be protected at all times.

When the $\overline{\text{BLANK}}$ pin is set LOW, the input video will be set to blanking levels until the $\overline{\text{BLANK}}$ pin is re-asserted HIGH. When set HIGH, the input video will not be blanked. This allows portions of the input video to be dynamically cropped, based on the timing of the $\overline{\text{BLANK}}$ input.

The $\overline{\text{BLANK}}$ input should be synchronized to the PCLK unless the internal FIFO is enabled and configured for video mode. If the FIFO is in video mode, the $\overline{\text{BLANK}}$ input should not be used.

3.7.2 Automatic Video Standard Detection

The GS9092A can detect the input video standard by using the timing parameters extracted from the received TRS ID words or supplied H, V, and F timing signals.

Total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are calculated and presented to the host interface via the four RASTER_STRUCTURE registers (Table 3-3).

In addition to the RASTER_STRUCTURE registers, bit 4 of the VIDEO_STANDARD register contains a status bit, STD_LOCK, which will be set HIGH whenever the device has achieved full synchronization to the detected video standard.

The STD_LOCK bit, as well as the RASTER_STRUCTURE registers will default to zero under any of the following conditions:

- $\overline{\text{RESET}}$ is LOW
- $\overline{\text{SMPTE\_BYPASS}}$ is LOW

NOTE: When the video data is removed, but the PCLK remains, the VIDEO_STANDARD register will contain the last detected standard. To clear the registers, the PCLK must be removed as well or the device must be reset.

Table 3-3: Host Interface Description for Raster Structure Registers

Register Name	Bit	Name	Description	R/W	Default
RASTER_STRUCTURE1 Address: 11h	15-11	–	Not Used	–	–
	10-0	RASTER_STRUCTURE1[10:0]	Total Lines Per Frame	R	0
RASTER_STRUCTURE2 Address: 12h	15-13	–	Not Used	–	–
	12-0	RASTER_STRUCTURE2[12:0]	Total Words Per Line	R	0
RASTER_STRUCTURE3 Address: 13h	15-13	–	Not Used	–	–
	12-0	RASTER_STRUCTURE3[12:0]	Words Per Active Line	R	0
RASTER_STRUCTURE4 Address: 14h	15-11	–	Not Used	–	–
	10-0	RASTER_STRUCTURE4[10:0]	Active Lines Per Field	R	0

3.7.3 Packet Generation and Insertion

In addition to input data blanking and automatic video standards detection, the GS9092A may also calculate, assemble, and insert into the data stream various types of ancillary data packets and TRS ID words.

These features are only available when the device is set to operate in SMPTE mode and the IOPROC_EN pin is set HIGH. Individual insertion features may be enabled or disabled via the IOPROC_DISABLE register (Table 3-4).

All of the IOPROC_DISABLE register bits default to '0' after device reset, enabling all of the processing features. To disable any individual error correction feature, the host interface must set the corresponding bit HIGH in this register.

Table 3-4: Host Interface Description for Internal Processing Disable Register

Register Name	Bit	Name	Description	R/W	Default
IOPROC_DISABLE Address: 00h	15-10	–	Not Used	–	–
	9	ANC_PKT_INS	Ancillary Packet Insertion Enable. When the FIFO is configured for ancillary data insertion, set HIGH to begin inserting ancillary data. NOTE: Setting ANC_PKT_INS LOW will not automatically disable ancillary data insertion (see Ancillary Data Insertion on page 29).	R/W	0
	8-7	FIFO_MODE[1:0]	FIFO Mode: These bits control which mode the internal FIFO is operating in (see Table 3-2)	R/W	0
	6	H_CONFIG	Horizontal sync timing output configuration. Set LOW for active line blanking timing. Set HIGH for H blanking based on the H bit setting of the TRS word. See Figure 3-8 in HVF Timing Signal Inputs on page 32.	R/W	0
	5	352M_CALC	SMPTE 352M Calculation. When set LOW, the GS9092A will automatically generate packet information prior to insertion. When set HIGH, the user must program the VIDEO_FORMAT registers with the SMPTE 352M packet to be inserted.	R/W	–
	4	352M_INS	SMPTE 352M Packet Insertion. The IOPROC_EN pin and SMPTE_BYPASS pin must also be set HIGH. Set HIGH to disable. NOTE: The user should disable Packet Insertion when serializing SDTI signals.	R/W	–
	3	ILLEGAL_REMAP	Illegal code re-mapping. Detection and correction of illegal code words within the active picture area. The IOPROC_EN pin and SMPTE_BYPASS pin must also be set HIGH. Set HIGH to disable.	R/W	0
	2	EDH_CRC_INS	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error insertion. The GS9092A will generate and insert EDH packets. The IOPROC_EN pin and SMPTE_BYPASS pin must also be set HIGH. Set HIGH to disable.	R/W	0
	1	ANC_CSUM_INS	Ancillary Data Checksum insertion. The IOPROC_EN pin and SMPTE_BYPASS pin must also be set HIGH. Set HIGH to disable.	R/W	0
	0	TRS_INS	Timing Reference Signal Insertion. Occurs only when IOPROC_EN pin and SMPTE_BYPASS pin is HIGH. Set HIGH to disable.	R/W	0

3.7.3.1 SMPTE 352M Payload Identifier Generation and Insertion

If the 352M_INS bit of the IOPROC_DISABLE register is set LOW, the GS9092A can generate and insert SMPTE 352M payload identifier ancillary data packets into the data stream automatically or based on information programmed into the host interface.

When the 352M_CALC bit of the IOPROC_DISABLE register is set HIGH, the user must program the SMPTE 352M packet to be inserted into the VIDEO_FORMAT registers (Table 3-5). In addition, the line number(s) in which the packet is to be inserted must be programmed in the 352M_LINE_1 and 352M_LINE_2 registers (Table 3-6). If both line number registers are set to zero, no packets will be inserted.

NOTE: The user must program the SMPTE 352M packet into the VIDEO_FORMAT registers prior to programming the line number(s) in which the packet is to be inserted.

NOTE: It is the responsibility of the user to ensure that there is sufficient space in the horizontal blanking interval for the insertion of the SMPTE 352M packets. These packets will be inserted immediately after the EAV word on the line designated in the standard or by the user

If there are other ancillary data packets present, the SMPTE 352M packet will be inserted in the first available space in the HANC. Ancillary data must be contiguous from the EAV. When there is insufficient space available, the 352M packets will not be inserted.

When the 352M_CALC bit of the IOPROC_DISABLE register is set LOW, the GS9092A will automatically generate and insert 352M packets into the video stream. The device will also write the generated packet into the VIDEO_FORMAT registers.

NOTE: When the IOPROC_EN pin is set HIGH and all registers contain their default values, the VIDEO_FORMAT registers are set to 0h and do not contain the SMPTE 352M packet.

The SMPTE 352M packet will be inserted into the data stream according to the line number and sample position defined in the standard.

The 4:3/16:9 bit of the SMPTE 352M packet will be set LOW by default to denote 4:3. For video payloads where 16:9 images are transmitted over 270Mb/s links, the user must program the SMPTE 352M packet accordingly.

The video payload identifier packet will be version 1 and comply with the structure defined in SMPTE 352M-2002.

NOTE: The user should turn off SMPTE 352M packet insertion when serializing SDTI signals.

Table 3-5: Host Interface Description for SMPTE 352M Payload Identifier Registers

Register Name	Bit	Name	Description	R/W	Default
VIDEO_FORMAT_B Address: 10h	15-8	SMPTE 352M Byte 4	SMPTE 352M Byte 4 information must be programmed in this register when 352M_INS is LOW and 352M_CALC is HIGH.	R/W	0
	7-0	SMPTE 352M Byte 3	SMPTE 352M Byte 3 information must be programmed in this register when 352M_INS is LOW and 352M_CALC is HIGH.	R/W	0
VIDEO_FORMAT_A Address: 0Fh	15-8	SMPTE 352M Byte 2	SMPTE 352M Byte 2 information must be programmed in this register when 352M_INS is LOW and 352M_CALC is HIGH.	R/W	0
	7-0	SMPTE 352M Byte 1	SMPTE 352M Byte 1 information must be programmed in this register when 352M_INS is LOW and 352M_CALC is HIGH.	R/W	0

Table 3-6: Host Interface Description for SMPTE 352M Packet Line Number Insertion Registers

Register Name	Bit	Name	Description	R/W	Default
352M_LINE_1 Address: 26h	15-11	–	Not Used	–	–
	10-0	352M_LINE_1 [10:0]	Line number where SMPTE352M packet is inserted in field 1. If the 352M_CALC bit is HIGH, and both 352M_LINE1 and 352M_LINE2 are set to zero, then no packets will be inserted.	R/W	0
352M_LINE_2 Address: 27h	15-11	–	Not Used	–	–
	10-0	352M_LINE_2 [10:0]	Line number where SMPTE352M packet is inserted in field 2. If the 352M_CALC bit is HIGH, and both 352M_LINE1 and 352M_LINE2 are set to zero, then no packets will be inserted.	R/W	0

3.7.3.2 Illegal Code Remapping

If the ILLEGAL_REMAP bit of the IOPROC_DISABLE register is set LOW, the GS9092A will remap all codes within the active picture between the values of 3FCh and 3FFh to 3FBh. All codes within the active picture area between the values of 000h and 003h will be remapped to 004h.

In addition, 8-bit TRS and ancillary data preambles will be remapped to 10-bit values if this feature is enabled.

NOTE: The EDH block always remaps EDH packet headers regardless of the ILLEGAL_REMAP setting.

3.7.3.3 EDH Generation and Insertion

If the EDH_CRC_INS bit of the IOPROC_DISABLE register is set LOW, the GS9092A may be configured to generate and insert complete EDH packets into the data stream, or update the CRC bits of existing EDH packets.

Generation and Insertion of New EDH Packets

When EDH_CRC_UPDATE is set LOW (bit 11 of address 04h), the GS9092A will generate all of the required EDH packet data including all ancillary data preambles (DID, DBN, DC), reserved code words and checksum. Calculation of both full field (FF) and active picture (AP) CRC's will be carried out by the device.

By default, after a system reset, the GS9092A will calculate the EDH ranges based on the setting of the DETECT_TRS pin. If DETECT_TRS is LOW, the device will calculate the EDH ranges based on the received H, V, and F timing. If DETECT_TRS is HIGH, the device will calculate the ranges based on the internal TRS timing.

Alternatively, the user can program the EDH calculation ranges in the host interface. The registers available to the host interface for programming EDH calculation ranges include active picture and full field line start and end positions for both fields. Table 3-7 shows the relevant registers, which default to '0' after device reset.

If any or all of these register values are zero, then the EDH CRC calculation ranges will be determined from the flywheel generated H signal. The first AP pixel will always be the first pixel after the SAV TRS code words. The first FF pixel will always be the first pixel after the EAV TRS code words. The last AP pixel and last FF pixel will always be the last pixel before the start of the EAV code words. Figure 3-9 shows the positions of the FF and AP pixel positions relative to TRS words and H timing.

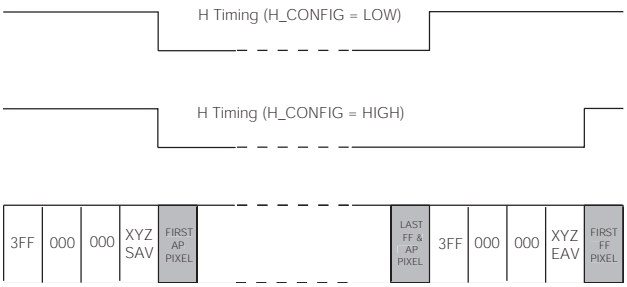


Figure 3-9: First and Last FF and AP Pixel Positions

EDH error flags (EDH, EDA, IDH, IDA, and UES) for ancillary data, full field, and active picture will also be inserted. These flags must be programmed into the EDH_FLAG registers of the device by the application layer (Table 3-8).

NOTE 1: It is the responsibility of the user to ensure that the EDH flag registers are updated once per field.

The prepared EDH packet will be inserted at the appropriate line of the video stream according to RP 165. The start pixel position of the inserted packet will be based on the SAV position of that line such that the last byte of the EDH packet (the checksum) will be placed in the sample immediately preceding the start of the SAV TRS word.

NOTE 2: It is also the responsibility of the user to ensure that there is sufficient space in the horizontal blanking interval for the EDH packet to be inserted.

CRC Update of Existing Packets

When the EDH_CRC_UPDATE bit is set HIGH, the GS9092A will not generate any new EDH packets, but will instead update the CRC bytes of the existing EDH packets within the input video data stream. Incoming EDH flags are preserved and can be read from the EDH_FLAG register, which becomes read-only (Table 3-8).

When EDH packets are detected, the EDH_FLAG register is updated on each field. These registers will be cleared LOW if no EDH packet is detected during blanking at the end of the vertical blanking period (falling edge of V).

The validity or ‘V’ bits of the incoming EDH packet will also be set to ‘1’ to denote that the CRC calculations are valid. The EDH packet checksum word is also re-calculated and re-inserted.

When incoming EDH packets are updated, the location of the packets within the video stream remains unchanged. EDH packets that are to be updated can be present anywhere within the horizontal blanking region of the vertical blanking period.

Table 3-7: Host Interface Description for EDH Calculation Range Registers

Register Name	Bit	Name	Description	R/W	Default
AP_LINE_START_F0 Address: 15h	15-11	–	Not Used	–	–
	10-0	AP_LINE_START_F0[10:0]	Field 0 Active Picture start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_END_F0 Address: 16h	15-11	–	Not Used	–	–
	10-0	AP_LINE_END_F0[10:0]	Field 0 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_START_F1 Address: 17h	15-11	–	Not Used	–	–
	10-0	AP_LINE_START_F1[10:0]	Field 1 Active Picture start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_END_F1 Address: 18h	15-11	–	Not Used	–	–
	10-0	AP_LINE_END_F1[10:0]	Field 1 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_START_F0 Address: 19h	15-11	–	Not Used	–	–
	10-0	FF_LINE_START_F0[10:0]	Field 0 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_END_F0 Address: 1Ah	15-11	–	Not Used	–	–
	10-0	FF_LINE_END_F0[10:0]	Field 0 Full Field end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_START_F1 Address: 1Bh	15-11	–	Not Used	–	–
	10-0	FF_LINE_START_F1[10:0]	Field 1 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_END_F1 Address: 1Ch	15-11	–	Not Used	–	–
	10-0	FF_LINE_END_F1[10:0]	Field 1 Full Field end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_START_F0 Address: 1Dh	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_START_F0[12:0]	Field 0 Active Picture start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_END_F0 Address: 1Eh	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_END_F0[12:0]	Field 0 Active Picture end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0

Table 3-7: Host Interface Description for EDH Calculation Range Registers (Continued)

Register Name	Bit	Name	Description	R/W	Default
AP_PIXEL_START_F1 Address: 1Fh	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_START_F1[12:0]	Field 1 Active Picture start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_PIXEL_END_F1 Address: 20h	15-13	–	Not Used	–	–
	12-0	AP_PIXEL_END_F1[12:0]	Field 1 Active Picture end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_START_F0 Address: 21h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_START_F0[12:0]	Field 0 Full Field start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_END_F0 Address: 22h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_END_F0[12:0]	Field 0 Full Field end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_START_F1 Address: 23h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_START_F1[12:0]	Field 1 Full Field start pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_PIXEL_END_F1 Address: 24h	15-13	–	Not Used	–	–
	12-0	FF_PIXEL_END_F1[12:0]	Field 1 Full Field end pixel data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0

Table 3-8: Host Interface Description for EDH Flag Register

Register Name	Bit	Name	Description	R/W	Default
EDH_FLAG Address: 02h	15	–	Not Used	–	–
	14	ANC-UES	Ancillary Unknown Error Status flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	13	ANC-IDA	Ancillary Internal device error Detected Already flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	12	ANC-IDH	Ancillary Internal device error Detected Here flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	11	ANC-EDA	Ancillary Error Detected Already flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	10	ANC-EDH	Ancillary Error Detected Here flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	9	FF-UES	Full Field Unknown Error Status flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	8	FF-IDA	Full Field Internal device error Detected Already flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	7	FF-IDH	Full Field Internal device error Detected Here flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0

Table 3-8: Host Interface Description for EDH Flag Register (Continued)

Register Name	Bit	Name	Description	R/W	Default
	6	FF-EDA	Full Field Error Detected Already flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	5	FF-EDH	Full Field Error Detected Here flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	4	AP-UES	Active Picture Unknown Error Status flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	3	AP-IDA	Active Picture Internal device error Detected Already flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	2	AP-IDH	Active Picture Internal device error Detected Here flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	1	AP-EDA	Active Picture Error Detected Already flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0
	0	AP-EDH	Active Picture Error Detected Here flag will be generated and inserted when IOPROC_EN and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. NOTE: When EDH_CRC_UPDATE is set HIGH, this bit is read-only, and will be updated by the device.	R/W	0

3.7.3.4 Ancillary Data Checksum Generation and Insertion

The GS9092A will calculate checksums for all detected ancillary data packets presented to the device. These calculated checksum values are inserted into the data stream prior to serialization.

Ancillary data checksum generation and insertion will only take place if the ANC_CSUM_INS bit of the IOPROC_DISABLE register is set LOW.

3.7.3.5 TRS Generation and Insertion

The GS9092A can generate and insert 10-bit TRS code words into the data stream as required. This feature is enabled by setting the TRS_INS bit of the IOPROC_DISABLE register LOW.

TRS word generation will be performed in accordance with the timing parameters, which will be locked either to the received TRS ID words or the supplied H, V, and F timing signals.

3.8 Parallel-to-Serial Conversion

The parallel data output of the internal data processing blocks is fed to the parallel-to-serial converter. The function of this block is to generate a serial data stream from the 10-bit parallel data words.

3.9 Serial Digital Data PLL

The input PCLK pin is internally connected to an integrated phase-locked loop. This PLL is also responsible for generating all internal clock signals required by the device. An internal VCO provides the transmission clock rate for the GS9092A.

The PLL and VCO each require a +1.8V DC power supply, which is supplied via the VCO_VDD / VCO_GND and PLL_VDD / PLL_GND pins. A loop filter capacitor should also be connected between the LF+ and LF- pins. See Typical Application Circuit on page 56.

NOTE: For a SMPTE compliant serial output, the jitter on the input PCLK across the frequency spectrum should not exceed 350ps.

3.10 Serial Digital Output

The GS9092A contains an integrated current mode differential serial digital output buffer/cable driver, capable of driving 800mV into two single ended 75Ω loads. Output pins SDO and $\overline{SDO}$ provide a single differential serial digital output. Alternatively, two 75Ω connections can be driven using single ended drive.

To enable the output, SDO_EN must be set HIGH by the application layer. Setting the SDO_EN signal LOW will cause the SDO and $\overline{SDO}$ output pins to become high impedance, resulting in reduced device power consumption.

With suitable external return loss matching circuitry, the GS9092A's serial digital outputs will provide a minimum output return loss of 15dB.

The output buffer / cable driver uses a separate power supply of +1.8V DC supplied via the CD_VDD and CD_GND pins.

3.10.1 Output Swing

Nominally, the voltage swing of the serial digital output is 800mV$_{p-p}$ single-ended into a 75Ω load. This is set externally by connecting the RSET pin to CD_VDD through a resistor. The output swing may be adjusted by altering the value of the RSET resistor.

SMPTE-compliant cable driver operation can be achieved at +1.8V operation by connecting external pull-up resistors from the differential output to the +1.8V source.

3.10.2 Serial Digital Output Mute Control

The GS9092A will automatically mute the serial digital output when $\overline{RESET}$ is LOW. In this case, the SDO and $\overline{SDO}$ signals are set to the last logic state.

3.10.3 Output Return Loss Measurement

Under normal operating conditions the cable connected to the BNC connector will provide a 75Ω load. Under this loaded condition, the outputs of the device swing between V_{CC}-0.4V and V_{CC}-1.2V. When a 75Ω load is not connected to the BNC connector, the outputs of the device will swing between V_{CC} and V_{CC} - 1.6V. The difference in output swing is shown in Figure 3-10.

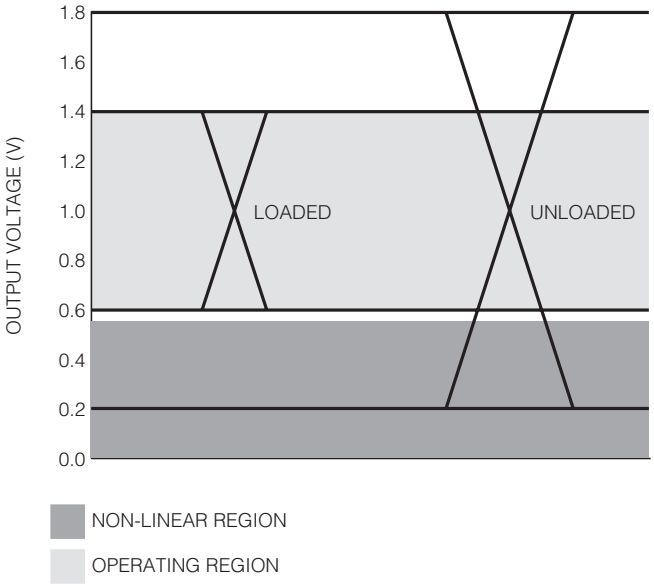


Figure 3-10: Output Swing in the non-linear region of the GS9092A's output

When performing a return loss measurement the output is in a static and unloaded condition. The typical cable driver power supply is 1.8V, which places the unloaded swing very close to the power rails of the GS9092A's cable driver. As the output voltage approaches the GND rail, the output driver enters a non-linear region. In this region, the GS9092A's output transistor's characteristics are not optimal (see Figure 3-10).

Figure 3-11 shows the return loss performance of the cable driver as a function of the output voltage level. When the output driver is latched low, the observed ORL in the non-linear region will appear degraded. When the output driver is latched high, the observed ORL will be representative of the operating return loss.

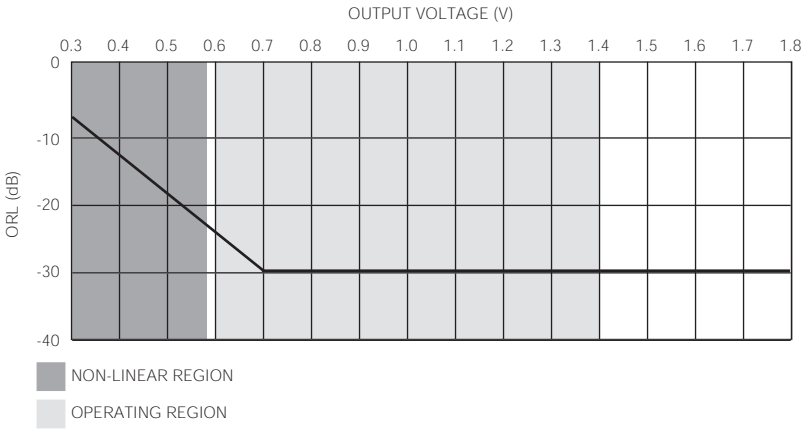


Figure 3-11: ORL vs. Output Voltage

3.11 Programmable Multi-function I/O

The GS9092A has a multi-function I/O port that uses 3 pins, STAT0 through STAT2. Each pin can be programmed via the host interface to output one of the following signals: H, V, F, FIFO_FULL, and FIFO_EMPTY (see Table 3-9). The pins may also act as inputs for external H, V and F signals if DETECT_TRS is set LOW. Alternatively, STAT[2:0] may be set to a high-impedance state.

Table 3-9: I/O Signals Available on Multi-function I/O Ports

I/O Status Signal	Reference
H	Section 3.4.1
V	Section 3.4.1
F	Section 3.4.1
FIFO_FULL	Section 3.3.2.1
FIFO_EMPTY	Section 3.3.2.1

The registers that determine the signals present on the STAT [2:0] pins are labelled STAT0_CONFIG[2:0], STAT1_CONFIG[2:0], and STAT2_CONFIG[2:0] respectively. Table 3-10 shows the setting of the IO_CONFIG registers for each of the available output signals.

Table 3-10: IO_CONFIG Settings

Function	I/O	DETECT_TRS Setting	IO_CONFIG Setting
H	Input	LOW	000b
	Output	HIGH	000b
V	Input	LOW	001b
	Output	HIGH	001b
F	Input	LOW	010b
	Output	HIGH	010b
High Z	Output	X	011b
High Z	Output	X	100b
High Z	Output	X	101b
FIFO_FULL	Output	X	110b
FIFO_EMPTY	Output	X	111b

The default setting for each IO_CONFIG register depends on the configuration of the device and the internal FIFO mode selected. This is shown in Table 3-11.

NOTE: The FIFO_FULL and FIFO_EMPTY flags can only be displayed on the STAT[2:0] pins when the device is in DVB-ASI mode. If the FIFO_FULL or FIFO_EMPTY value (100b and 101b respectively) is programmed into the IO_CONFIG registers when the device is in SMPTE mode, the value will be ignored and the I/O pin will be set to a high impedance state.

Table 3-11: STAT [2:0] Output Default Configuration

Device Configuration	IO_CONFIG Register	I/O	Function	Default IO_CONFIG Setting
SMPTE Functionality $\overline{\text{SMPTE\_BYPASS}}$ = HIGH DVB_ASI = LOW FIFO: Video Mode or Ancillary Data Insertion Mode	STAT0_CONFIG	I/O	H	000b
	STAT1_CONFIG	I/O	V	001b
	STAT2_CONFIG	I/O	F	010b
DVB-ASI DVB_ASI = HIGH FIFO: DVB-ASI Mode	STAT0_CONFIG	Output	FIFO_FULL	110b
	STAT1_CONFIG	Output	FIFO_EMPTY	111b
	STAT2_CONFIG	Output	High Z	000b
Data-Through $\overline{\text{SMPTE\_BYPASS}}$ = LOW DVB_ASI = LOW	STAT0_CONFIG	Output	High Z	000b
	STAT1_CONFIG	Output	High Z	000b
	STAT2_CONFIG	Output	High Z	000b

3.12 Low Latency Mode

When the IOPROC_EN pin is set LOW, the GS9092A will enter a low-latency mode such that the serial digital data will be output with the minimum PCLK latency possible. The FIFO and all processing blocks except the SMPTE scrambling block will be bypassed when $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

Low-latency mode will also be selected when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW, regardless of the setting of the IOPROC_EN signal (see Table 3-12).

In DVB-ASI mode (DVB-ASI Mode on page 33), the device will have a higher latency then low-latency mode, although this latency will be less than SMPTE mode (SMPTE Mode on page 32).

Table 3-12: Pin Settings in Low-latency Mode

IOPROC_EN Setting	$\overline{\text{SMPTE\_BYPASS}}$ Setting	Latency (PCLK Cycles)
LOW	LOW	9
HIGH	LOW	10
LOW	HIGH	8
HIGH	HIGH	21

3.13 GSPI Host Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features of the GS9092A and/or to provide additional status information through configuration registers in the device.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 3-12.

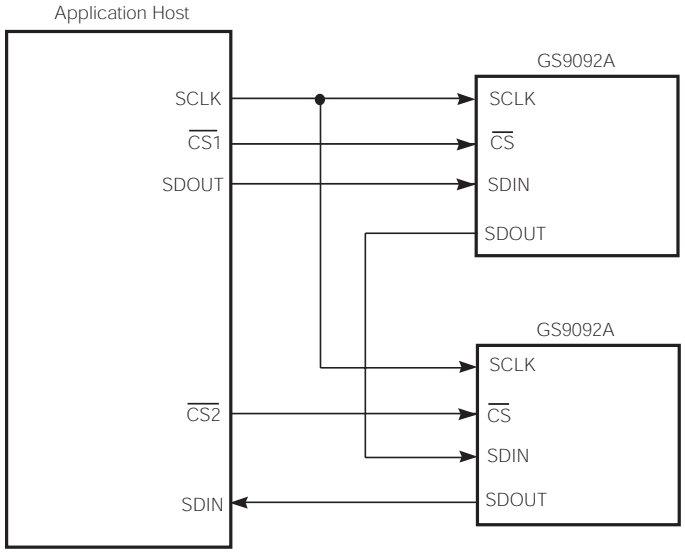


Figure 3-12: GSPI Application Interface Connection

All read or write access to the GS9092A is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

NOTE: All unused GSPI input pins ($\overline{CS}$, SDIN, SCLK) should be pulled up to VCC_IO.

3.13.1 Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 3-13 shows the command word format and bit configurations.

Command words are clocked into the GS9092A on the rising edge of the serial clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each command word must be followed by only one data word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following data word will be written into the address specified in the command word, and subsequent data words will be written into incremental addresses from the previous data word. This facilitates multiple address writes without sending a command word for each data word.

Auto-Increment may be used for both read and write access.

3.13.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 3-15 and Figure 3-16 respectively. The timing parameters are defined in Table 3-13.

When several devices are connected to the GSPI chain, only one $\overline{CS}$ must be asserted during a read sequence.

During the write sequence, all command and following data words input at the SDIN pin are output at the SDOUT pin as is. Where several devices are connected to the GSPI chain, data can be written simultaneously to all the devices that have $\overline{CS}$ set LOW.

Table 3-13: GSPI Timing Parameters

Parameter	Definition	Specification
t_0	The minimum duration of time chip select, $\overline{CS}$, must be LOW before the first SCLK rising edge.	1.5 ns
t_1	The minimum SCLK period.	18.5 ns
t_2	Duty cycle tolerated by SCLK.	40% to 60%
t_3	Minimum input setup time.	1.5 ns
t_4	Write Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	37.1 ns
t_5	Read Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	148.4 ns
t_5	Read Cycle - ANC_DATA_RDBACK bit HIGH when FIFO is in ancillary insertion mode (see Ancillary Data Insertion on page 29): the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	222.6 ns

Table 3-13: GSPI Timing Parameters (Continued)

Parameter	Definition	Specification
t_6	Minimum output hold time.	1.5 ns
t_7	The minimum duration of time between the last SCLK of the GSPI transaction and when $\overline{CS}$ can be set HIGH.	37.1 ns
t_8	Minimum input hold time.	1.5 ns

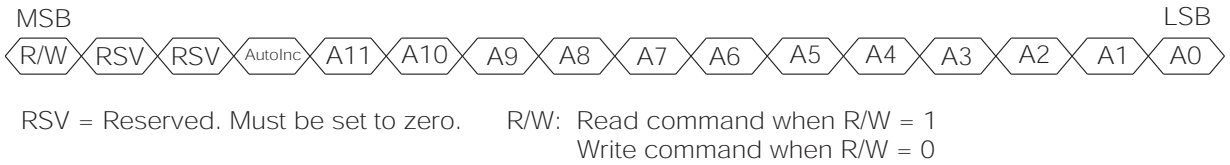


Figure 3-13: Command Word Format

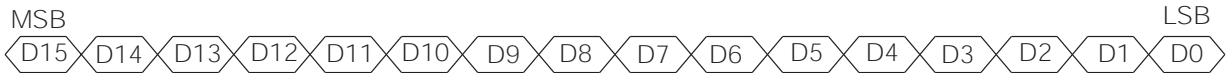


Figure 3-14: Data Word Format

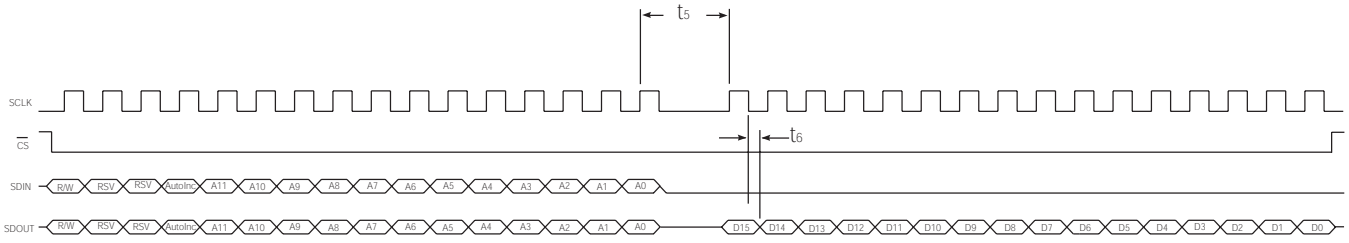


Figure 3-15: GSPI Read Mode Timing

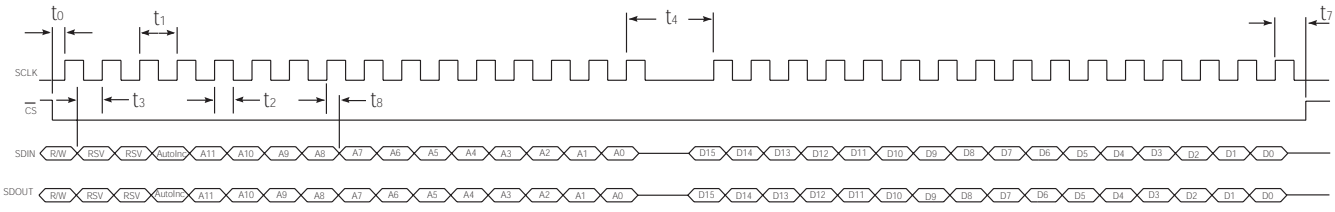


Figure 3-16: GSPI Write Mode Timing

3.13.3 Configuration and Status Registers

Table 3-14 summarizes the GS9092A's internal status and configuration registers.

All of these registers are available to the host via the GSPI and are all individually addressable.

Where status registers contain less than the full 16 bits of information, two or more registers may be combined at a single logical address.

Table 3-14: GS9092A Internal Registers

Address	Register Name	Reference
00h	IOPROC_DISABLE	Section 3.7.3
02h	EDH_FLAG	Section 3.7.3.3
04h	VIDEO_STANDARD	Section 3.7.2
05h	IO_CONFIG	Section 3.11
06h	FIFO_EMPTY_OFFSET	Section 3.3.2.1
07h	FIFO_FULL_OFFSET	Section 3.3.2.1
08h - 09h	ANC_LINE	Section 3.3.3
0Fh - 10h	VIDEO_FORMAT	Section 3.7.3.1
11h - 14h	RASTER_STRUCTURE	Section 3.7.2
15h - 24h	EDH_CALC_RANGES	Section 3.7.3.3
26h - 27h	352M_LINE	Section 3.7.3.1
28h	ANC_WORDS	Section 3.3.3
02Ch - 42Bh	INTERNAL FIFO	Section 3.3.3

3.14 JTAG Operation

When the JTAG/$\overline{\text{HOST}}$ pin is set HIGH by the application layer, the host interface port (as described in GSPI Host Interface on page 50) will be configured for JTAG test operation. In this mode, pins 16, 17, 19, and 20 become TMS, TCK, TDO, and TDI respectively. In addition, the $\overline{\text{RESET}}$ pin will operate as the test reset pin, as well as resetting the internal registers.

Boundary scan testing using the JTAG interface will be possible in this mode.

There are two methods in which JTAG can be used on the GS9092A:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; or
2. Under control of the host for applications such as system power self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 3-17.

Alternatively, if the test capabilities are to be used in the system, the host may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 3-18.

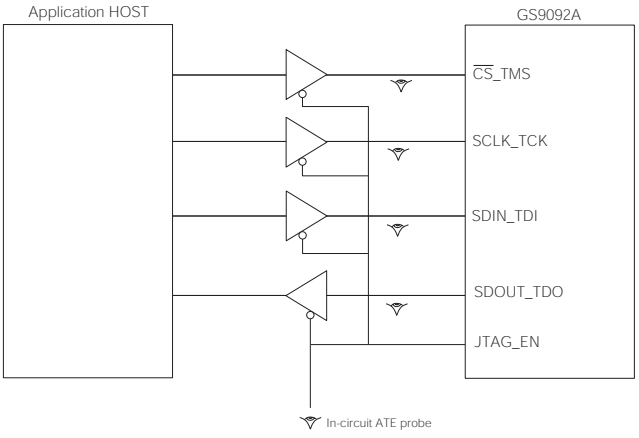


Figure 3-17: In-Circuit JTAG

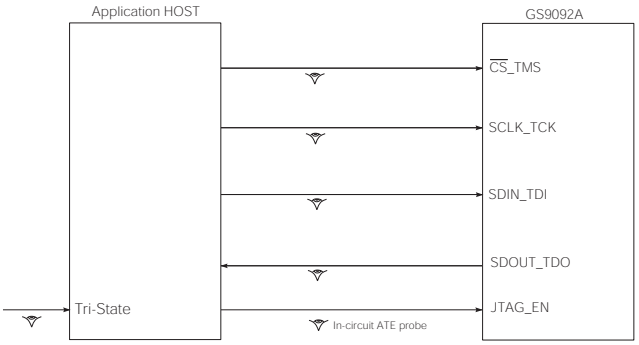


Figure 3-18: System JTAG

3.15 Device Power Up

The GS9092A has a recommended power supply sequence. To ensure correct power up, power the CORE_VDD pins before the IO_VDD pins. In order to initialize all internal operating conditions to their default state the application layer must hold the RESET pin LOW for a minimum of t_{reset} = 1ms.

Device pins can be driven prior to power up without causing damage.

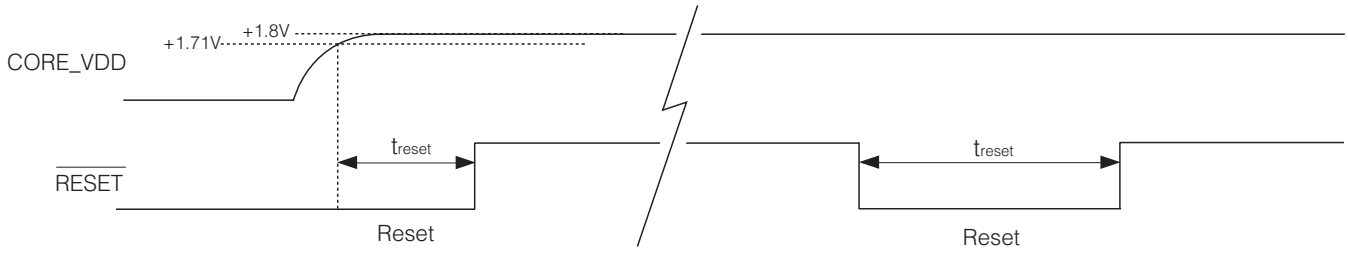


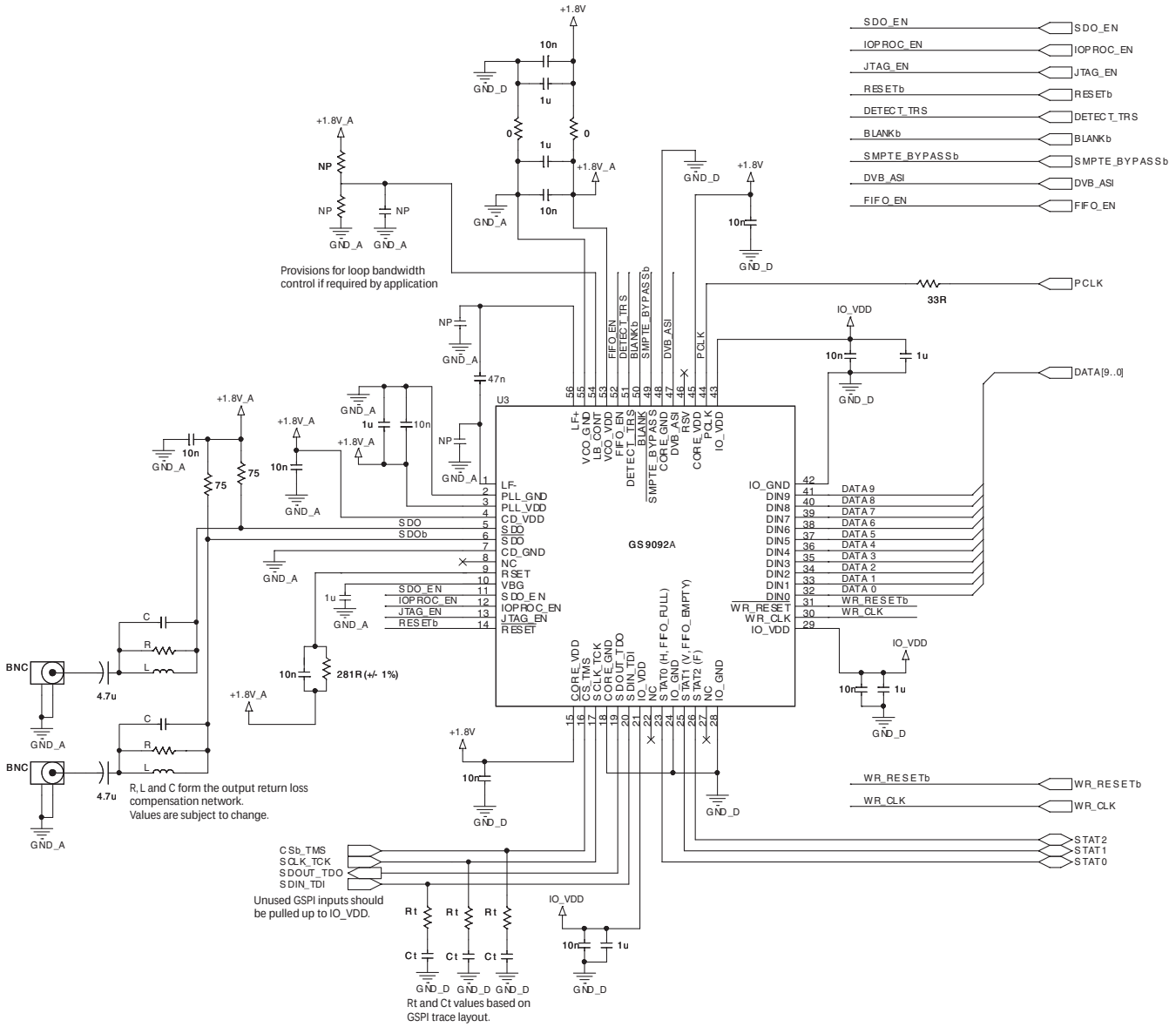
Figure 3-19: Reset pulse

4. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 267M	Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching

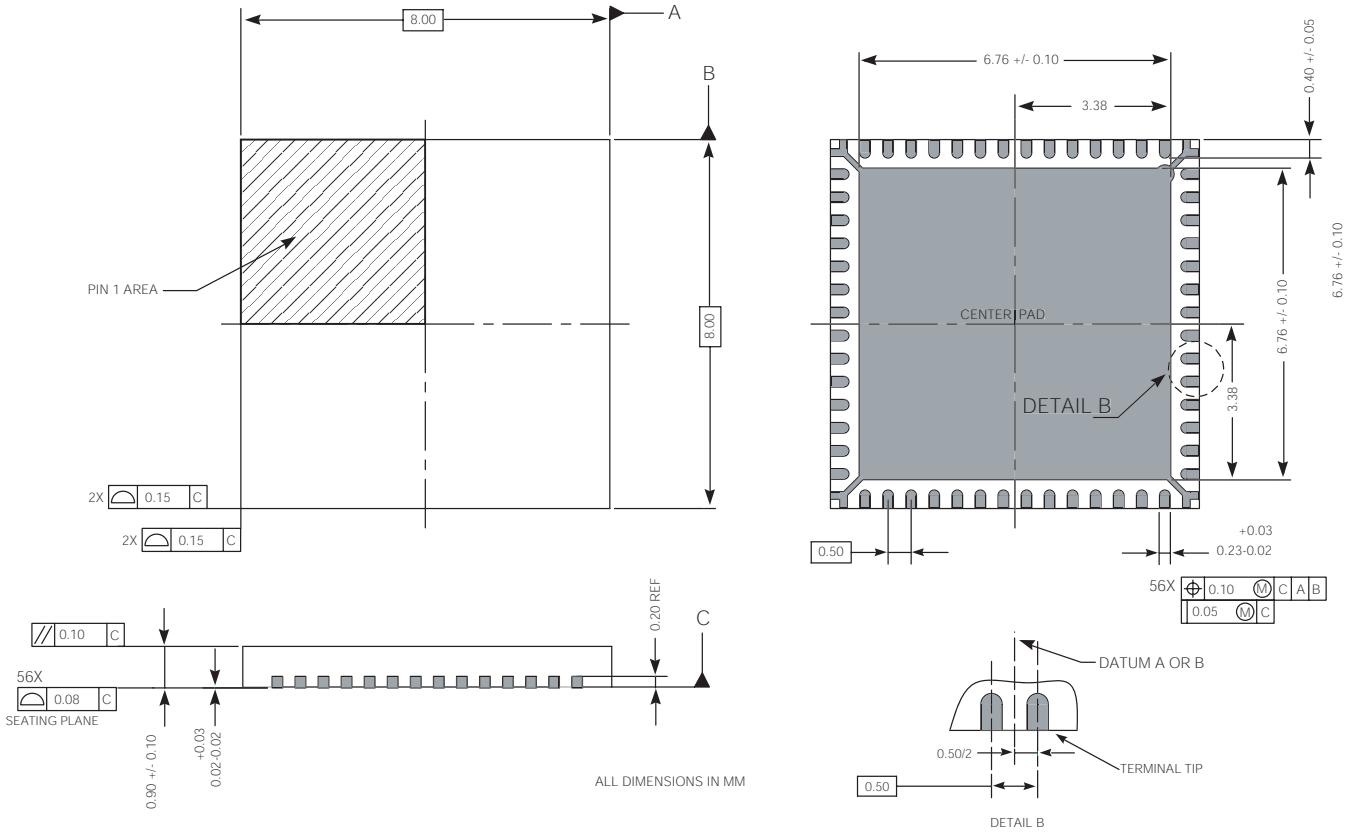
5. Application Information

5.1 Typical Application Circuit

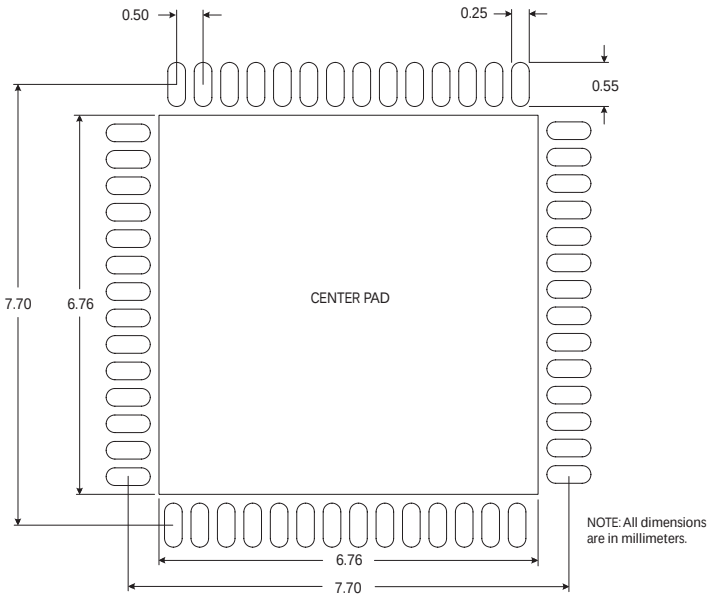


6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad of the PCB footprint should be connected to the CORE_GND plane by a minimum of 25 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	8mm x 8mm 56-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	12.2°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	25.8°C/W
Psi	9.1°C/W
Pb-free and RoHS compliant	Yes

6.4 Ordering Information

Part Number	Package	Temperature Range
GS9092ACNE3	56-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and / or Modifications
0	138237	–	February 2006	New Document

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

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