

TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

# GT8G133

## Strobe Flash Applications

- Compact and Thin (TSSOP-8) package
- Enhancement-mode
- 4-V gate drive voltage:  $V_{\rm GE}$  = 4.0 V (min) (@IC = 150 A)
- Peak collector current:  $I_C = 150 \text{ A (max)}$

## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Collector-emitter voltage		V <sub>CES</sub>	400	V	
Gate-emitter voltage	DC	V <sub>GES</sub>	± 6	٧	
	Pulse	V <sub>GES</sub>	± 8		
Collector current	Pulse (Note 1)	I <sub>CP</sub>	150	A	
Collector power	(Note 2a)	P <sub>C</sub> (1)	1.1	W	
dissipation (t=10 s)	(Note 2b)	P <sub>C</sub> (2)	0.6	W	
Junction temperature		Tj I	150	°C	
Storage temperature range		T <sub>stg</sub>	-55~150	°C	

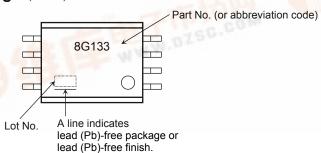
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

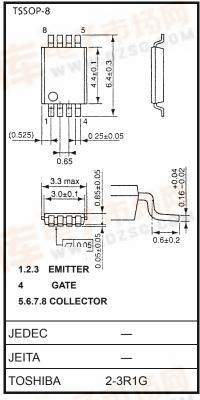
## Thermal Characteristics

Characteristics	Symbol	Rating	Unit	
Thermal resistance, junction to ambient (t = 10 s) (Note2a)	R <sub>th (j-a)</sub> (1)	114	°C/W	
Thermal resistance , junction to ambient (t = 10 s) (Note2b)	R <sub>th (j-a)</sub> (2)	208	°C/W	

## Marking (Note 3)

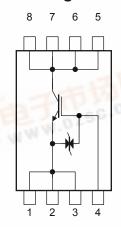


Unit: mm



Weight: 0.035 g (typ.)

## **Circuit Configuration**



For (Note 1), (Note 2a), (Note 2b) and (Note 3), Please refer to the next page.

# **Electrical Characteristics (Ta = 25°C)**

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GES</sub>	$V_{GE} = \pm 6 \text{ V}, V_{CE} = 0$	_	_	± 10	μΑ
Collector cut-off current		I <sub>CES</sub>	V <sub>CE</sub> = 400 V, V <sub>GE</sub> = 0	_	_	10	μА
Gate-emitter cut-off voltage		V <sub>GE</sub> (OFF)	$I_C = 1 \text{ mA}, V_{CE} = 5 \text{ V}$	0.7	1.05	1.4	V
Collector-emitter saturation voltage		V <sub>CE</sub> (sat)	I <sub>C</sub> = 150 A, V <sub>GE</sub> = 4 V	_	2.9	_	V
Input capacitance		C <sub>ies</sub>	$V_{CE} = 10 \text{ V}, V_{GE} = 0, f = 1 \text{ MHz}$	_	2500	_	pF
Switching time	Rise time	t <sub>r</sub>	$\begin{array}{c} 4 \text{ V} \\ 0 \\ \hline \\ V_{\text{IN}}: \ t_r \leq 100 \text{ ns} \\ t_f \leq 100 \text{ ns} \\ \hline \\ \text{Duty cycle} \leq 1\% \\ \end{array} \Rightarrow 300 \text{ V}$		1.6	_	μ <b>s</b>
	Turn-on time	t <sub>on</sub>		_	1.7	_	
	Fall time	t <sub>f</sub>			1.7	_	
	Turn-off time	t <sub>off</sub>		_	2.0	_	

#### **Note**

Note 1: Please use devices on condition that the junction temperature is below 150°C. Repetitive rating: pulse width limited by maximum junction temperature.

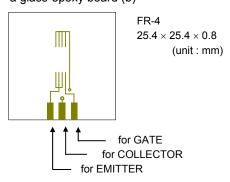
Note 2a : Device mounted on a glass-epoxy board (a)

FR-4
25.4 × 25.4 × 0.8

(unit : mm)

for COLLECTOR
for EMITTER
for GATE

Note 2b : Device mounted on a glass-epoxy board (b)



Note 3: O on lower right of the marking indicates Pin 1.

Weekly code: (Three digits)
 Week of manufacture
 (01 for first week of year, continues up to 52 or 53)
 Year of manufacture
 (One low-order digits of calendar year)

Pb-Free Finish (Only a coating lead terminal) :

It is marking about an underline to a week of manufacture mark.

## **Caution on handling**

This device is MOS gate type. Therefore , please care of a protection from ESD in your handling .

# Caution in design

You should be design dV/dt value is below 400 V/ $\mu s$  when IGBT turn off.

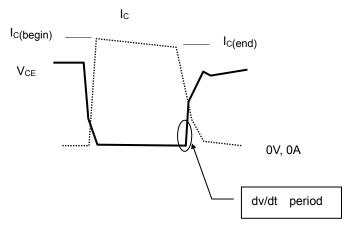
definition of dv/dt

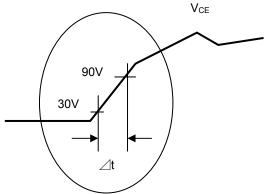
The slope of vce from 30v to 90v (attached figure.1)

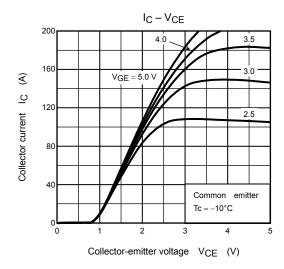
$$dv/dt = (90V-30V) / (\triangle t)$$
$$= 60V / \triangle t$$

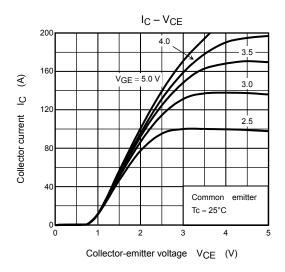
waveform

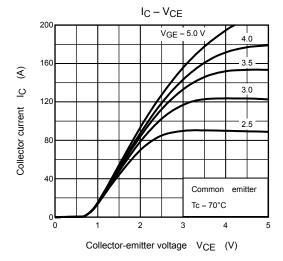
•waveform (expansion)

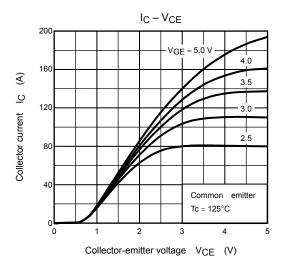


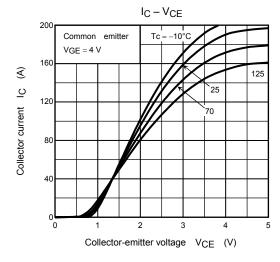


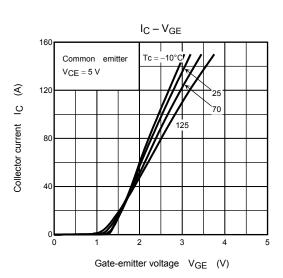


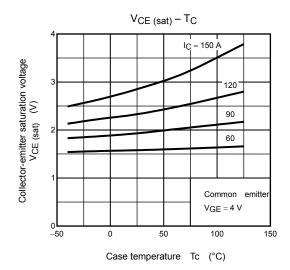


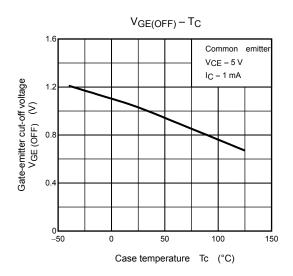


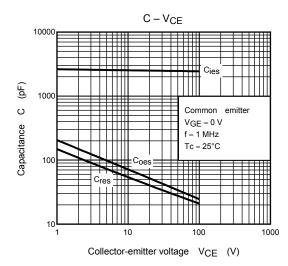


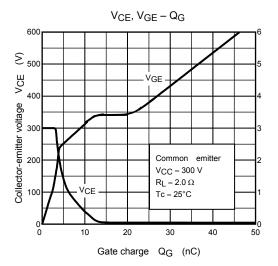




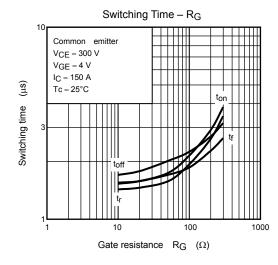


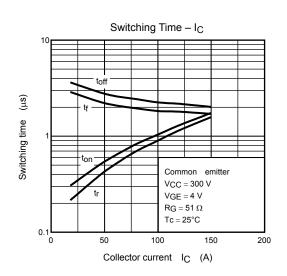


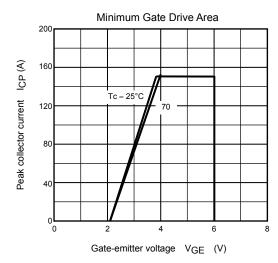


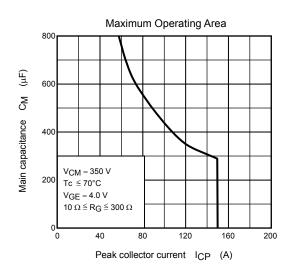












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