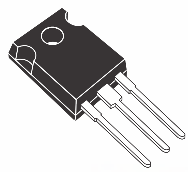
STGW30NC60VD

N-channel 40A - 600V - TO-247
Very fast switching PowerMESH™ IGBT

General features

Type	V_{CES}	$V_{CE(sat)}$ (Max)@ 25°C	I_C @100°C
STGW30NC60VD	600V	<2.5V	40A

- High current capability
- High frequency operation up to 50KHz
- Very soft ultra fast recovery antiparallel diode
- New generation products with tighter parameter distribution

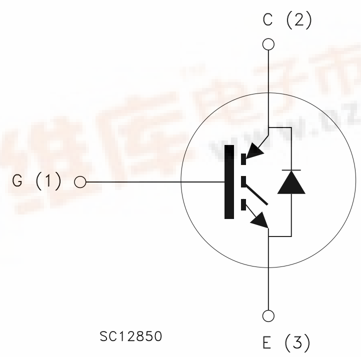


TO-247

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “V” identifies a family optimized for high frequency.

Internal schematic diagram



Applications

- High frequency inverters, UPS
- Motor drivers
- SMPS and PFC in both hard switch and resonant topologies

Order code

Part number	Marking	Package	Packaging
STGW30NC60VD	GW30NC60VD	TO-247	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C (1)	Collector current (continuous) at 25°C	80	A
I_C (1)	Collector current (continuous) at 100°C	40	A
I_{CM} (2)	Collector current (pulsed)	100	A
I_{CL}	Turn-off soa minimum current	100	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Diode RMS forward current at Tc=25°C	30	A
P_{TOT}	Total dissipation at T_C = 25°C	250	W
T_j	Operating junction temperature	– 55 to 150	°C
T_{stg}	Storage temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 2. Thermal resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
Rthj-case	Thermal resistance junction-case IGBT			0.48	°C/W
	Thermal resistance junction-case diode			1.5	°C/W
Rthj-amb	Thermal resistance junction-ambient			62.5	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 1mA, V_{GE} = 0	600			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	V_{GE}=15V, I_C=20A,Tj=25°C V_{GE}=15V, I_C=20A,Tj=125°C		1.8 1.7	2.5	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250µA	3.75		5.75	V
I_{CES}	Collector-emitter leakage current (V_{GE} = 0)	V_{CE} = Max rating,Tc=25°C V_{CE}= Max rating, Tc=125°C			250 1	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} = ± 20V, V_{CE} = 0			±100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C= 20A		15		S

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1 MHz, V_{GE}= 0		2200 225 50		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 20A, V_{GE} = 15V, *(see Figure 17)*		100 16 45	140	nC nC nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{onf}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC}=390 V, I_C= 20A, R_G=3.3Ω, V_{GE}=15V Tj=25°C *(see Figure 16)*		31 11 1600		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC}=390 V, I_C= 20A, R_G=3.3Ω, V_{GE}=15V Tj=125°C *(see Figure 16)*		31 11.5 1500		ns ns A/µs
$t_{r(Voff)}$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC}=390 V, I_C= 20A, R_G=3.3Ω, V_{GE}=15V Tj=25°C *(see Figure 16)*		28 100 75		ns ns ns
$t_{r(Voff)}$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC}=390 V, I_C= 20A, R_G=3.3Ω, V_{GE}=15V Tj=125°C *(see Figure 16)*		66 150 130		ns ns ns

Table 6. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
E_{on} (1) E_{off} E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC}=390 V, I_C= 20A, R_G=3.3Ω, V_{GE}=15V, Tj= 25°C *(see Figure 18)*		220 330 550	300 450 750	µJ µJ µJ
E_{on} (1) E_{off} E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC}=390 V, I_C= 20A, R_G=3.3Ω, V_{GE}=15V, Tj= 125°C *(see Figure 18)*		450 770 1220		µJ µJ µJ

1. Eon is the turn-on losses when a typical diode is used in the test circuit in *Figure 18*. Eon include diode recovery energy. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)

Table 7. Collector-emitter diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
V_f	Forward on-voltage	If = 10A If = 10A, Tj = 125°C		1.3 1	2.0	V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	If = 20A, V_R = 40V, T_j = 25°C, di/dt =100A/µs *(see Figure 19)*		44 66 3		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	If = 20A, V_R = 40V, T_j = 125°C, di/dt =100A/µs *(see Figure 19)*		88 237 5.4		ns nC A

2.1 Electrical characteristics (curves)

Figure 1. Output characteristics

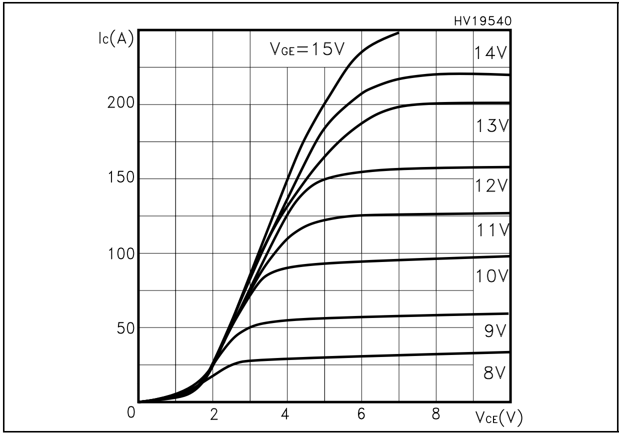


Figure 2. Transfer characteristics

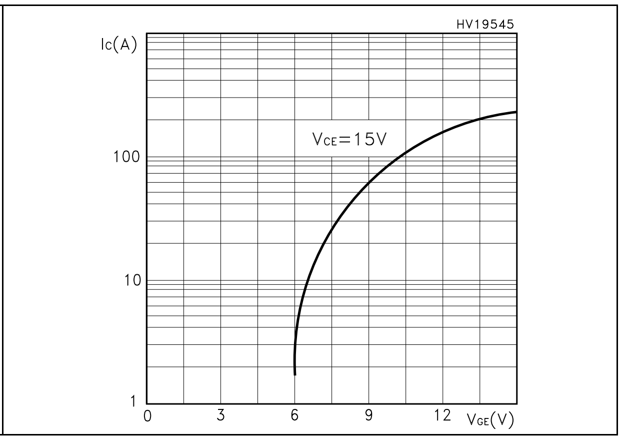


Figure 3. Transconductance

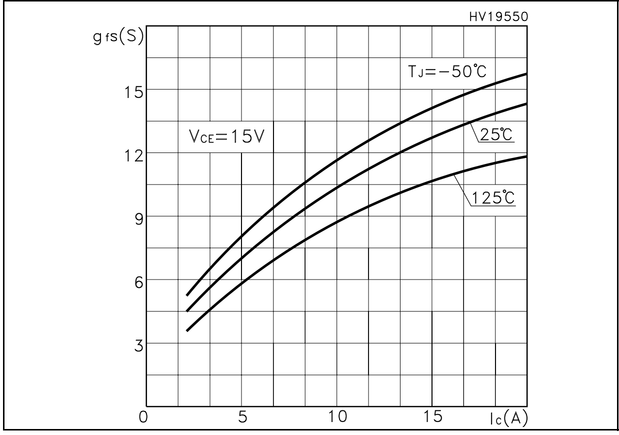


Figure 4. Collector-emitter on voltage vs temperature

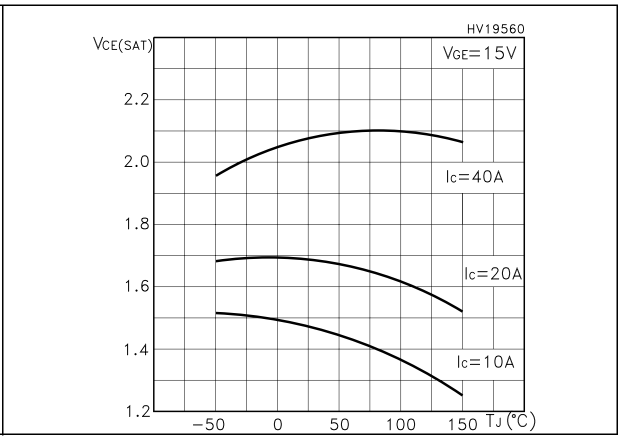


Figure 5. Collector-emitter on voltage vs collector current

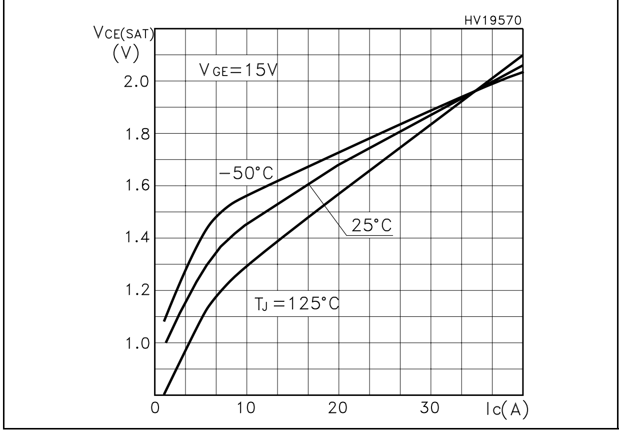


Figure 6. Normalized gate threshold vs temperature

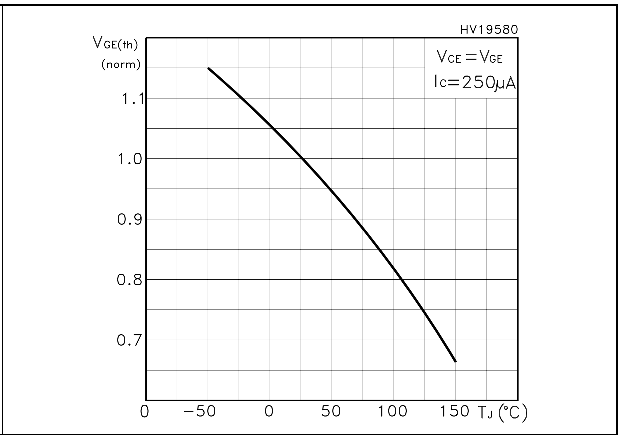


Figure 7. Normalized breakdown voltage vs temperature

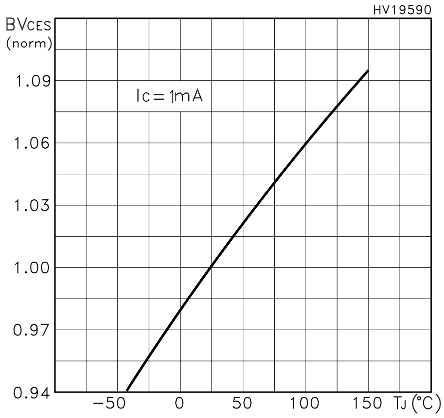


Figure 8. Gate charge vs gate-emitter voltage

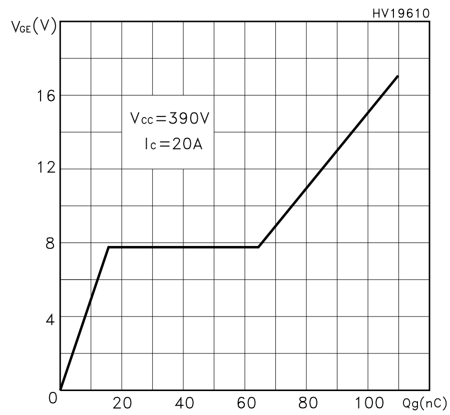


Figure 9. Capacitance variations

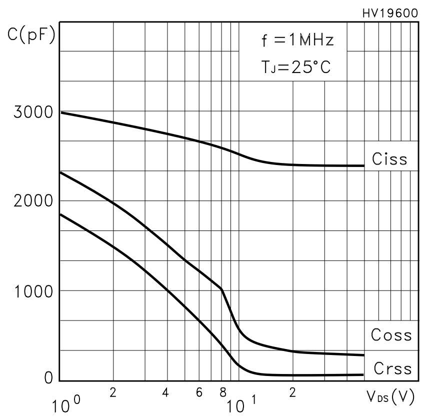


Figure 10. Switching losses vs temperature

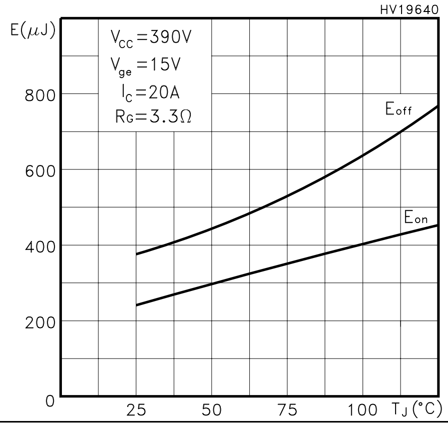


Figure 11. Switching losses vs gate resistance

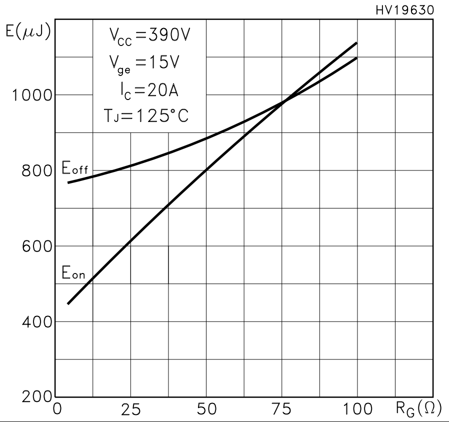


Figure 12. Switching losses vs collector current

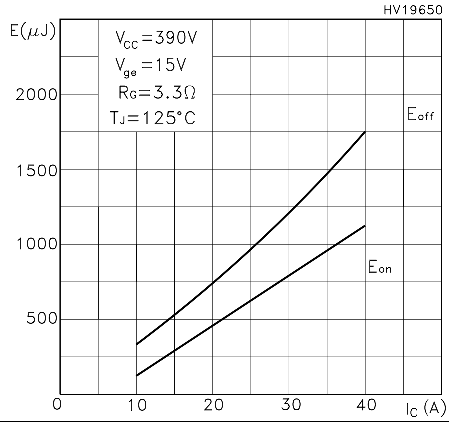


Figure 13. Thermal impedance

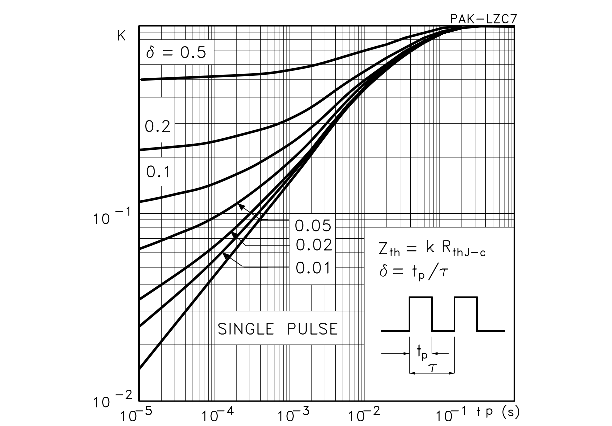


Figure 14. Turn-off SOA

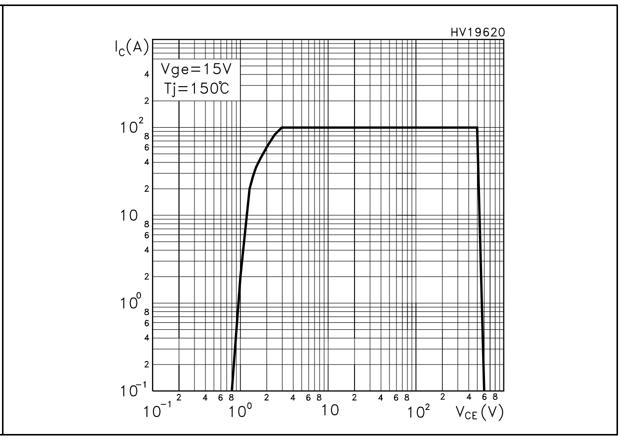
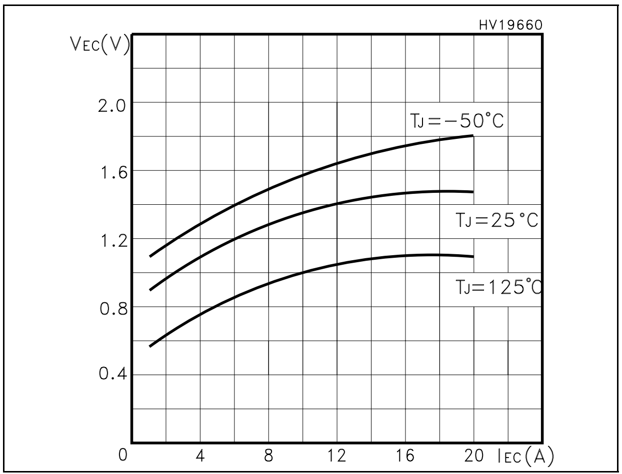


Figure 15. Emitter-collector diode characteristics



3 Test circuit

Figure 16. Test circuit for inductive load switching

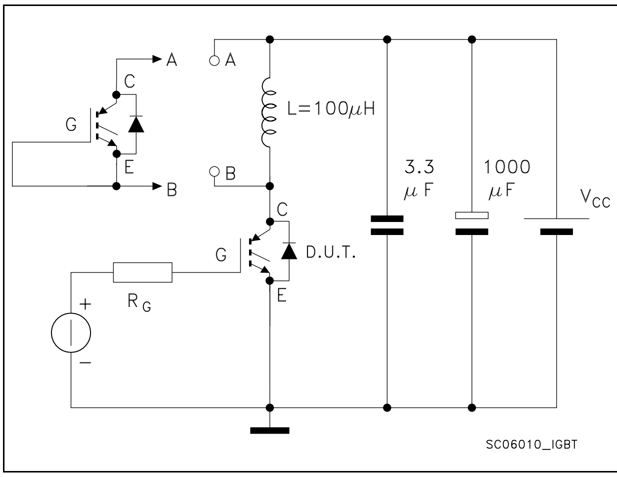


Figure 17. Gate charge test circuit

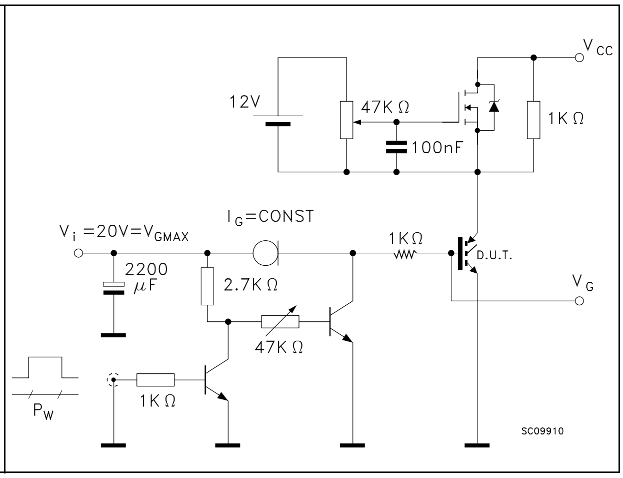


Figure 18. Switching waveforms

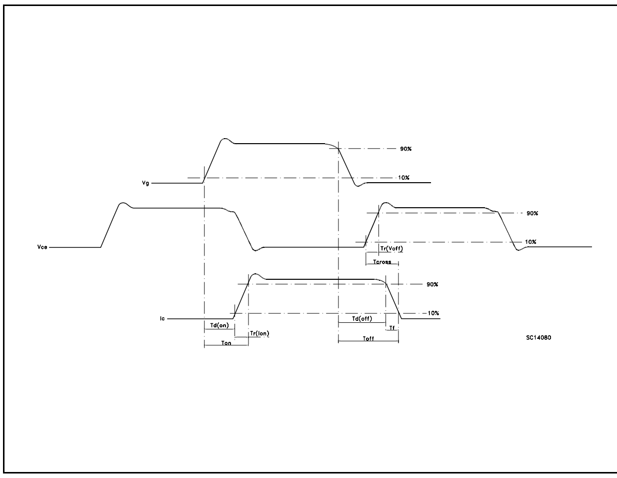
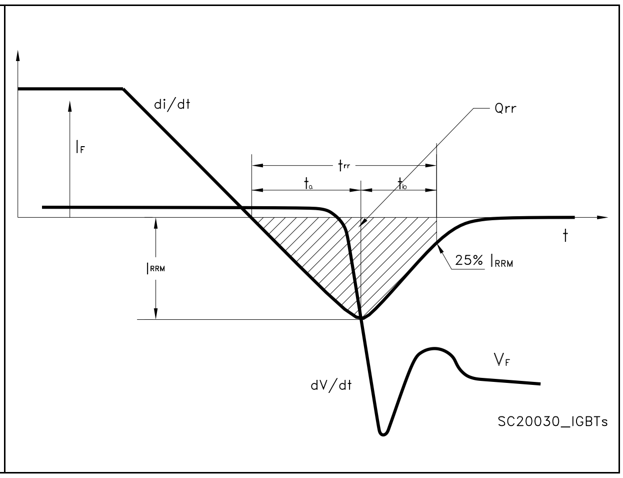


Figure 19. Diode recovery times waveform

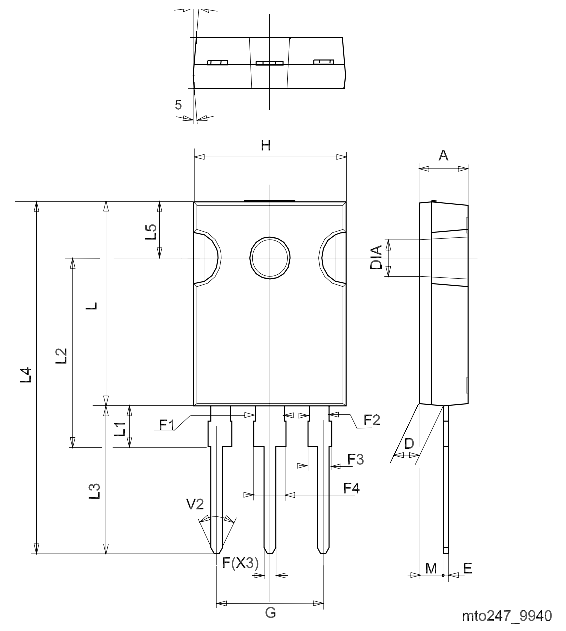


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.90		5.16	0.193		0.203
D	2.35		2.45	0.093		0.096
E	0.6		0.76	0.024		0.030
F	1.2		1.33	0.047		0.052
F1		3			0.118	
F2		2			0.078	
F3	1.9		2.13	0.075		0.084
F4	3.04		3.2	0.120		0.126
G		10.90			0.429	
H	15.77		16.03	0.621		0.631
L	20.83		21.09	0.820		0.830
L1	3.93		4.45	0.155		0.175
L2	18.72		19.18	0.737		0.755
L3	20.04		20.31	0.789		0.800
L4	40.88		41.40	1.609		1.630
L5	6.04		6.30	0.238		0.248
M	2		3		0.078	0.118
V		5°			5°	
V2		60°			60°	
Diam	3.56		3.66	0.140		0.144



5 Revision history

Table 8. Revision history

Date	Revision	Changes
12-Feb-2007	1	First release
19-Feb-2007	2	*Figure 5.* has been updated