2W Stereo Audio Amplifier

Features

- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Depop Circuitry Integrated**
- **Output Power at 1% THD+N, VDD=5V**
  --2.0W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Bridge-Tied Load (BTL) Supported**
- **Fully differential Input**
- **Shutdown Control Available**
- **Surface-Mount Power Package**
  20-Pin TSSOP-P & 20-Pin TQFN 4X4

Applications

- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

General Description

G1431 is a stereo audio power amplifier in 20pin TSSOP thermal pad package or 20-pin TQFN 4X4. It can drive 2W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage. Its THD is smaller than 1% under the above operation condition. To simplify the audio system design in the notebook application and to enlarge the driving power, G1431 supports the Bridge-Tied Load (BTL) mode for driving the speakers. For the low current consumption applications, the SHDN mode is supported to disable G1431 when it is idle. The current consumption can be reduced to 150μA (typically).

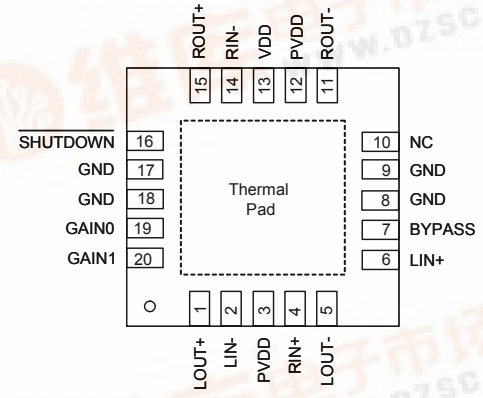
Amplifier gain is internally configured and controlled by two terminals (GAIN0, GAIN1). BTL gain settings of 6dB, 10dB, 15.6dB, 21.6dB are provided.

Ordering Information

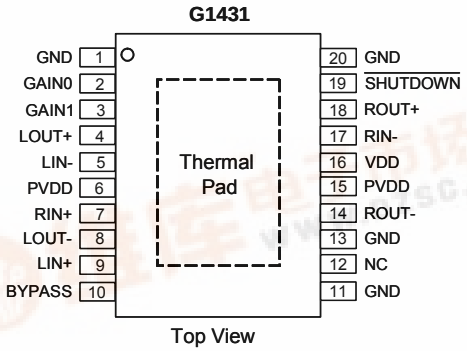
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G1431F2U	G1431	-40°C to +85°C	TSSOP-20 (FD)
G1431R9U	1431	-40°C to +85°C	TQFN4X4-20

Note: F2: TSSOP-20 (FD) R9:TQFN4X4-20
U: Tape & Reel

Pin Configuration



G1431 TQFN4X4-20



Top View
TSSOP-20 (FD)

Absolute Maximum Ratings

Supply Voltage, V_{CC} 6V
Operating Ambient Temperature Range
T_A . . . . -40°C to +85°C
Maximum Junction Temperature, T_J . . . . . 150°C
Storage Temperature Range, T_{STG} . . . .-65°C to+150°C
Reflow Temperature (soldering, 10sec) . . . . . .260°C

Power Dissipation (1)
$T_A \leq 25°C$ 2.7W
$T_A \leq 70°C$ 1.7W
Electrostatic Discharge, V_{ESD}
Human body mode . . . . . 3000V(2)

Note:
(1): Recommended PCB Layout
(2): Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, T_A=+25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage VDD	V_{DD}		4.5	5	5.5	V
High-Level Input voltage, V_{IH}	V_{IH}	$\overline{\text{SHUTDOWN}}$, GAIN0, GAIN1	2	---	---	V
Low-Level Input voltage, V_{IL}	V_{IL}	$\overline{\text{SHUTDOWN}}$, GAIN0, GAIN1	---	---	0.8	V
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2	---	5	50	mV
Supply Current in Mute Mode	I_{DD}	V_{DD} = 5V Stereo BTL	---	7.5	11	mA
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V	---	160	300	µA

(AC Operation Characteristics, V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω G=-2V/V	---	2	---	W
		THD = 1%, BTL, R_L = 8Ω G=-2V/V	---	1.2	---	
		THD = 10%, BTL, R_L = 4Ω G=-2V/V	---	2.5	---	
		THD = 10%, BTL, R_L = 8Ω G=-2V/V	---	1.6	---	
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω G=-2V/V	---	100	---	m%
		P_O = 1W, BTL, R_L = 8Ω G=-2V/V	---	60	---	
Maximum output power bandwidth	B_{OM}	THD = 5%	---	15	---	kHz
Power supply ripple rejection	PSRR	F=1kHz, BTL mode G=-2V/V C_{BYP}=1µF	---	68	---	dB
Channel-to-channel output separation		f = 1kHz	---	80	---	dB
Input impedance	ZI		See Table 2			MΩ
Signal-to-noise ratio		P_O = 500mW, BTL, G=-2V/V	---	90	---	dB
Output noise voltage	V_n	BTL,G=-2V/V, A Weighted filter	---	45	---	µV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

Typical Characteristics

Table of Graphs

		FIGURE
THD +N Total harmonic distortion plus noise	vs Frequency	1,2,7,8,13,14
	vs Output Power	3,4,5,6,9,10,11,12,15,16,17,18
V_n Output noise voltage	vs Frequency	21
Supply ripple rejection ratio	vs Frequency	19
Crosstalk	vs Frequency	20
P_O Output power	vs Load Resistance	22
P_D Power dissipation	vs Output Power	23

Total Harmonic Distortion Plus Noise vs Frequency

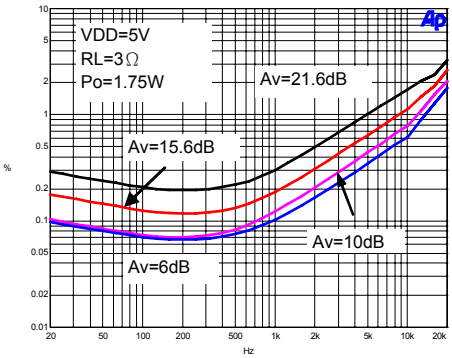


Figure 1

Total Harmonic Distortion Plus Noise vs Frequency

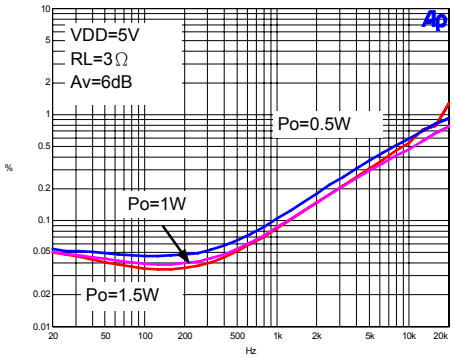


Figure 2

Total Harmonic Distortion Plus Noise vs Output Power

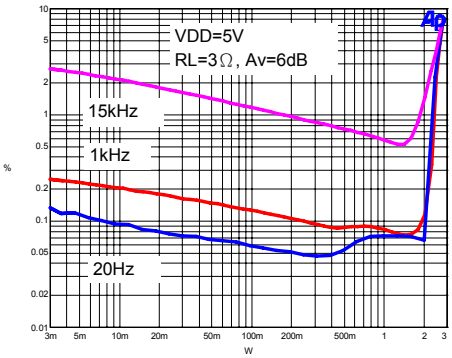


Figure 3

Total Harmonic Distortion Plus Noise vs Output Power

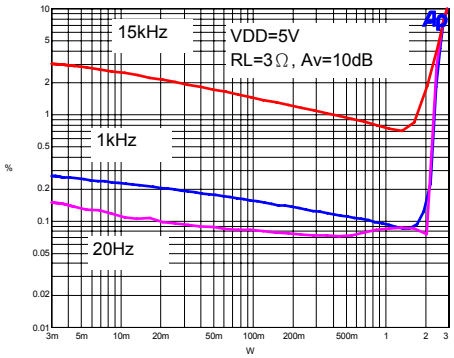


Figure 4

Typical Characteristics (continued)

Total Harmonic Distortion Plus Noise vs Output Power

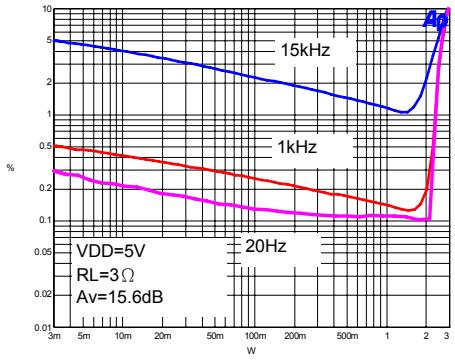


Figure 5

Total Harmonic Distortion Plus Noise vs Output Power

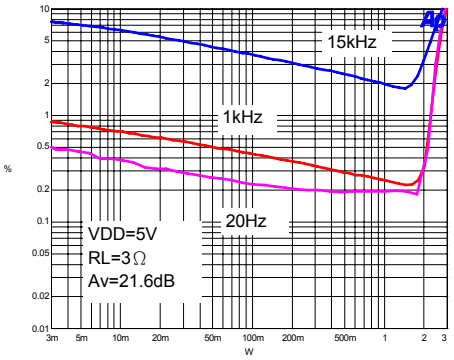


Figure 6

Total Harmonic Distortion Plus Noise vs Frequency

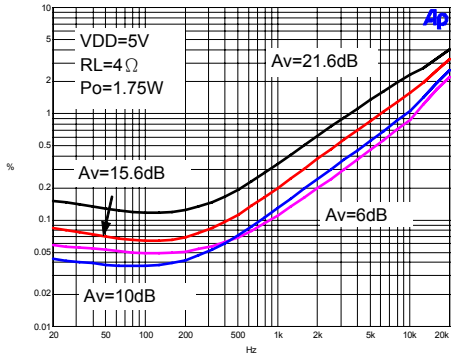


Figure 7

Total Harmonic Distortion Plus Noise vs Frequency

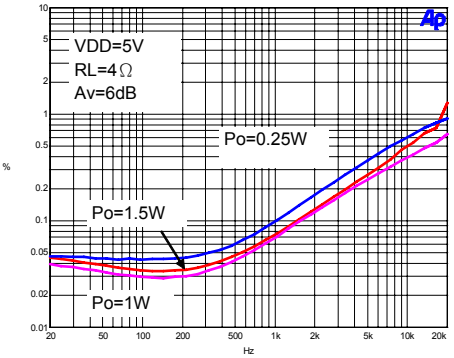


Figure 8

Total Harmonic Distortion Plus Noise vs Output Power

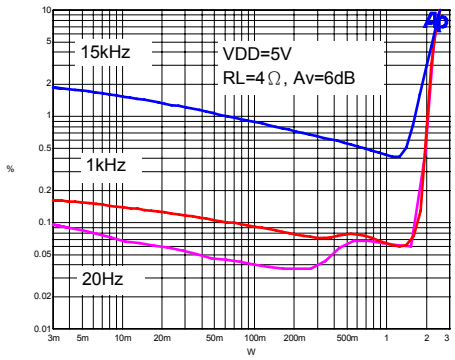


Figure 9

Total Harmonic Distortion Plus Noise vs Output Power

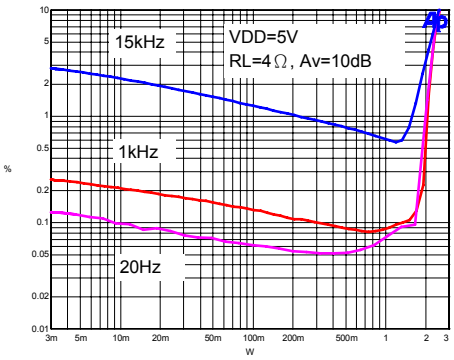


Figure 10

Typical Characteristics (continued)

Total Harmonic Distortion Plus Noise vs Output Power

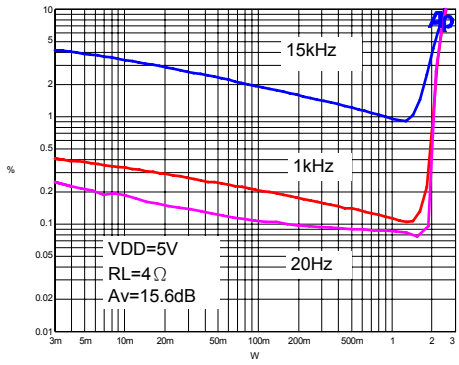


Figure 11

Total Harmonic Distortion Plus Noise vs Output Power

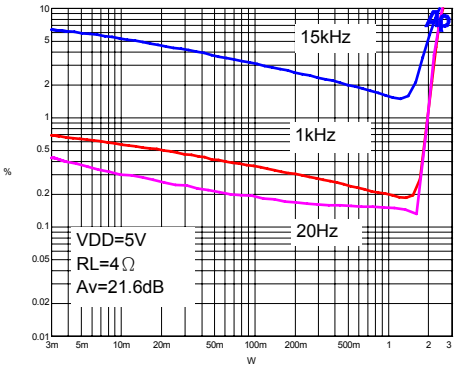


Figure 12

Total Harmonic Distortion Plus Noise vs Frequency

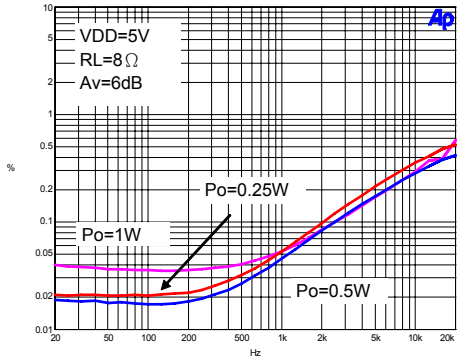


Figure 13

Total Harmonic Distortion Plus Noise vs Frequency

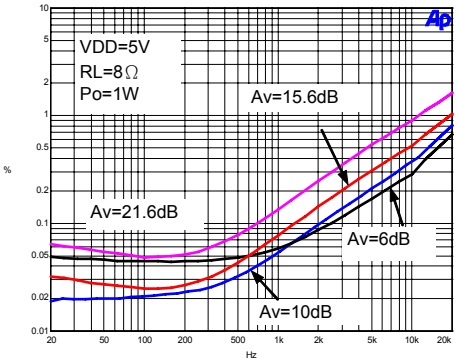


Figure 14

Total Harmonic Distortion Plus Noise vs Output Power

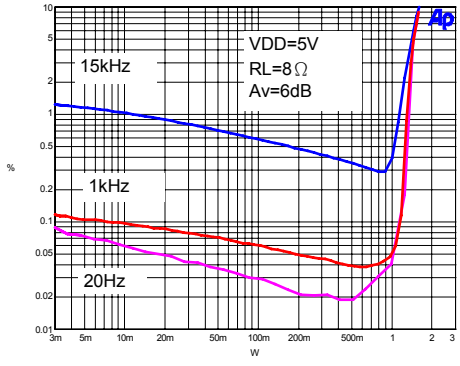


Figure 15

Total Harmonic Distortion Plus Noise vs Output Power

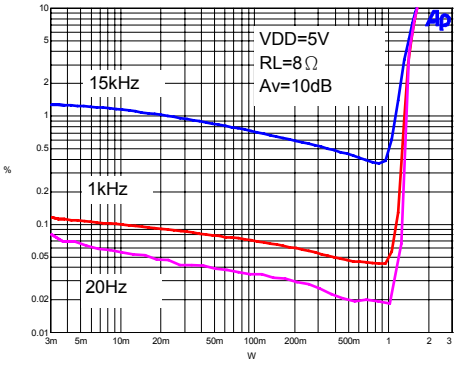


Figure 16

Typical Characteristics (continued)

Total Harmonic Distortion Plus Noise vs Output Power

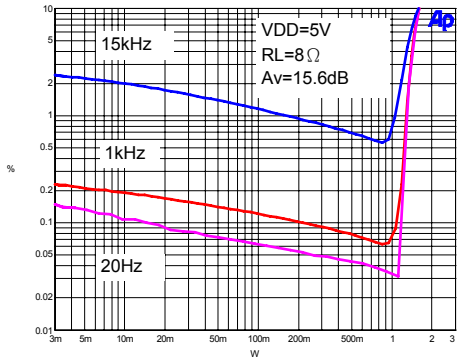


Figure 17

Total Harmonic Distortion Plus Noise vs Output Power

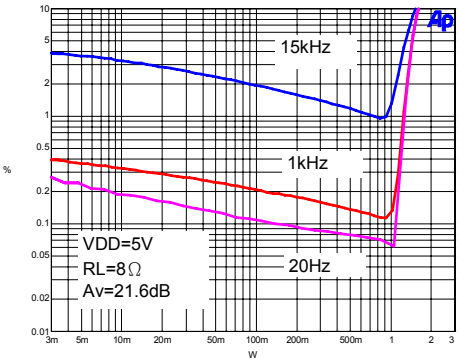


Figure 18

Supply Ripple Rejection Ratio vs Frequency

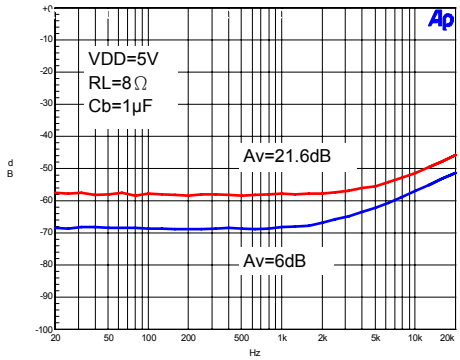


Figure 19

Channel Separation

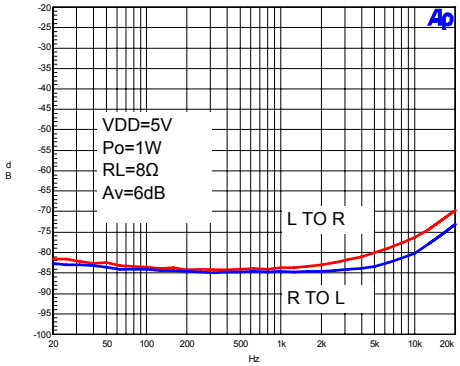


Figure 20

Output Noise vs Frequency

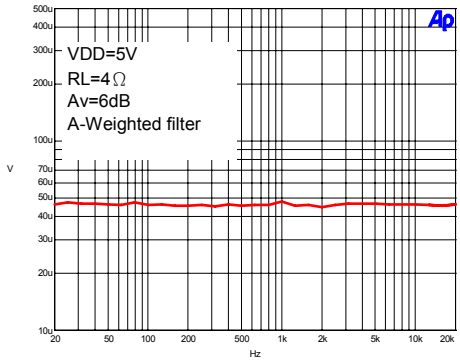


Figure 21

Output Power vs Load Resistance

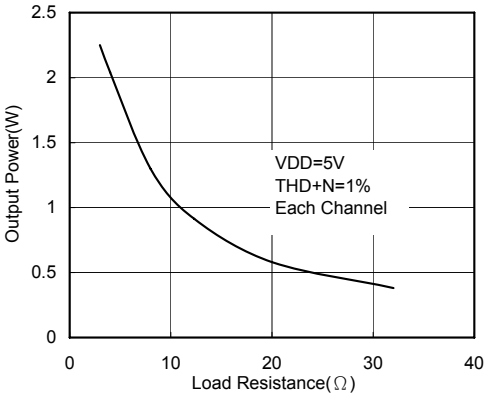


Figure 22

Typical Characteristics (continued)

Power Dissipation vs Output Power

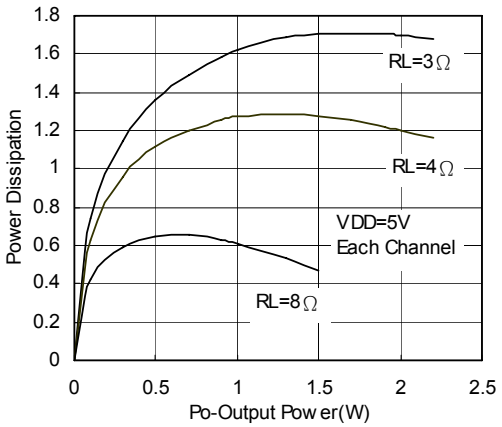
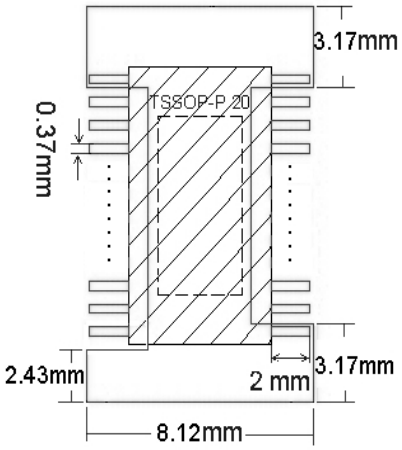


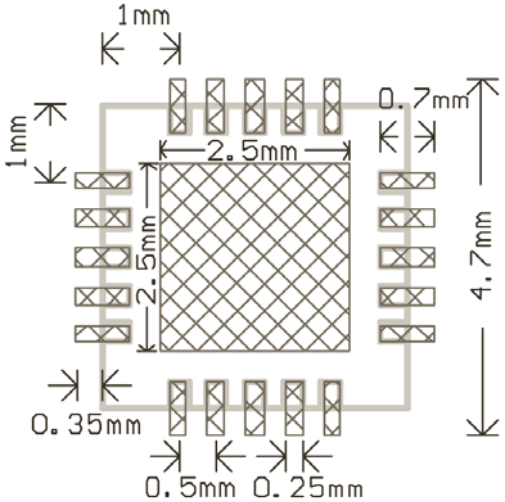
Figure 23

Recommended Minimum Footprint

TSSOP-20 (FD)



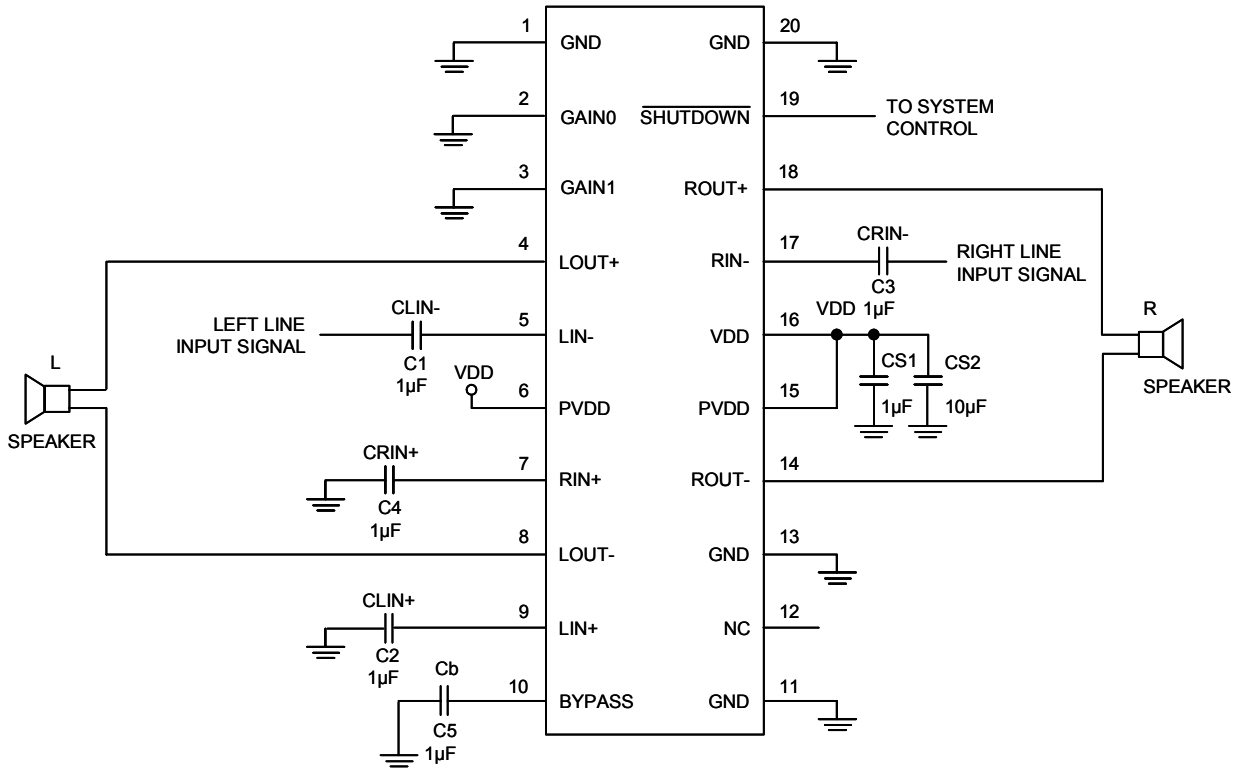
TQFN4X4-20



Pin Description

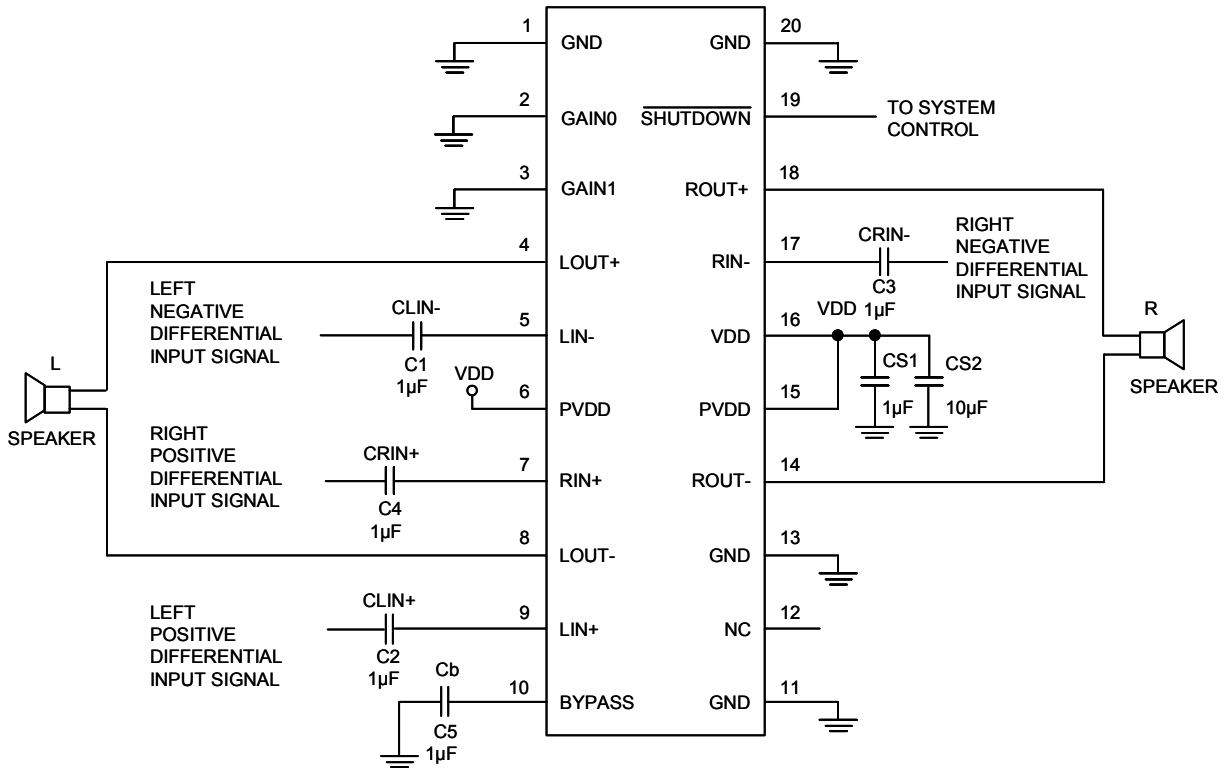
PIN		NAME	I/O	FUNCTION
TSSOP-20(FD)	TQFN4X4-20			
1,11,13,20	8,9,17,18	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
2	19	GAIN0	I	Bit 0 of gain control
3	20	GAIN1	I	Bit 1 of gain control
4	1	LOUT+	O	Left channel + output in BTL mode
5	2	LIN-	I	Negative left input for fully differential inputs.
6,15	3,12	PVDD		Power supply for output stages.
7	4	RIN+	I	Positive right input for fully differential inputs. AC ground for single-ended inputs.
8	5	LOUT-	O	Left channel - output in BTL mode
9	6	LIN+	I	Positive left input for fully differential inputs. AC ground for single-ended inputs.
10	7	BYPASS		Tap to voltage divider for internal mid-supply bias generator.
12	10	NC		NC
14	11	ROUT-	O	Right channel - output in BTL mode
16	13	VDD		Analog VDD input supply. This terminal needs to be isolated from PVDD to achieve highest performance.
17	14	RIN-	I	Negative right input for fully differential inputs.
18	15	ROUT+	O	Right channel + output in BTL mode
19	16	$\overline{\text{SHUTDOWN}}$	I	Places entire IC in shutdown mode when held low

Application Circuit



Typical G1431 Application Circuit Using Single-Ended Inputs

Application Circuit (continued)



Typical G1431 Application Circuit Using Differential Inputs

Application Information

Gain setting via GAIN0 and GAIN1 inputs

The internal gain setting is determined by two input terminals, GAIN0 and GAIN1. The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This will cause the internal input impedance, Z_I, to be dependent on the gain setting. Although the real input impedance will shift by 30% due to process variation from part-to-part, the actual gain settings are controlled by the ratios of the resistors and the actual gain distribution from part-to-part is quite good.

Table 1

GAIN0	GAIN1	A_V (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

Input Resistance

The typical input impedance at each gain setting is given in the Table 2. Each gain setting is achieved by varying the input resistance of the amplifier, which can be over 6 times from its minimum value to the maximum value. As a result, if a single capacitor is used in the input high pass filter, the –3dB or cut-off frequency will be also change over 3.5 times. To reduce the variation of the cut-off frequency, an additional resistor can be connected from the input pin of the amplifier to the ground, as shown in the figure below. With the extra resistor, the cut-off frequency can be re-calculated using equation : $f_{-3dB}= 1/ 2\pi C(R||R_I)$. Using small external R can reduce the variation of the cut-off frequency. But the side effect is small external R will also let $(R||R_I)$ become small, the cut-off frequency will be larger and degraded the bass-band performance. The other side effect is with extra power dissipation through the external resistor R to the ground. So using the external resistor R to flatting the variation of the cut-off frequency, the user must also consider the bass-band performance and the extra power dissipation to choose the accepted external resistor R value.

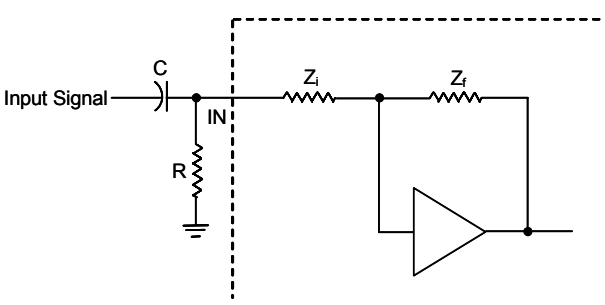


Table 2

Zi (kΩ)	A_V (dB)
30	21.6
45	15.6
70	10
90	6

Input Capacitor

In the typical application, an input capacitor C_i is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier, Z_i, form a high-pass filter with the –3dB determined by the equation: $f_{-3dB}= 1/ 2\pi R_I C_i$

The value of C_i is important to consider as it directly affects the bass performance of the application circuit. For example, if the input resistor is 15kΩ, the input capacitor is 1µF, the flat bass response will be down to 10.6Hz.

Because the small leakage current of the input capacitors will cause the dc offset voltage at the input to the amplifier that reduces the operation headroom, especially at the high gain applications. The low-leakage tantalum or ceramic capacitors are suggested to be used as the input coupling capacitors. When using the polarized capacitors, it is important to let the positive side connecting to the higher dc level of the application.

Power Supply Decoupling

The G1431 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to make sure the output total harmonic distortion (THD) as low as possible. The optimum decoupling is using two capacitors with different types that target different types of noise on the power supply leads. For high frequency transients, spikes, a good low ESR ceramic capacitor works best, typically 0.1µF/1µF used and placed as close as possible to the G1431 VDD lead. A larger aluminum electrolytic capacitor of 10µF or greater placed near the device power is recommended for filtering low-frequency noise.

Optimizing DEPOP Operation

Circuitry has been implemented in G1431 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B x 170k\Omega) \leqq 1/(C_I*(R_I+R_F))$. Where 170kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain set-

ting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

De-popping circuitry of G1431 is shown as below Figure 1. The PNP transistor limits the voltage drop across the 120kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

For better performance, C_B is recommended to be at least 1.5 times of input coupling capacitor C_I. For example, if using 1µF input coupling capacitor, 2.2µF ceramic or tantalum low-ESR capacitors are recommended to achieve the better THD performance.

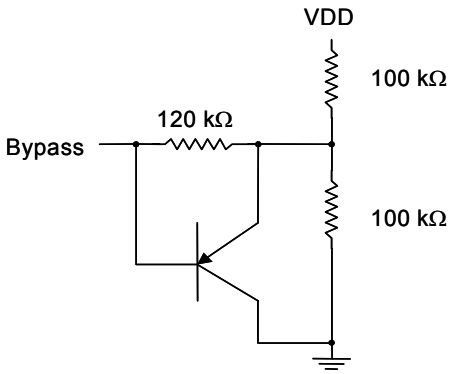


Figure 1

Bridged-Tied Load Mode Operation

G1431 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure 2 shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage V_O(PP) on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc offsets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.

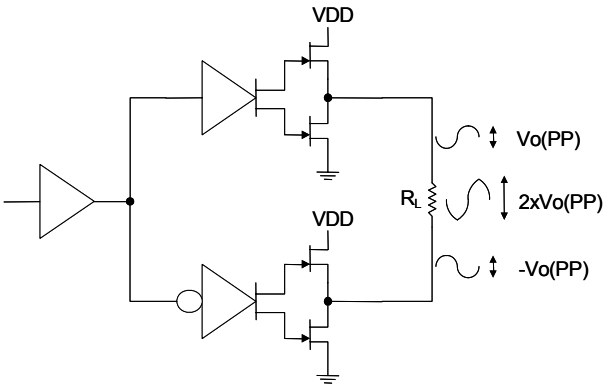


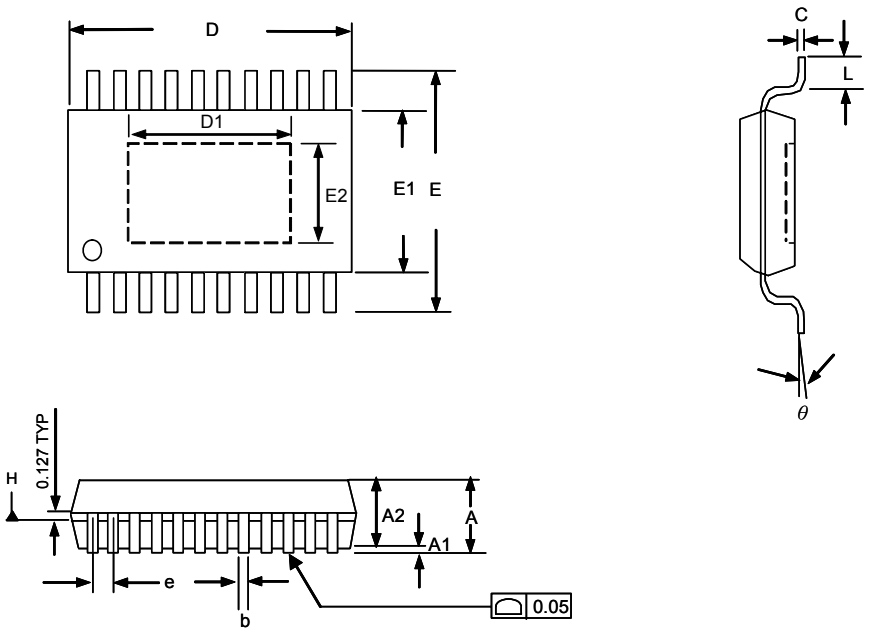
Figure 2

Shutdown mode

When the normal operation, the SHUTDOWN pin should be held high. Pulling SHUTDOWN low will mute the outputs and deactivate the most of the circuits. At this moment, the current of this device will be reduced to about 160µA to save the battery energy. The SHUTDOWN pin should never be left unconnected during the normal applications.

INPUT *	AMPLIFIER STATE
SHUTDOWN	OUTPUT
Low	Mute
High	BTL
* Inputs should never be left unconnected X= do not care	

Package Information

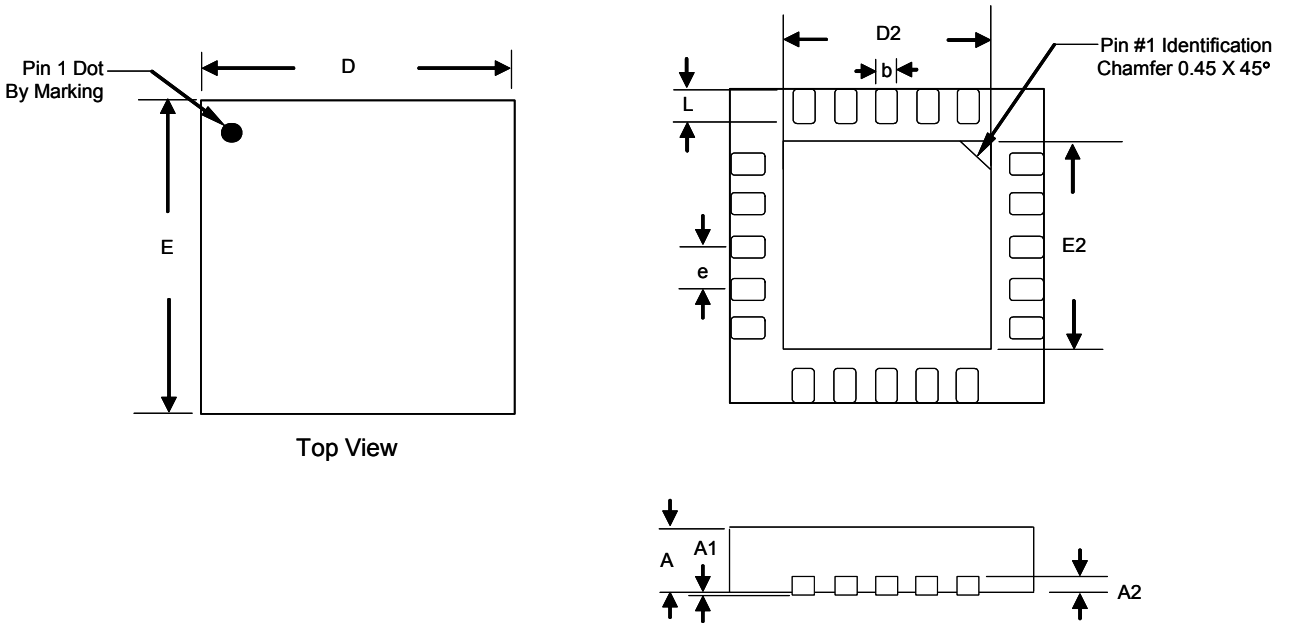


TSSOP-20 (FD) Package

Note:

1. JEDCE outline: MP-153 AC/MO-153 ACT (thermally enhanced variations only)
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension “E1” does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the “b” dimension at maximum material conditions. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimensions “D” and “E1” to be determined at datum plane “H”.

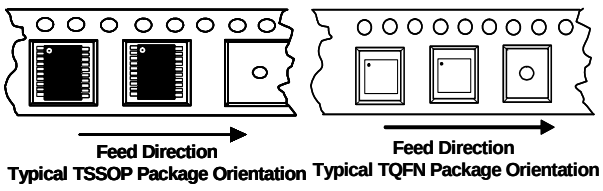
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-----	-----	1.20	-----	-----	0.047
A1	0.00	-----	0.15	0.000	-----	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.20	-----	-----	0.008	-----	-----
D	6.40	6.50	6.60	0.252	0.256	0.260
D1	3.90	-----	4.40	0.154	-----	0.173
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.70	-----	3.20	0.106	-----	0.126
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	-----	8°	0°	-----	8°



TQFN4X4-20 Package

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-----	0.050	0.000	-----	0.002
A2	0.195	0.203	0.211	0.008	0.008	0.008
b	0.180	0.230	0.280	0.007	0.009	0.011
D	3.950	4.000	4.050	0.156	0.157	0.159
D2	2.400	2.500	2.600	0.094	0.098	0.102
E	3.950	4.000	4.050	0.156	0.157	0.159
E2	2.400	2.500	2.600	0.094	0.098	0.102
e	0.500 BSC			0.020 BSC		
L	0.350	0.400	0.450	0.014	0.016	0.018

Taping Specification



PACKAGE	Q'TY/ REEL
TSSOP-20 (FD)	2,500 ea
TQFN4X4-20	3,000 ea