Pb Free Plating Product

GTM CORPORATION

ISSUED DATE :2005/04/21
REVISED DATE :2005/07/14B

G2N7002K

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

BV_{DSS}	60V
$R_{DS(ON)}$	2Ω
I_D	640mA

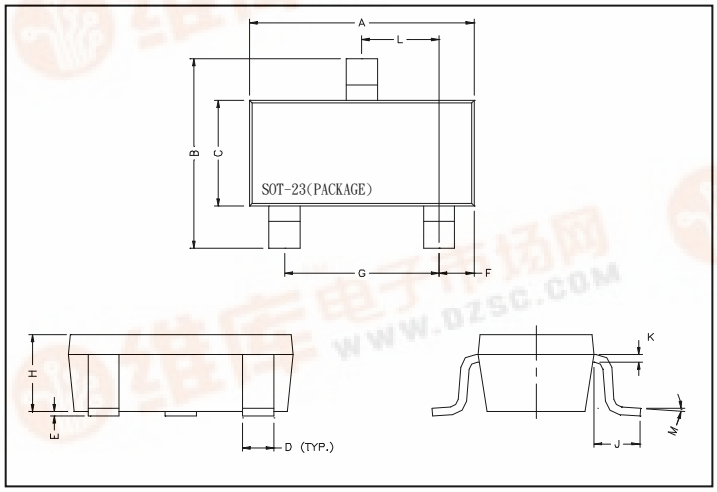
Description

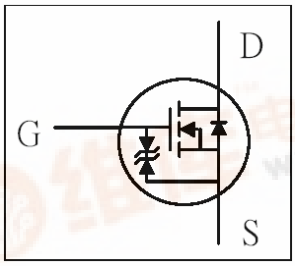
The G2N7002K utilized advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device.
The G2N7002K is universally used for all commercial-industrial applications.

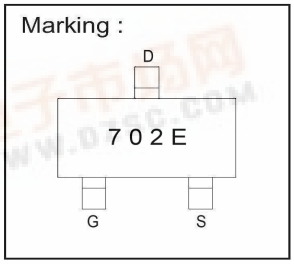
Features

*Simple Drive Requirement
*Small Package Outline
*RoHS Compliant

Package Dimensions







REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	1.90	REF.
B	2.40	2.80	H	1.00	1.30
C	1.40	1.60	K	0.10	0.20
D	0.35	0.50	J	0.40	-
E	0	0.10	L	0.85	1.15
F	0.45	0.55	M	0°	10°

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current[3], V_{GS}@10V	I_D @T_A=25℃	640	mA
Continuous Drain Current[3], V_{GS}@10V	I_D @T_A=70℃	500	mA
Pulsed Drain Current[1,2]	I_{DM}	950	mA
Power Dissipation	P_D @T_A=25℃	1.38	W
Linear Derating Factor		0.01	W/℃
Operating Junction and Storage Temperature Range	Tj, Tstg	-55 ~ +150	℃

Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient[3] Max.	Rthj-a	90	℃/W

Electrical Characteristics(Tj = 25℃ Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	60	-	-	V	V_{GS}=0, I_D=250uA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle Tj$	-	0.06	-	V/℃	Reference to 25℃, I_D=1mA
Gate Threshold Voltage	$V_{GS(th)}$	1.0	-	3.0	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transconductance	g_{fs}	-	600	-	mS	V_{DS}=10V, I_D=600mA
Gate-Source Leakage Current	I_{GSS}	-	-	±10	uA	V_{GS}= ±20V
Drain-Source Leakage Current(Tj=25℃)	I_{DSS}	-	-	1	uA	V_{DS}=60V, V_{GS}=0
Drain-Source Leakage Current(Tj=70℃)		-	-	100	uA	V_{DS}=48V, V_{GS}=0
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	-	2	Ω	V_{GS}=10V, I_D=500mA
		-	-	4		V_{GS}=4.5V, I_D=200mA
Total Gate Charge[2]	Q_g	-	1	1.6	nC	I_D=600mA V_{DS}=50V V_{GS}=4.5V
Gate-Source Charge	Q_{gs}	-	0.5	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	0.5	-		
Turn-on Delay Time[2]	$T_{d(on)}$	-	12	-	ns	V_{DS}=30V I_D=600mA V_{GS}=10V R_G=3.3Ω R_D=52Ω
Rise Time	T_r	-	10	-		
Turn-off Delay Time	$T_{d(off)}$	-	56	-		
Fall Time	T_f	-	29	-		
Input Capacitance	C_{iss}	-	32	50	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
Output Capacitance	C_{oss}	-	8	-		
Reverse Transfer Capacitance	C_{rss}	-	6	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage[2]	V_{SD}	-	-	1.2	V	I_S=200mA, V_{GS}=0V

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width≦300us, duty cycle≦2%.

3. Surface mounted on 1 in^2 copper pad of FR4 board; 270℃/W when mounted on Min. copper pad.

Characteristics Curve

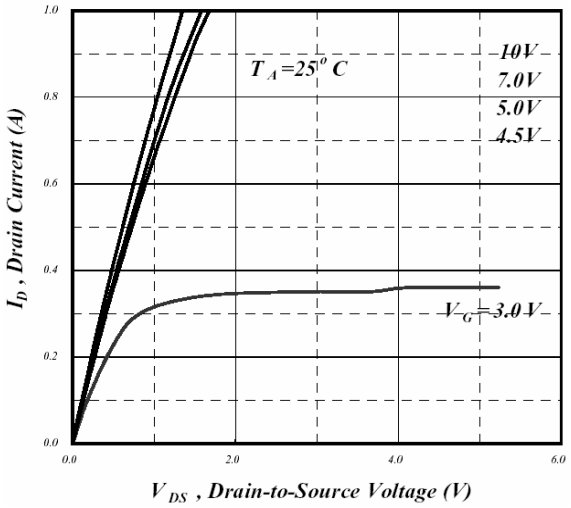


Fig 1. Typical Output Characteristics

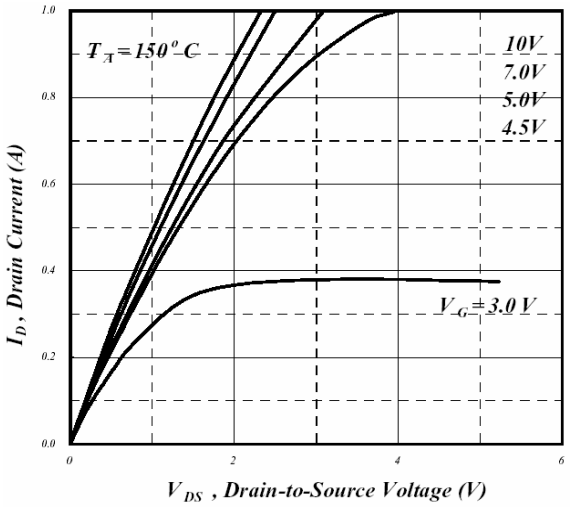


Fig 2. Typical Output Characteristics

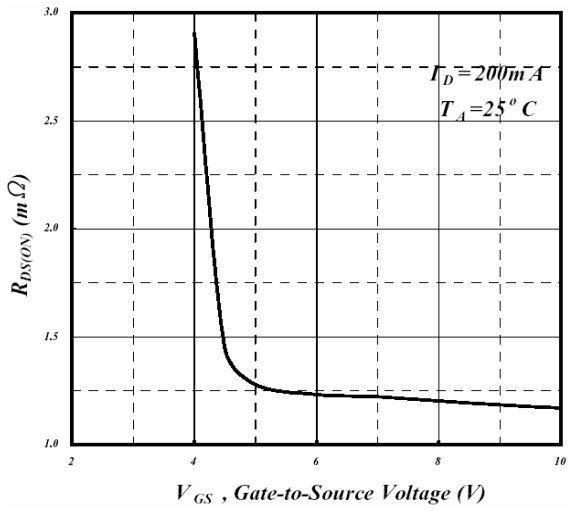


Fig 3. On-Resistance v.s. Gate Voltage

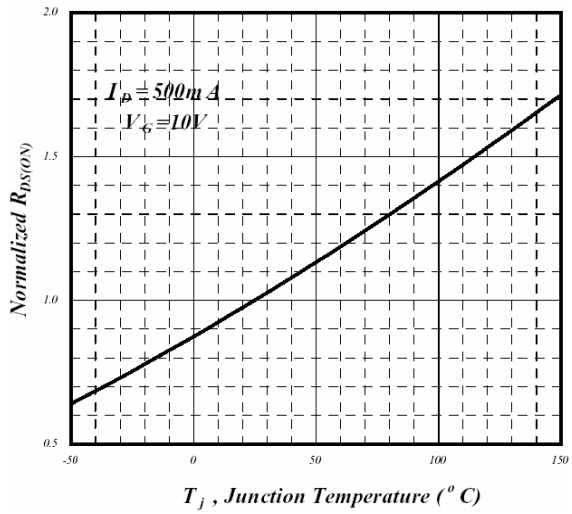


Fig 4. Normalized On-Resistance v.s. Junction Temperature

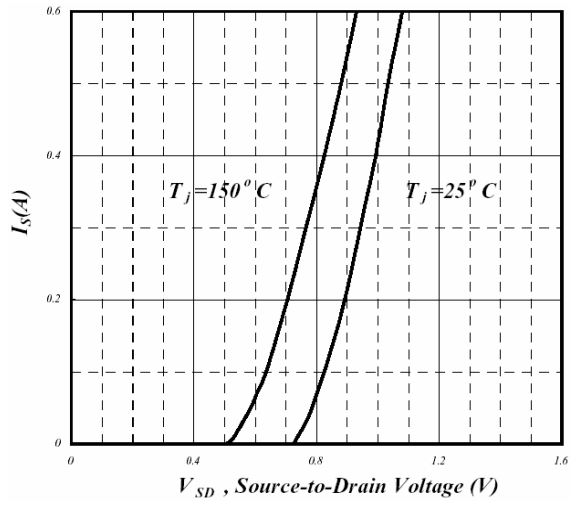


Fig 5. Forward Characteristics of Reverse Diode

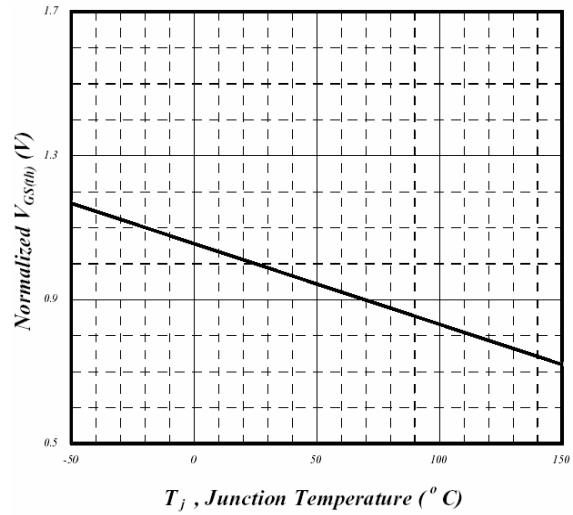


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

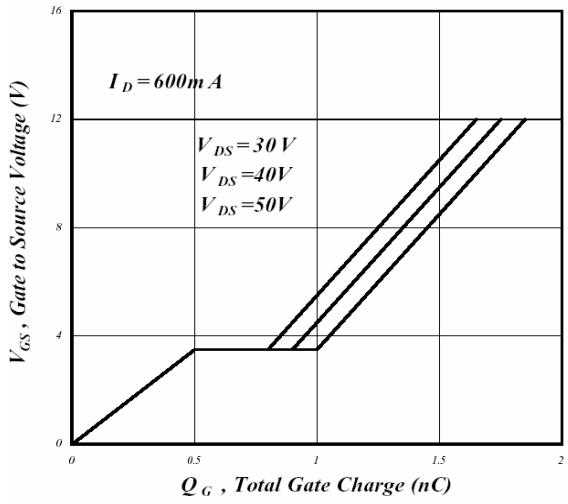


Fig 7. Gate Charge Characteristics

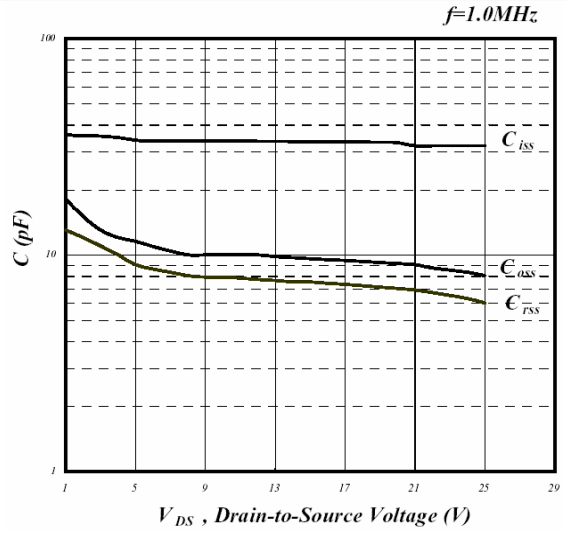


Fig 8. Typical Capacitance Characteristics

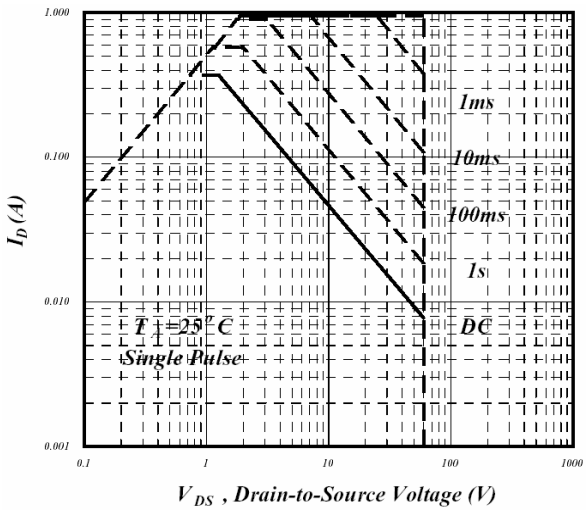


Fig 9. Maximum Safe Operating Area

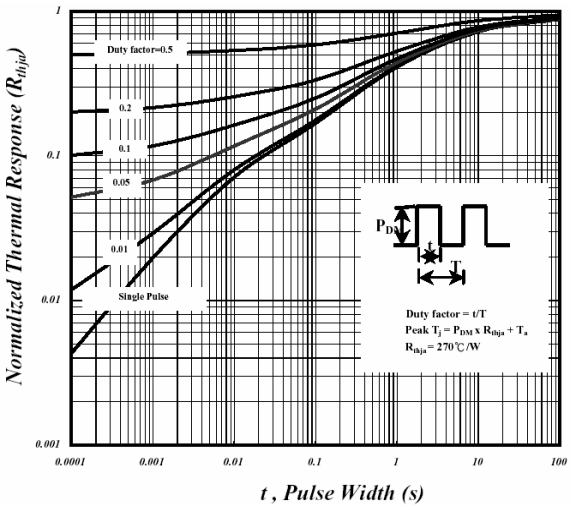


Fig 10. Effective Transient Thermal Impedance

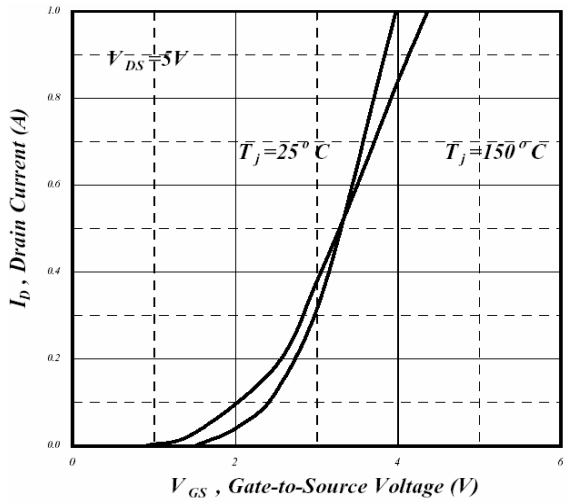


Fig 11. Transfer Characteristics

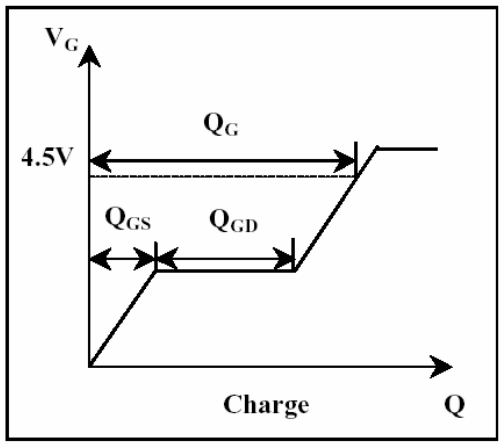


Fig 12. Gate Charge Waveform

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