DDR Termination Regulator

Features

- Support Both DDR I (1.25VTT) and DDR II (0.9 VTT) Requirements
- Input Voltage Range: 3.3V to 5.5V
- VLDOIN Voltage Range: 1.2V to 3.6V
- Requires Only 20µF Ceramic Output Capacitance
- Supports High-Z in S3 and Soft-Off in S5
- Integrated Divider Tracks 1/2 VDDQSNS for Both VTT and VTTREF
- Remote Sensing (VTTSNS)
- ±20mV Accuracy for VTT and VTTREF
- 10mA Buffered Reference (VTTREF)
- Built-In Soft-Start
- Over Current Protection
- Thermal Shutdown Protection
- MSOP-10 and MSOP-10(Exposed Pad) Package

Applications

- DDR I/II Memory Termination
- SSTL−2, SSTL−18
- HSTL Termination

General Description

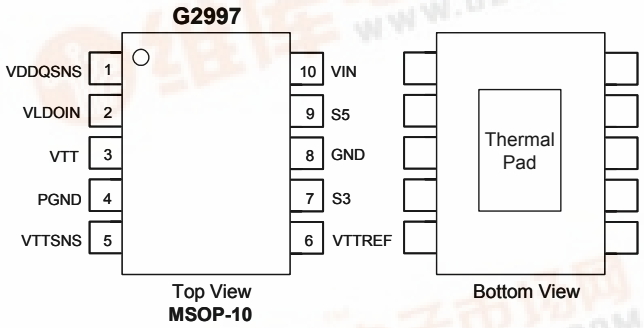
The G2997 is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost/ low-external component count systems. The G2997 maintains a high speed operational amplifier that provides fast load transient response and only requires 20µF (2x10µF) of ceramic output capacitance. The G2997 supports remote sensing functions and all features required to power the DDR I / DDR II VTT bus termination according to the JEDEC specification. In addition, the G2997 includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (Shutdown). The G2997 is available in the thermally efficient 10pin MSOP and MSOP (Exposed PAD).

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G2997P7U	G2997	-40°C~85°C	MSOP-10
G2997F6U	G2997	-40°C~85°C	MSOP-10 (FD)

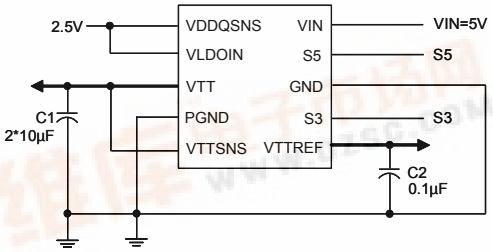
Note: P7: MSOP-10 F6: MSOP-10 (FD)
U: Tape & Reel
(FD): Thermal Pad

Pin Configuration



Note: Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Typical Application Circuit



Absolute Maximum Ratings (1)

Supply Voltage Range

VIN, VLDOIN, VTTSNS, VDDQSNS, S3, S5..-0.3V to +6V

PGND . . . . . .-0.3V to 0.3V

Output Voltage Range

VTT, VTTREF . . . . . .-0.3V to 6V

Maximum Junction Temperature,T_J . . . .160°C

Storage Temperature Range, T_{STG}.-55°C to +160°C

Reflow Temperature (soldering, 10sec). . . . . 260°C

Thermal Resistance Junction to Ambient, (θ_{JA})

MSOP-10 . . . . . 120°C/W

MSOP-10 (FD) . . . . 60°C/W(3)

Recommend Operating Range (1) (2)

VIN . . . . . .3.3V to 5.5V

S3, S5 . . . . . .-0.1V to 5.5V

VDDQSNS. . . . . .1.6V to 3.6V

VLDOIN . . . . . .1.2V to 3.6V

PGND . . . . . .-0.1V to 0.1V

Operating Ambient Temperature Range

T_A . . . .-40°C to 85°C

Note:

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) VLDOIN, VTTSNS, VDDQSNS, S3, S5 must be lower than VIN on operation.

(3) Please refer to PCB size described in EV2997-10.

Electrical Characteristics

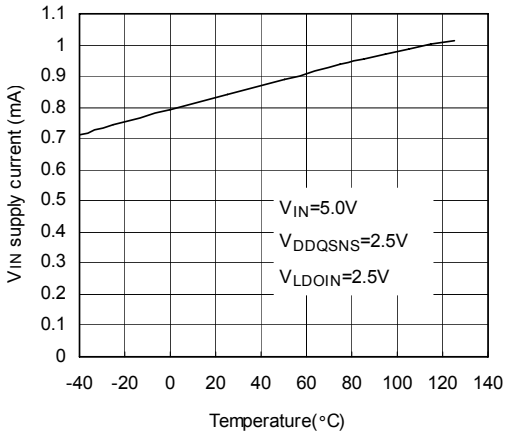
Specifications with standard typeface are for T_A=25°C, V_{IN}=5V, VLDOIN=2.5V and VDDQSNS=2.5V. Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, VIN	I_{VIN}	V_{VIN}=5V, no load, S5=5V, S3 =5V	0.5	0.8	2	mA
Standby current, VIN	I_{VINSTB}	V_{VIN}=5V, no load, S5=5V, S3 =0V	---	110	200	µA
Shutdown current, VIN	I_{VINSDN}	V_{VIN}=5V, no load, S5=0V, S3 =0V	---	---	1	µA
Supply current, VLDOIN	I_{VLDOIN}	V_{VIN}=5V, no load, S5=5V, S3 =5V	---	0.03	2	mA
Standby current, VLDOIN	$I_{VLDOINSTB}$	V_{VIN}=5V, no load, S5=5V, S3 =0V	---	0.1	10	µA
Shutdown current, VLDOIN	$I_{VLDOINSDN}$	V_{VIN}=5V, no load, S5=0V, S3 =0V	---	0.1	1	µA
VDDQSNS input Impedance	$Z_{VDDQSNS}$	V_{VIN}=5V, S5=5V, S3 =5V	---	200	---	KΩ
VTTSNS input current	I_{VTTSNS}	V_{VIN}=5V, S5=5V, S3 =5V	---	0.3	1	µA
VTT output voltage	VTT	(DDR I/DDR II)	---	1.25/0.9	---	V
VTT Output Voltage Load Regulation (VTTREF-VTT)	V_{OS}VTT	I_{VTT}=0	-20	---	20	mV
		$\|I_{VTT}\|$<1.5A	-30	---	30	
		$\|I_{VTT}\|$<3A	-40	---	40	
VTT Source Current limit	$I_{VTTOCLSRC}$	VTT=VDDQSNS/2 *0.95, PGOOD=Hi	3	4	---	A
		VTT=0	1.5	2	---	
VTT Sink Current limit	$I_{VTTOCLSNK}$	VTT=VDDQSNS/2 *1.05, PGOOD=Hi	3	4	---	A
		VTT=$V_{VDDQSNS}$	1.5	2	---	
VTT leakage current in S3 mode	I_{VTTLK}	S3=0V, S5=5V	---	0.01	---	µA
VTT Discharge Current	$I_{DISCHARGE}$	S5=0V, VDDQSNS=0, VTT=0.5V	10	20	---	mA
VTTREF output voltage	V_{TTREF}	(DDR I/DDR II)	---	1.25/0.9	---	V
VTTREF Voltage Load Regulation	ΔV_{TTREF}	|IVTTREF|<10mA	-20	---	20	mV
High Level Input Voltage	V_{IH}	S3 and S5 pin	1.6	---	---	V
Low Level Input Voltage	V_{IL}	S3 and S5 pin	---	---	1	V
Logic input leakage current	I_{ILEAK}	S3 and S5 pin	-1	---	1	µA
Thermal Shutdown	T_{SD}		---	160	---	°C
Thermal Shutdown Hystersis			---	20	---	°C

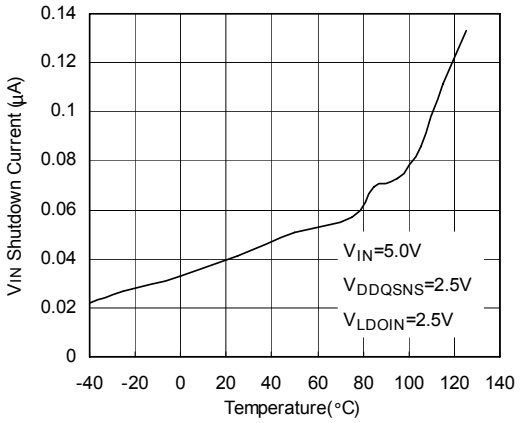
Typical Performance Characteristics

C_{VLDOIN}=10µF/MLCC/X5R, C_{VIN}=1µF/MLCC/X5R, C_{VTTREF} =0.1µF,C_{VTT}=20µF/X5R/MLCC unless otherwise noted.

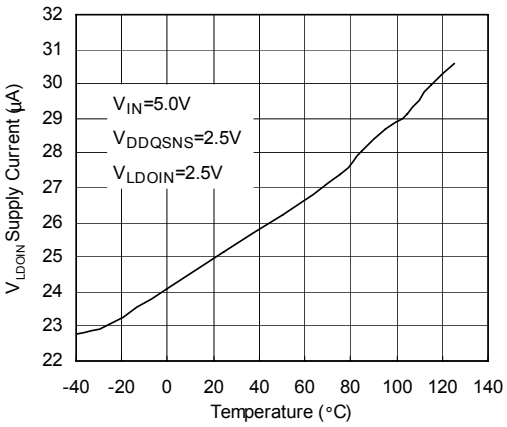
V_{IN} Supply Current vs Temperature



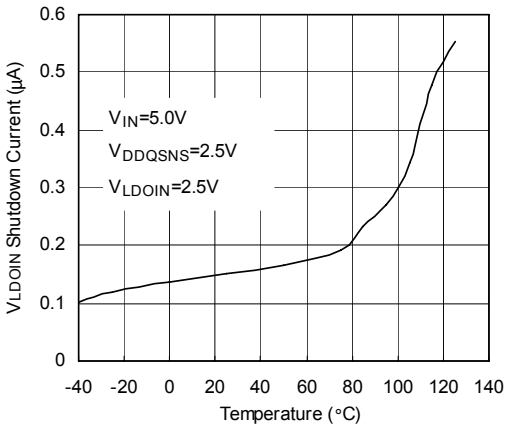
V_{IN} Shutdown Current vs Temperature



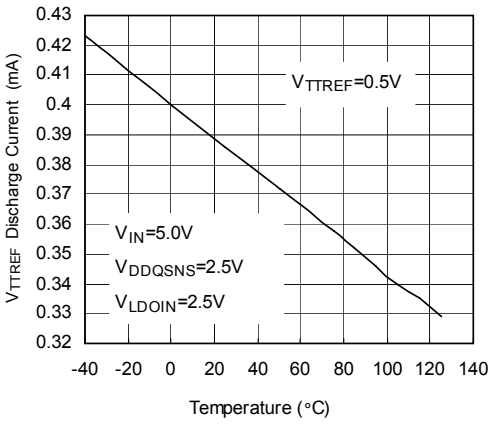
V_{LDOIN} Supply Current vs Temperature



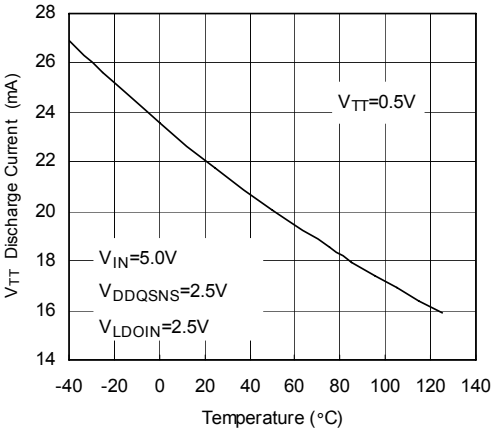
V_{LDOIN} Shutdown Current vs Temperature



V_{TTREF} Discharge Current vs Temperature

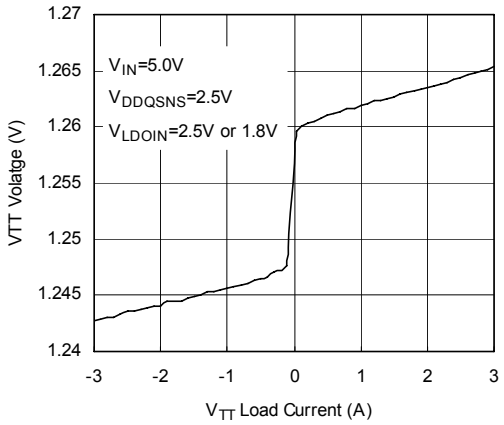


V_{TT} Discharge Current vs Temperature

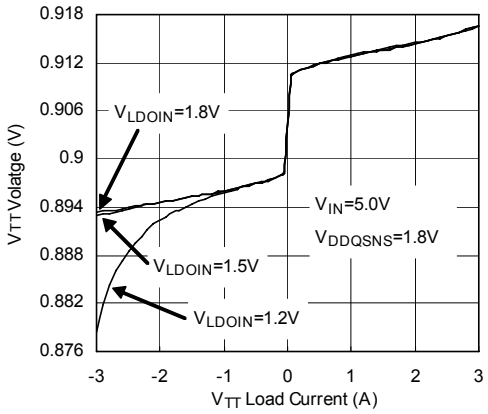


Typical Performance Characteristics (continued)

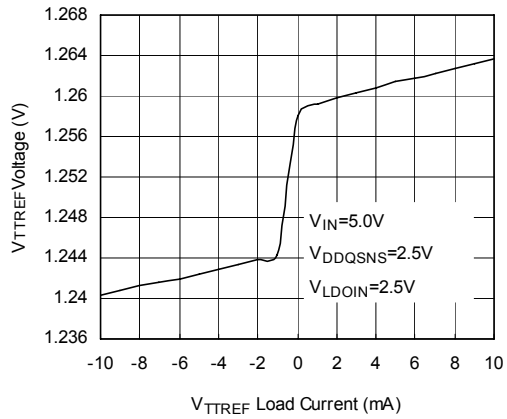
V_{TT} Voltage Regulation vs V_{TT} Load Current (DDR I)



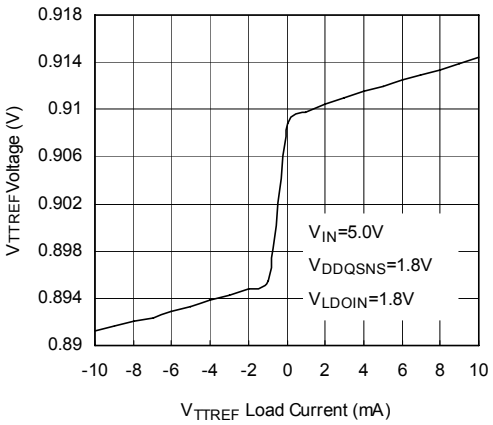
V_{TT} Voltage Regulation vs V_{TT} Load Current (DDR II)



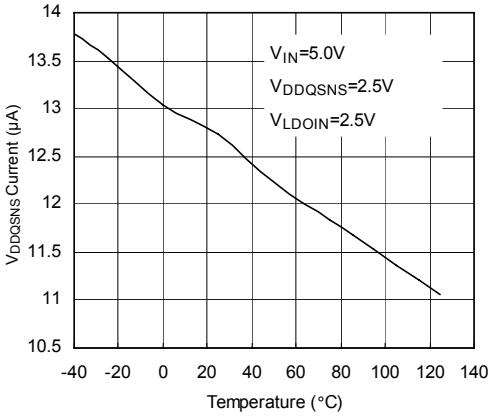
V_{TTREF} Voltage Load Regulation vs V_{TTREF} Load Current (DDR I)



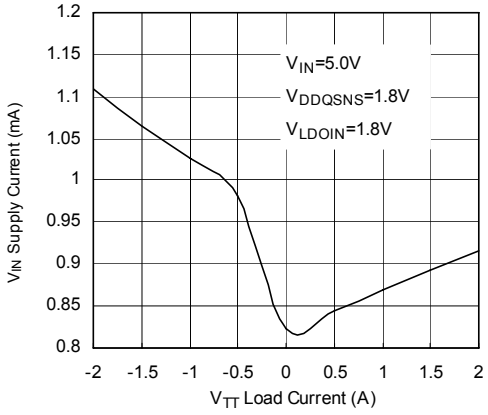
V_{TTREF} Voltage Load Regulation vs V_{TTREF} Load Current (DDR II)



V_{DDQSNS} Current vs Temperature

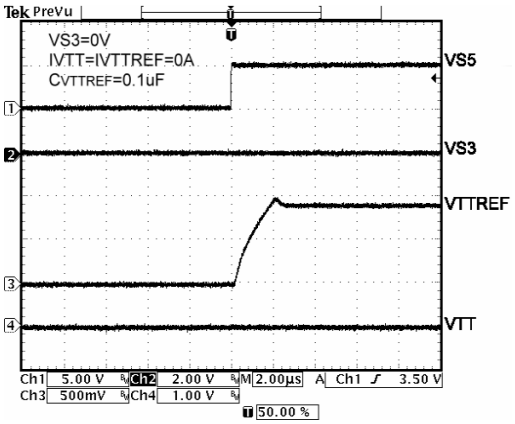


V_{IN} Supply Current vs V_{TT} Load Current

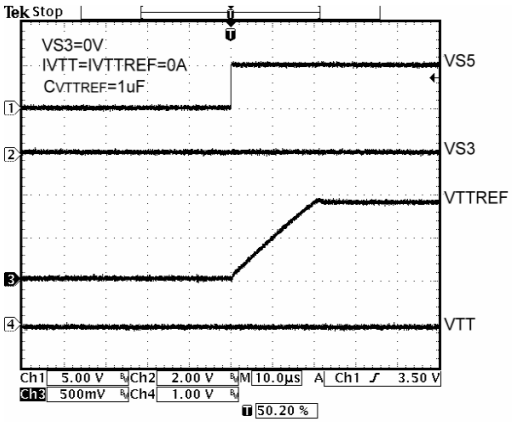


Typical Performance Characteristics (continued)

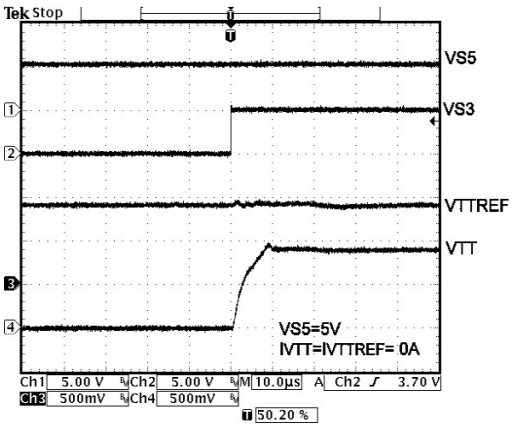
Start Up Waveforms S5 Low to High



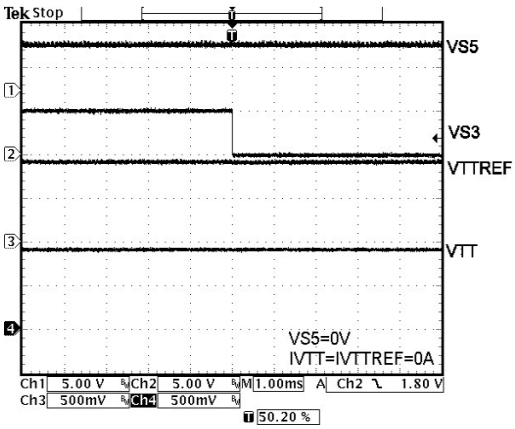
Start Up Waveforms S5 Low to High



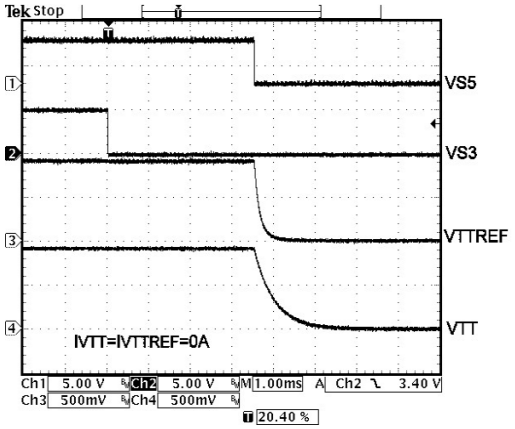
Start Up Waveforms S3 Low to High



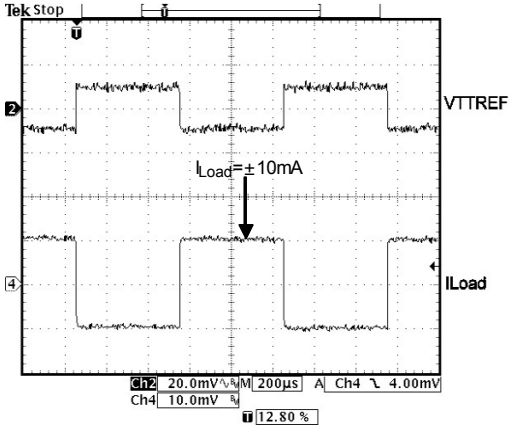
Shutdown Waveforms S3 High to Low



Shutdown Waveforms S3 and S5 High to Low

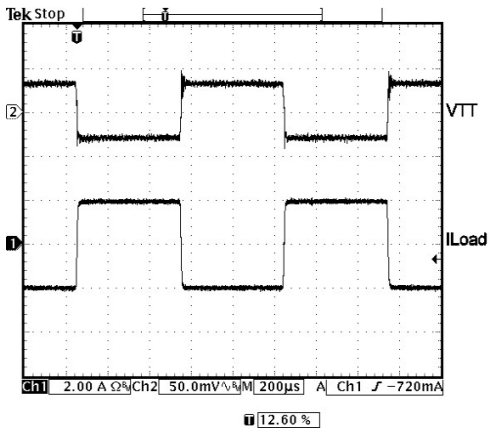


V_{TTREF} Voltage Transient Response



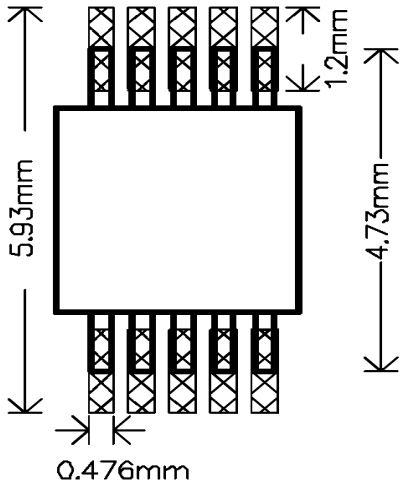
Typical Performance Characteristics (continued)

V_{TT} Voltage Load Transient Response

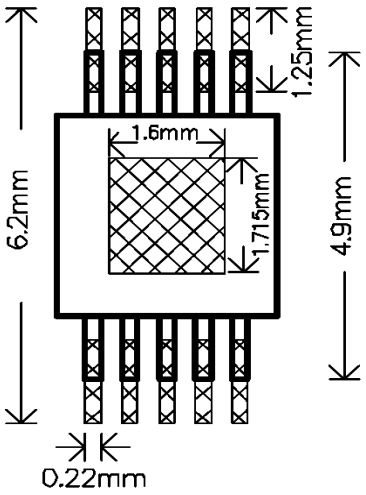


Recommended Minimum Footprint

MSOP-10



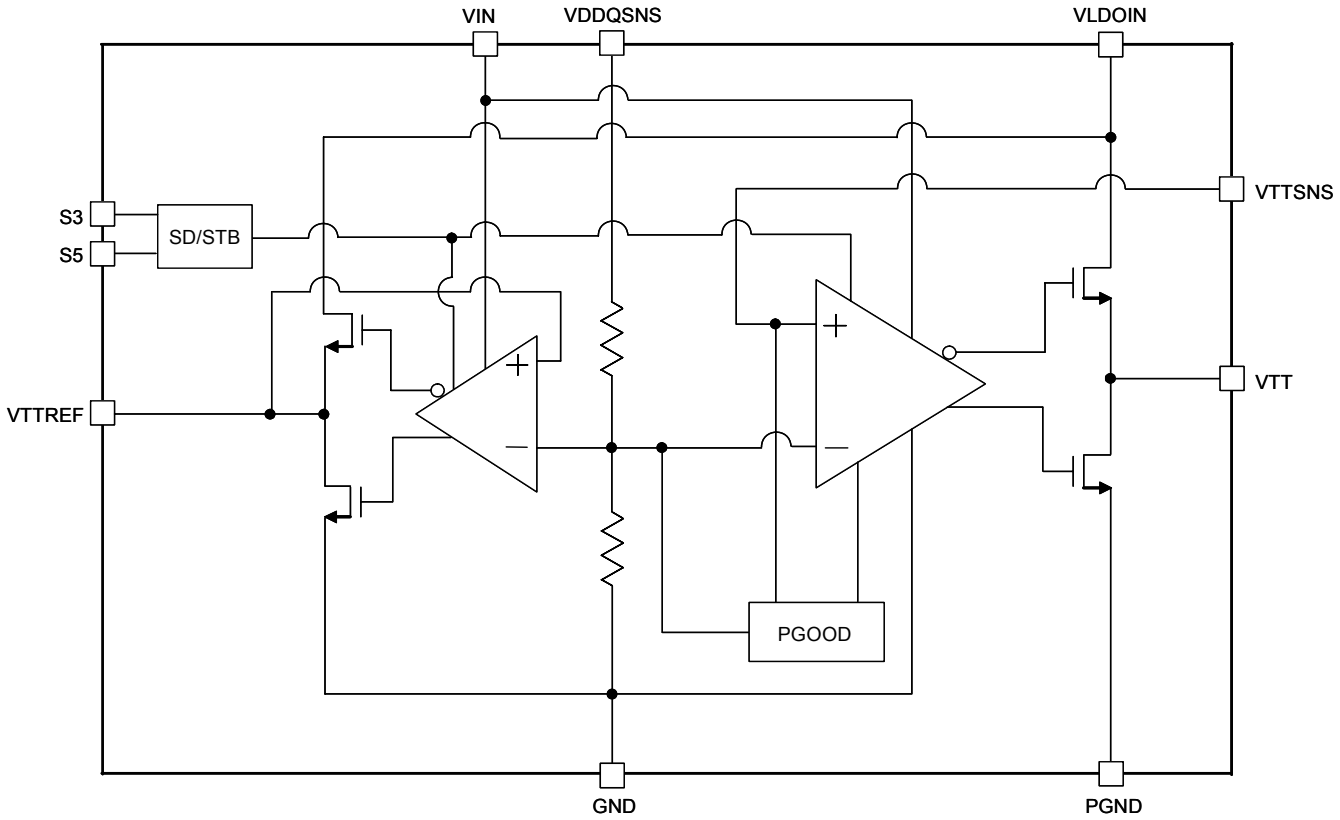
MSOP-10 (FD)



Pin Description

PIN	NAME	DESCRIPTIONS
1	VDDQSNS	VDDQ sense input
2	VLDOIN	Power supply for the VTT and VTTREF output stage
3	VTT	Output voltage for connection to termination resistors, equal to VDDQSNS/2
4	PGND	Power ground output for the VTT output
5	VTTSNS	Voltage sense input for the VTT LDO. Connect to plus terminal of the output capacitor
6	VTTREF	Buffered output that is a reference output ,equal to VDDQSNS/2
7	S3	Active low suspend to RAM mode control pin, VTT is turned off and left Hi-Z
8	GND	Ground
9	S5	Active low shutdown control pin, both VTT and VTTREF are turned off and discharged to ground
10	VIN	Analog input pin
Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram



Description

VTT SINK/SOURCE REGULATOR

The G2997 is a 3A sink/source tracking termination regulator designed specially for low-cost, low external components system where space is at premium such as notebook PC applications. The G2997 integrates high performance low-dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator is implemented with ultimately fast response feedback loop so that small ceramic capacitors are enough to keep tracking to the VTTREF within 40mV at all conditions including fast load transient. To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, VTTSNS, should be connected to the positive node of VTT output capacitor as a separate trace from the high current line from VTT.

VTTREF REGULATOR

The VTTREF block consists of an on-chip 1/2 divider, LPF and buffer. This regulator can source/sink current up to 10mA. Bypass VTTREF to GND using a 0.1µF ceramic capacitor to ensure stable operation. To ensure better start-up and transient performance, the larger 1µF ceramic capacitors are recommended.

Power on sequence

To operate safely, the G2997 must keep VIN voltage larger than other Input-PIN voltage .This condition is due to the internal parasitic diodes between VIN to others PIN for ESD issue. If the V_{IN} voltage is lower than the other pins voltage, the G2997 will consume extra current through the parasitic diodes during the power-on period.

Soft-Start

The soft-start function of the VTT is achieved via a current clamp, allowing the output capacitors to be charged with low and constant current that gives linear ramp up of the output voltage. The current limit threshold is changed in two stages using an internal powergood signal. When VTT is outside the powergood threshold, the current limit level is 2A. When VTT rises above (VTTREF - 5%) or falls below (VTTREF + 5%) the current limit level switches to 4 A. The thresholds are typically VTTREF 5% (from outside regulation to inside) and 10% (when it falls outside). The soft-start function is completely symmetrical and it works not only from GND to VTTREF voltage, but also from VDDQSNS to VTTREF voltage. Note that the VTT output is in a high impedance state during the S3 state (S3 = low, S5 = high) and its voltage can be up to VDDQSNS voltage depending on the external condition. Note that VTT does not start under a full load condition.

S3, S5 Control and Soft-Off

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals respectively. Both VTTREF and VTT are turned on at normal state (S3 = high, S5 = high). VTTREF is kept alive while VTT is turned off and left high impedance in standby state (S3 = low, S5 = high). Both VTT and VTTREF outputs are turned off and discharged to the ground through internal MOSFETs during shutdown state (S5 = low). The control function is showed on the Table 1.

Table 1. S3 and S5 Control Table

STATE	S3	S5	VTT	VREF
Normal	Hi	Hi	1.25V/0.9V	1.25V/0.9V
Standby	Lo	Hi	12mV/6mV (High-Z)	1.25V/0.9V
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)
Shutdown	Hi	Lo	0V (Discharge)	0V (Discharge)

VTT Current Protection

The LDO has a constant overcurrent limit (OCL) at 4A. This trip point is reduced to 2A before the outputvoltage comes within 5% of the target voltage or goes outside of 10% of the target voltage.

Input Capacitor

Adding a capacitance close to VLDOIN pin can improve the VTT performance when fast load- transient. In general, 1/2 COUT is recommended for the VLDOIN capacitance. Separating the VDDQSNS and VLDOIN pins will get better transient performance. The recommended capacitor types are tabulated in the Table 2.

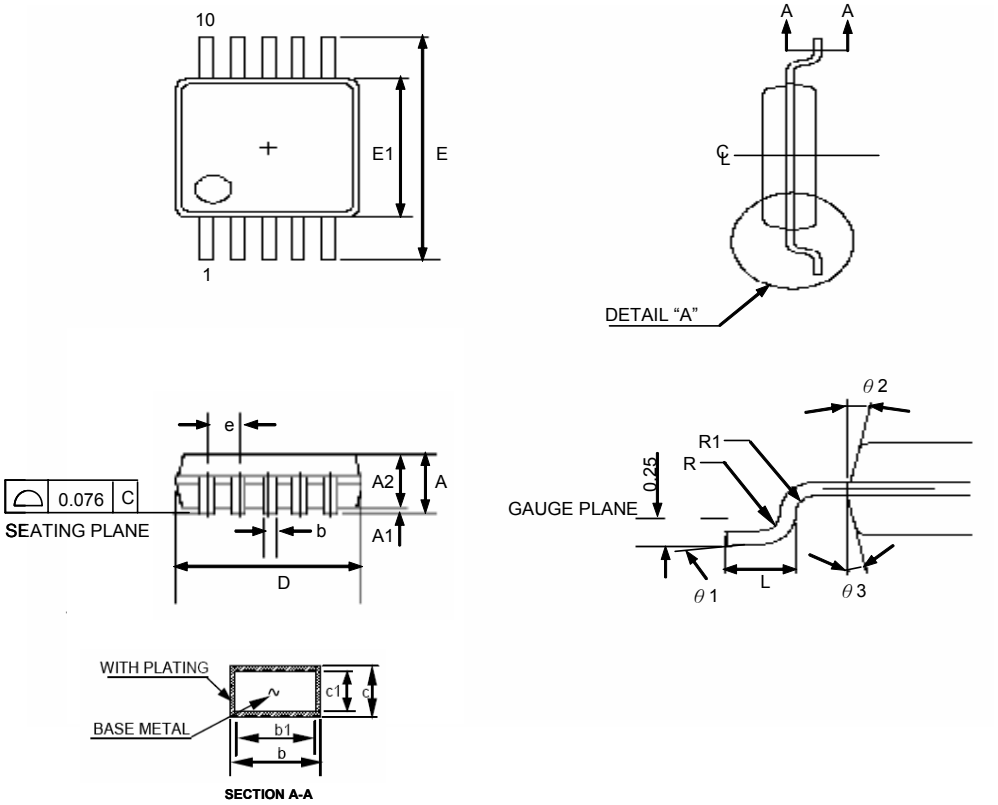
Output Capacitor

For stable operation, total capacitance of the VTT output terminal can be equal or greater than 20µF. The output capacitor should be located near VTT output terminal as close as possible to minimize the effect of ESR and ESL. The recommended capacitor types are tabulated in the Table 2.

Table 2.

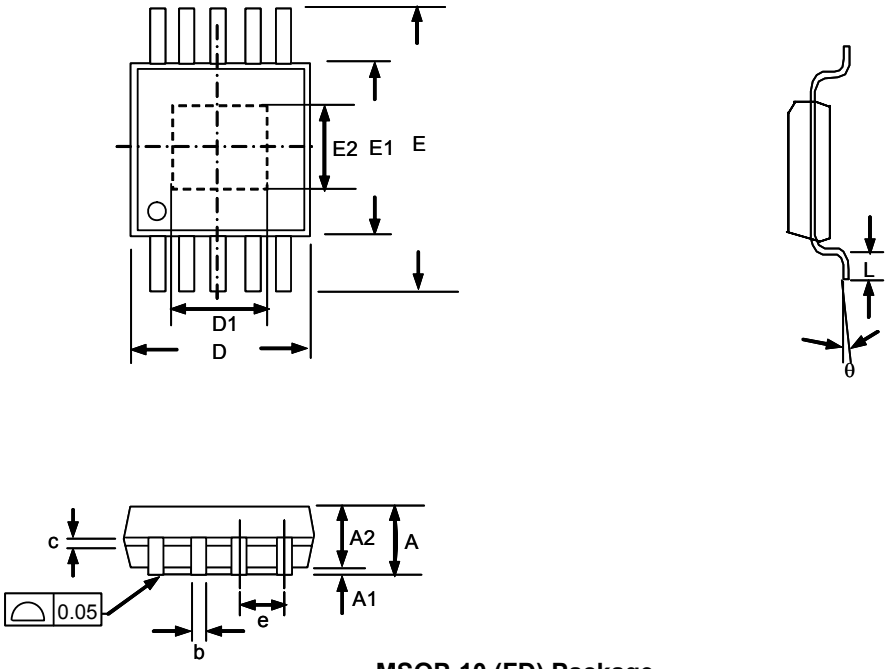
CAP	MANUF	PART NUMBER
C1	TAYO YUDEN	EMK 325BJ106KD
C2	TAYO YUDEN	UMK 212BJ104KG

Package Information



MSOP-10 Package

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.10	-----	-----	0.043
A1	0.05	-----	0.15	0.002	-----	0.006
A2	0.81	0.86	0.91	0.032	0.034	0.036
b	0.15	-----	0.30	0.006	-----	0.012
b1	0.15	0.20	0.25	0.006	0.008	0.010
c	0.13	-----	0.23	0.005		0.009
c1	0.13	0.15	0.18	0.005	0.006	0.007
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.50 BSC			0.020 BSC	
E		4.90 BSC			0.193 BSC	
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
θ1	0°	-----	6°	0°	-----	6°
θ2		12 REF			12 REF	
θ3		12 REF			12 REF	
R	0.09	-----	-----	0.004	-----	-----
R1	0.09	-----	-----	0.004	-----	-----
JEDEC	MO-187BA					



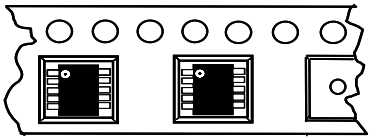
MSOP-10 (FD) Package

Note:1. JEDEC Outline: MO-187 BA/MO-187 BA-T (Thermally Enhanced Variations Only)

2. Dimension "D" does not include mold flash. Protrusions or gate burrs. Mold flash. Protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
4. Dimension "0.22" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the "0.22" dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum spac between protrusion and adjacent lead is 0.07mm.
5. Dimensions "D" and "E1" to be determined at datum plane.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.10	-----	-----	0.043
A1	0.00	-----	0.15	0.000	-----	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.17	-----	0.27	0.007	-----	0.011
c	0.08	-----	0.23	0.003	-----	0.009
D	3.00 BSC			0.118 BSC		
D1	1.60 REF			0.063 REF		
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.715 REF			0.068 REF		
e	0.50 BSC			0.002 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
θ	0°	-----	8°	0°	-----	8°

Taping Specification



Feed Direction
Typical MSOP Package Orientation

PACKAGE	Q'TY/BY REEL
MSOP-10	2,500 ea
MSOP-10 (FD)	2,500 ea