HAF2012(L), HAF2012(S)

Silicon N Channel MOS FET Series
Power Switching

REJ03G1139-0400
Rev.4.00
Jul 13, 2007

Description

This FET has the over temperature shut-down capability sensing to the junction temperature.

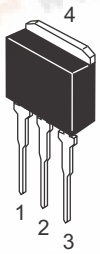
This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

Features

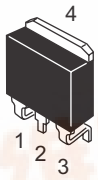
- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut-down operation (Need 0 voltage recovery)

Outline

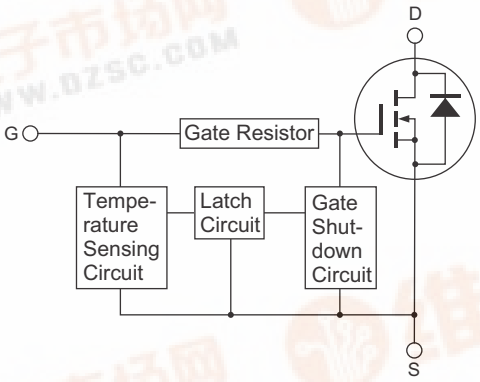
RENESAS Package code: PRSS0004AE-A
(Package name: LDPAK (L))



RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK (S)-(1))



1. Gate
2. Drain
3. Source
4. Drain



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	16	V
	V_{GSS}	–2.8	V
Drain current	I_D	20	A
Drain peak current	$I_{D\ (pulse)}$ Note 1	40	A
Body-drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch Note 2	50	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Ta = 25°C

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	100	µA	Vi = 8 V, V_{DS} = 0
	I_{IH2}	—	—	50	µA	Vi = 3.5 V, V_{DS} = 0
	I_{IL}	—	—	1	µA	Vi = 1.2 V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH\ (sd)\ 1}$	—	0.8	—	mA	Vi = 8 V, V_{DS} = 0
	$I_{IH\ (sd)\ 2}$	—	0.35	—	mA	Vi = 3.5 V, V_{DS} = 0
Shut down temperature	Tsd	—	175	—	°C	Channel temperature
Gate operation voltage	V_{OP}	3.5	—	13	V	

Electrical Characteristics

(Ta = 25°C)

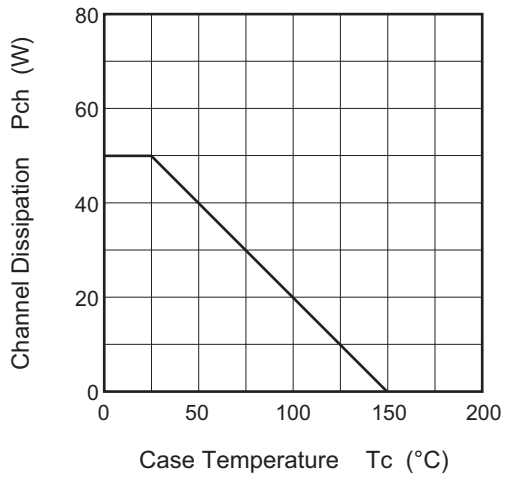
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	10	—	—	A	V_{GS} = 3.5 V, V_{DS} = 2 V
	I_{D2}	—	—	10	mA	V_{GS} = 1.2 V, V_{DS} = 2 V
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)\ GSS}$	16	—	—	V	I_G = 100 µA, V_{DS} = 0
	$V_{(BR)\ GSS}$	–2.8	—	—	V	I_G = –100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS1}	—	—	100	µA	V_{GS} = 8 V, V_{DS} = 0
	I_{GSS2}	—	—	50	µA	V_{GS} = 3.5 V, V_{DS} = 0
	I_{GSS3}	—	—	1	µA	V_{GS} = 1.2 V, V_{DS} = 0
	I_{GSS4}	—	—	–100	µA	V_{GS} = –2.4 V, V_{DS} = 0
Input current (shut down)	$I_{GS\ (op)\ 1}$	—	0.8	—	mA	V_{GS} = 8 V, V_{DS} = 0
	$I_{GS\ (op)\ 2}$	—	0.35	—	mA	V_{GS} = 3.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS\ (off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS\ (on)}$	—	50	65	mΩ	I_D = 10 A, V_{GS} = 4 V Note 3
	$R_{DS\ (on)}$	—	30	43	mΩ	I_D = 10 A, V_{GS} = 10 V Note 3
Forward transfer admittance	$\|y_{fs}\|$	6	12	—	S	I_D = 10 A, V_{DS} = 10 V Note 3
Output capacitance	Coss	—	630	—	pF	V_{DS} = 10 V, V_{GS} = 0 f = 1 MHz
Turn-on delay time	$t_{d\ (on)}$	—	7.5	—	µs	I_D = 5 A V_{GS} = 5 V R_L = 6 Ω
Rise time	t_r	—	29	—	µs	
Turn-off delay time	$t_{d\ (off)}$	—	34	—	µs	
Fall time	t_f	—	26	—	µs	
Body-drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 20 A, V_{GS} = 0
Body-drain diode reverse recovery time	t_{rr}	—	110	—	ns	I_F = 20 A, V_{GS} = 0 di_F/dt = 50 A/µs
Over load shut down operation time Note4	t_{os1}	—	1.8	—	ms	V_{GS} = 5 V, V_{DD} = 12 V
	t_{os2}	—	0.7	—	ms	V_{GS} = 5 V, V_{DD} = 24 V

Notes: 3. Pulse test

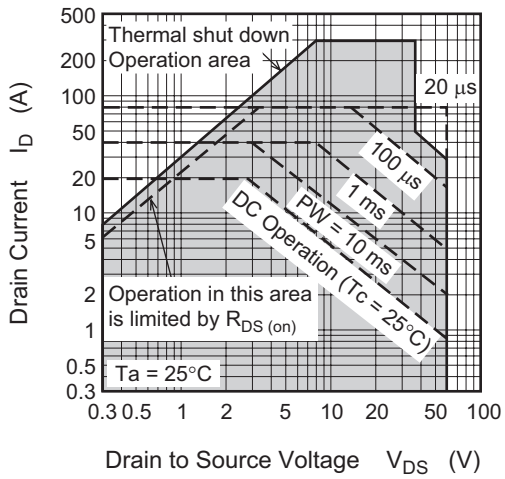
4. Including the junction temperature rise of the over loaded condition.

Main Characteristics

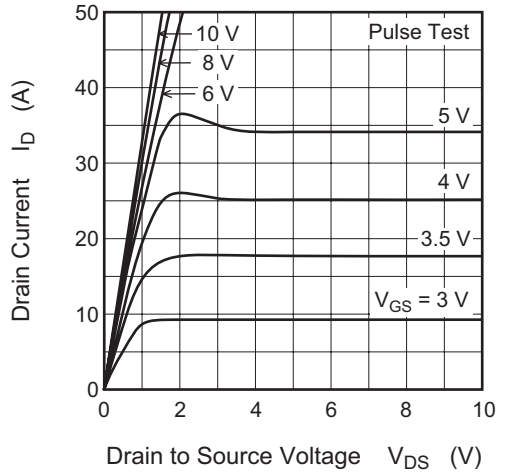
Power vs. Temperature Derating



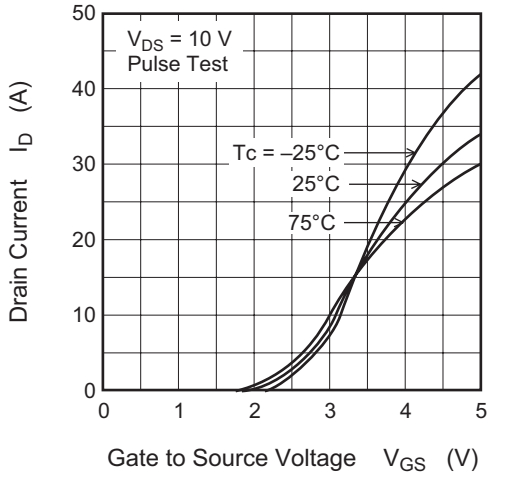
Maximum Safe Operation Area



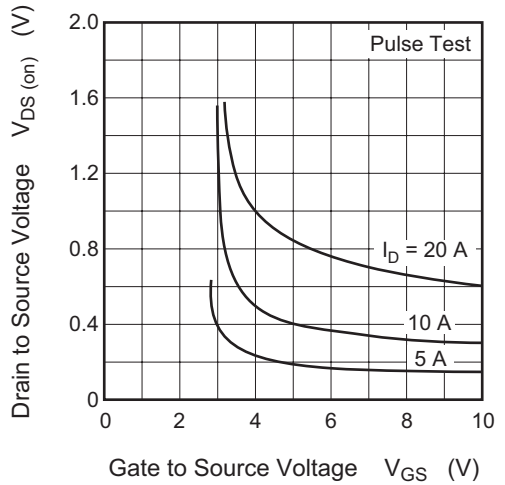
Typical Output Characteristics



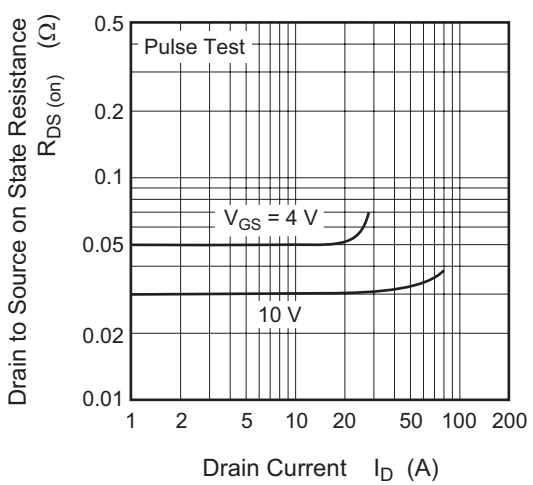
Typical Transfer Characteristics



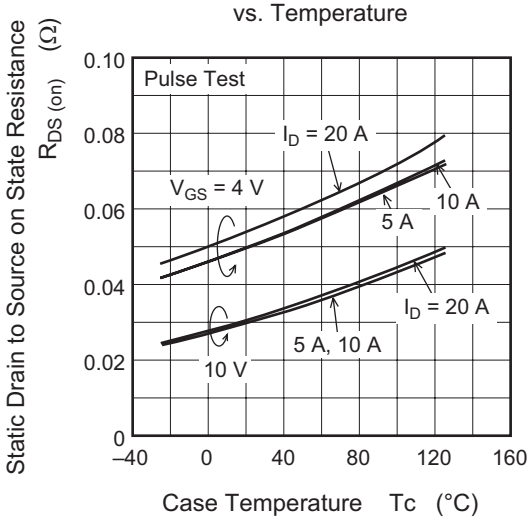
Drain to Source Saturation Voltage vs. Gate to Source Voltage



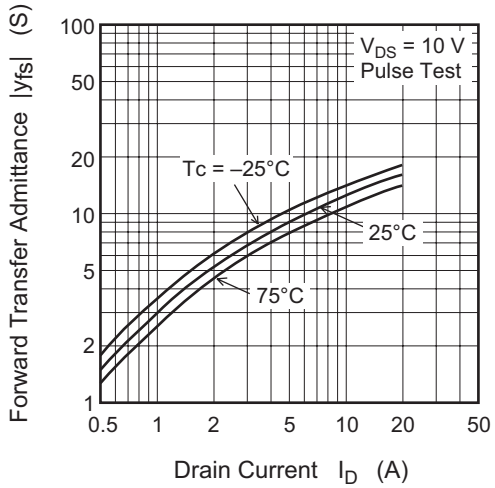
Static Drain to Source on State Resistance vs. Drain Current



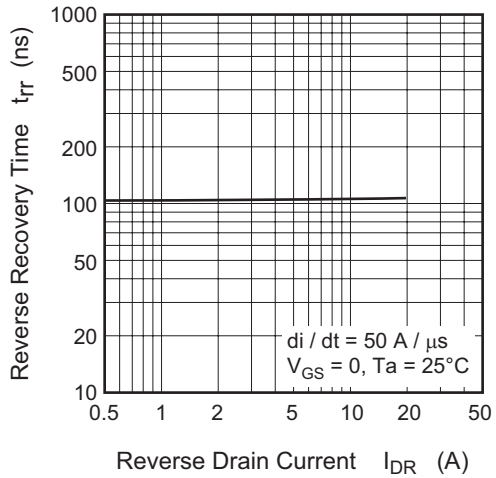
Static Drain to Source on State Resistance vs. Temperature



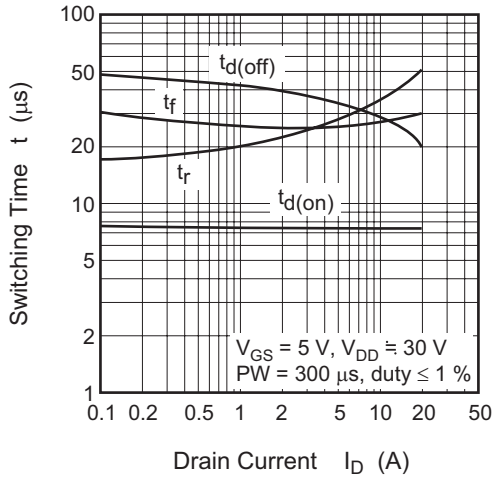
Forward Transfer Admittance vs. Drain Current



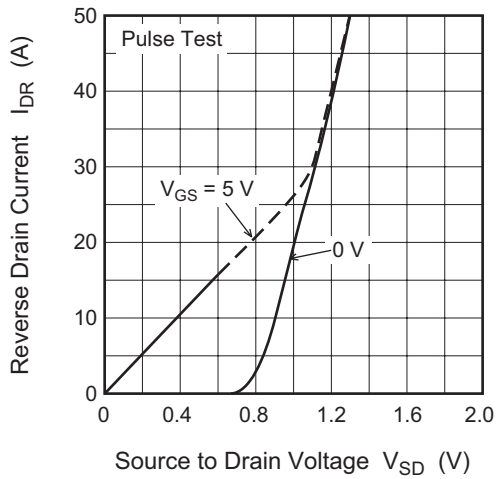
Body-Drain Diode Reverse Recovery Time



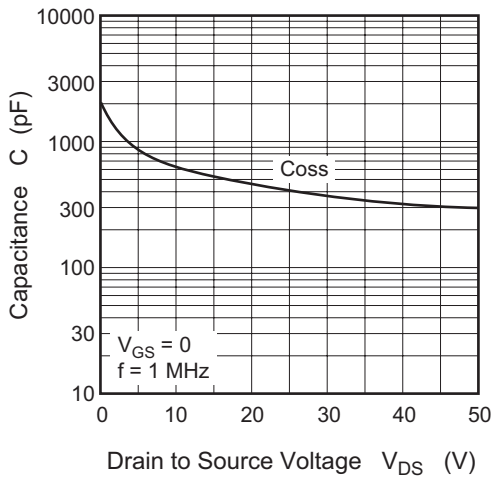
Switching Characteristics



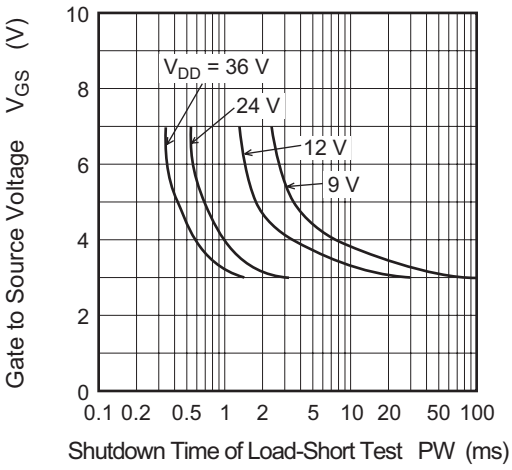
Reverse Drain Current vs. Source to Drain Voltage



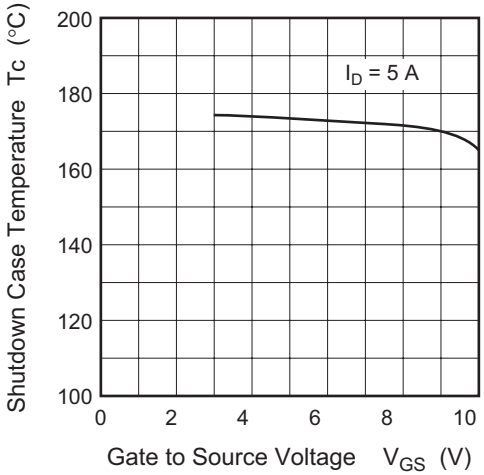
Typical Capacitance vs. Drain to Source Voltage



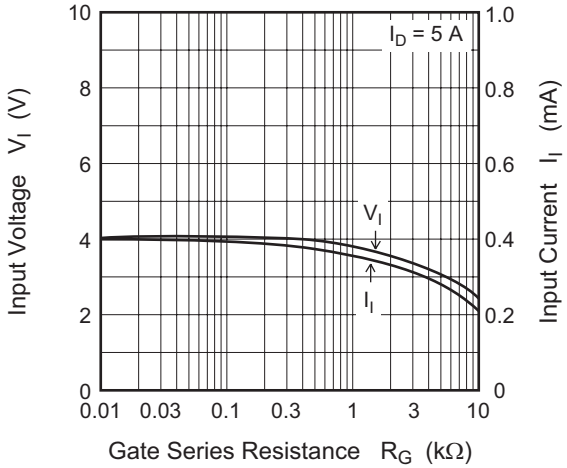
Gate to Source Voltage vs.
Shutdown Time of Load-Short Test



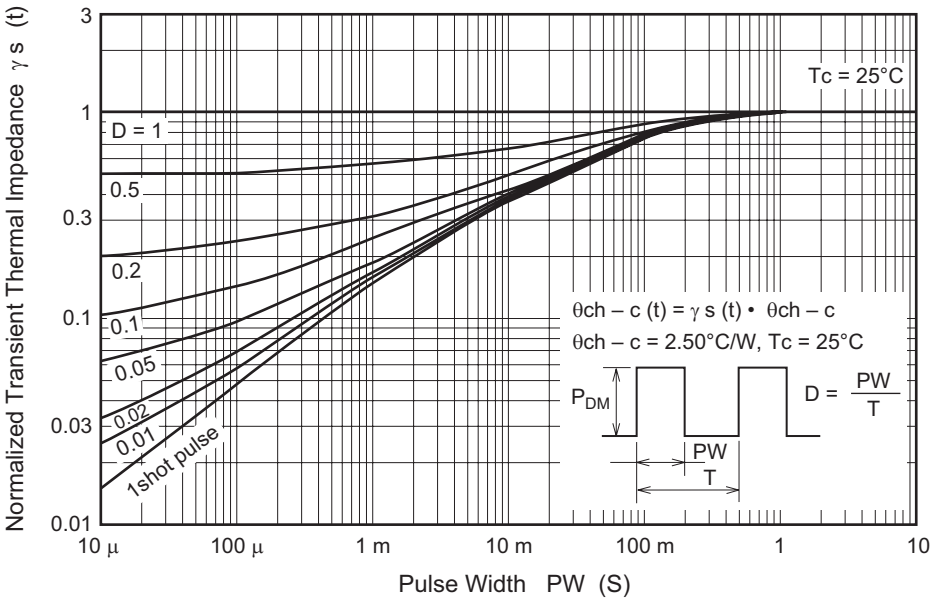
Shutdown Case Temperature vs.
Gate to Source Voltage



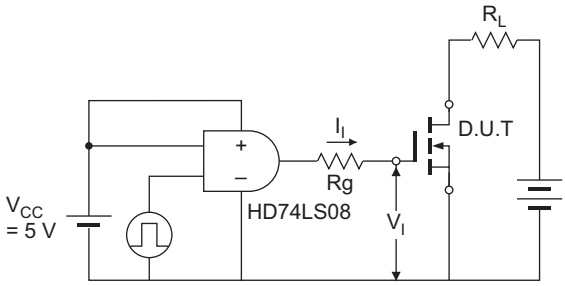
TTL Drive Characteristics

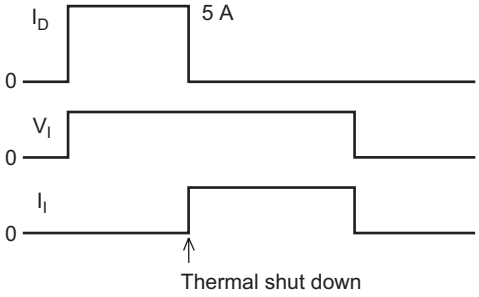


Normalized Transient Thermal Impedance vs. Pulse Width

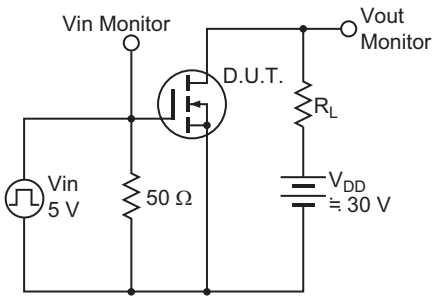


Test Circuit

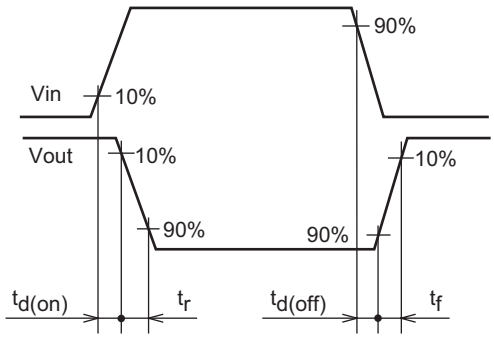




Switching Time Test Circuit



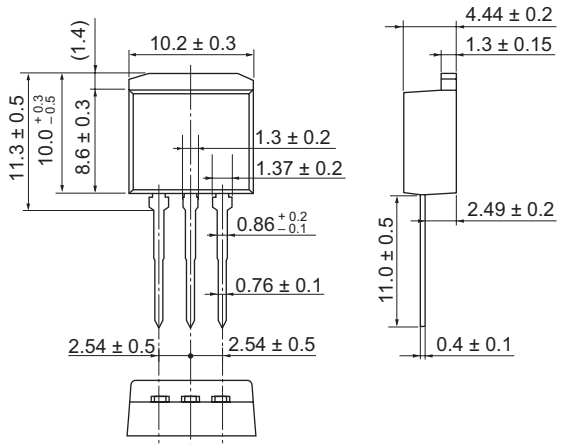
Waveform



Package Dimensions

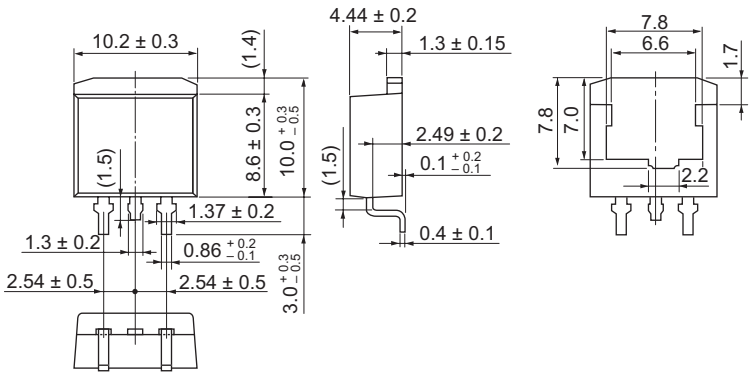
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(L)	—	PRSS0004AE-A	LDPAK(L) / LDPAK(L)V	1.40g

Unit: mm



Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(S)-(1)	SC-83	PRSS0004AE-B	LDPAK(S)-(1) / LDPAK(S)-(1)V	1.30g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
HAF2012-90L	Max: 50 pcs/sack	Sack
HAF2012-90S	Max: 50 pcs/sack	Sack
HAF2012-90STL	1000 pcs/Reel	Embossed tape
HAF2012-90STR	1000 pcs/Reel	Embossed tape

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RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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