



HAT1055R, HAT1055RJ

Silicon P Channel Power MOS FET
High Speed Power Switching

REJ03G0067-0100Z

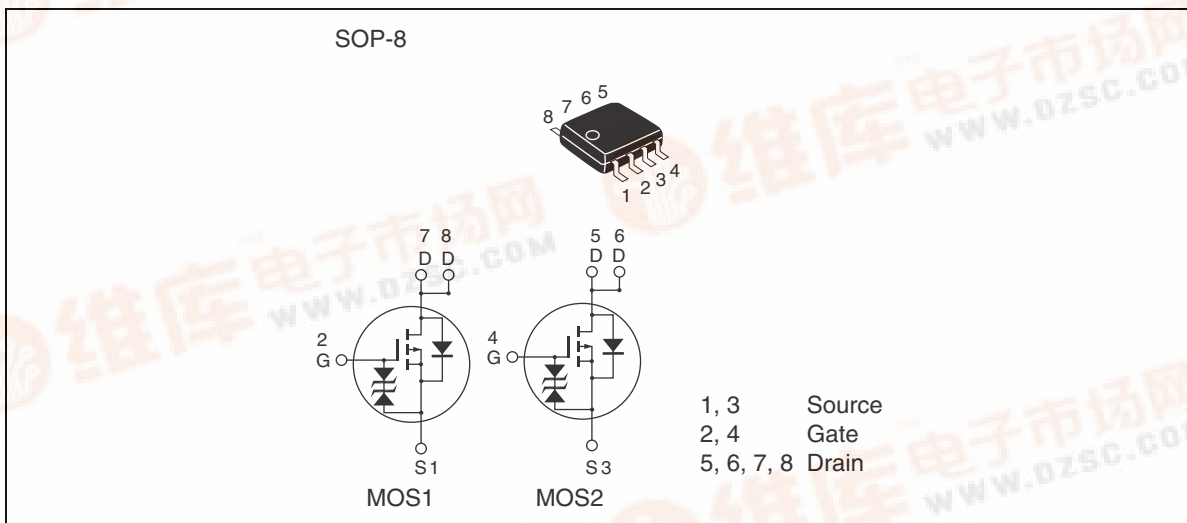
Rev.1.00

Aug.29.2003

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- “J” is for Automotive application
High temperature D-S leakage guarantee
Avalanche rating

Outline



HAT1055R, HAT1055RJ

Absolute Maximum Ratings

(T_a = 25°C)

Item	Symbol	Ratings		Unit
		HAT1055R	HAT1055RJ	
Drain to source voltage	V _{DSS}	-60	-60	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	-5	-5	A
Drain peak current	I _D (pulse) ^{Note1}	-40	-40	A
Avalanche current	I _{AP} ^{Note4}	—	-5	A
Avalanche energy	E _{AR} ^{Note4}	—	2.14	mJ
Channel dissipation	P _{ch} ^{Note2}	2	2	W
Channel dissipation	P _{ch} ^{Note3}	3	3	W
Channel temperature	T _{ch}	150	150	°C
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1%

2. 1 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

3. 2 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

4. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

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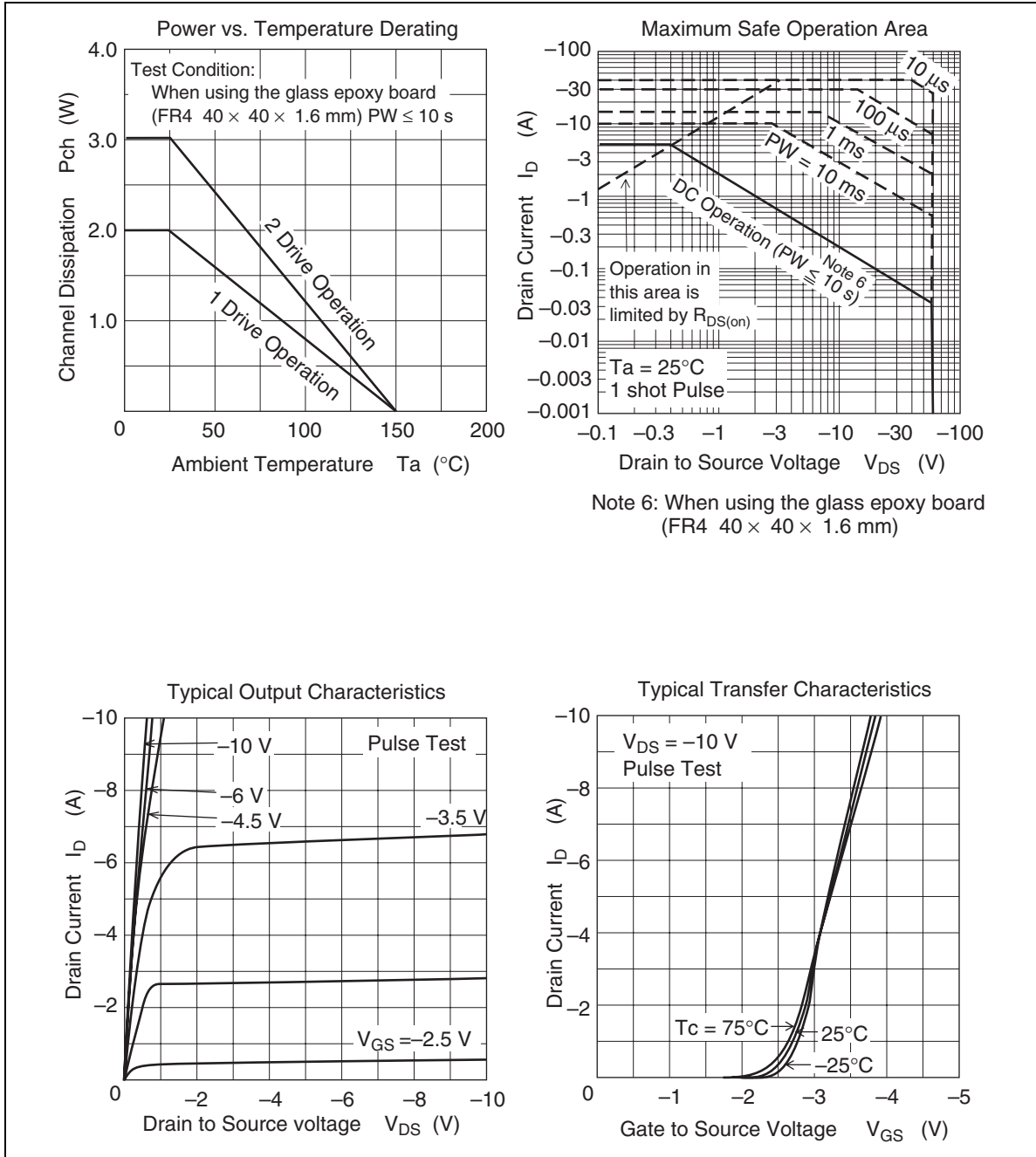
Electrical Characteristics

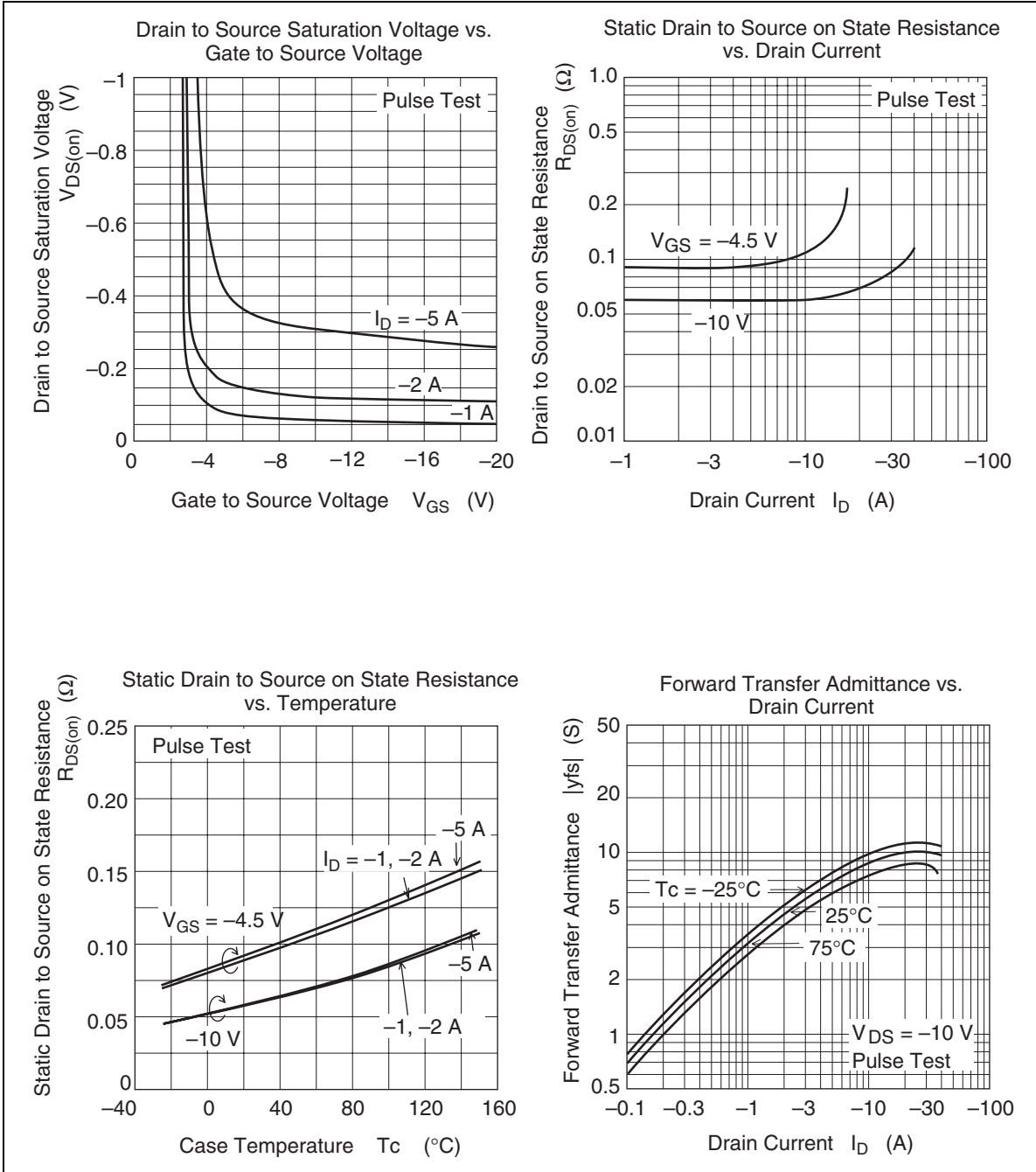
(Ta = 25°C)

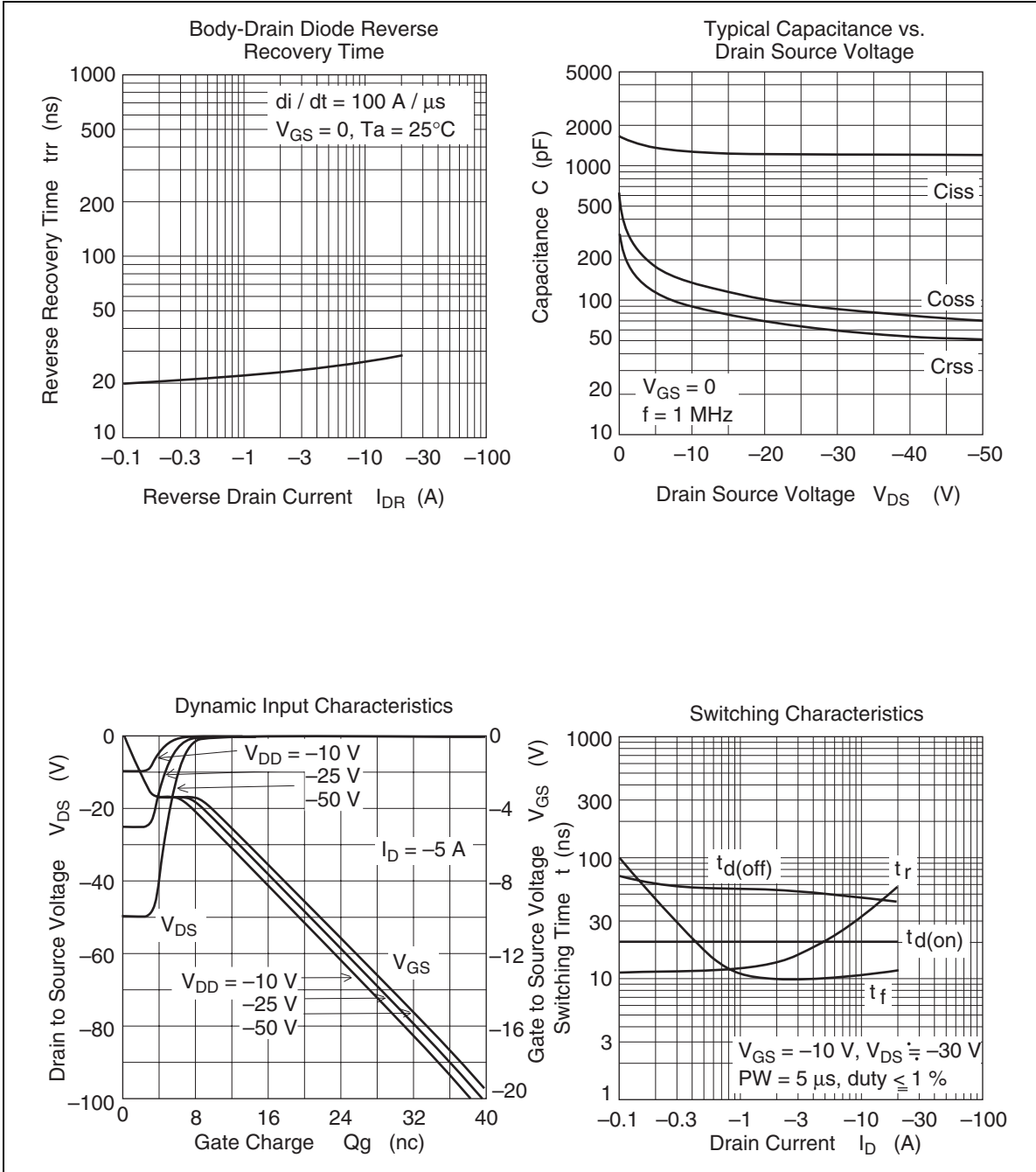
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to Source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Zero gate voltage drain current	HAT1055R	I_{DSS}	—	—	μA	$V_{DS} = -48 \text{ V}$, $V_{GS} = 0$
	HAT1055RJ	I_{DSS}	—	—	-10	μA
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	3	5	—	S	$I_D = -2.5 \text{ A}^{\text{Note5}}$, $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	60	76	m Ω	$I_D = -2.5 \text{ A}^{\text{Note5}}$, $V_{GS} = -10 \text{ V}$
	$R_{DS(on)}$	—	90	130	m Ω	$I_D = -2.5 \text{ A}^{\text{Note5}}$, $V_{GS} = -4.5 \text{ V}$
Input capacitance	C_{iss}	—	1350	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$
Output capacitance	C_{oss}	—	135	—	pF	f = 1 MHz
Reverse transfer capacitance	C_{rss}	—	85	—	pF	
Total gate charge	Q_g	—	21	—	nC	$V_{DD} = -25 \text{ V}$
Gate to source charge	Q_{gs}	—	3	—	nC	$V_{GS} = -10 \text{ V}$
Gate to drain charge	Q_{gd}	—	4	—	nC	$I_D = -5 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -2.5 \text{ A}$
Rise time	t_r	—	15	—	ns	$V_{DD} \cong -30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	$R_L = 12 \text{ }\Omega$
Fall time	t_f	—	10	—	ns	$R_G = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	-0.85	-1.10	V	$I_F = -5 \text{ A}$, $V_{GS} = 0^{\text{Note5}}$
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	$I_F = -5 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

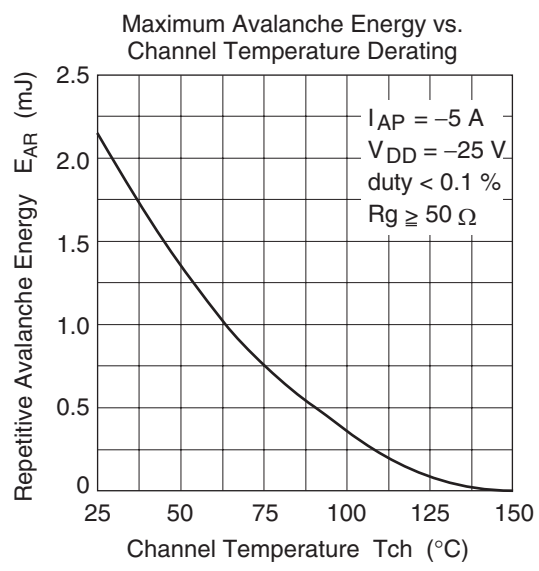
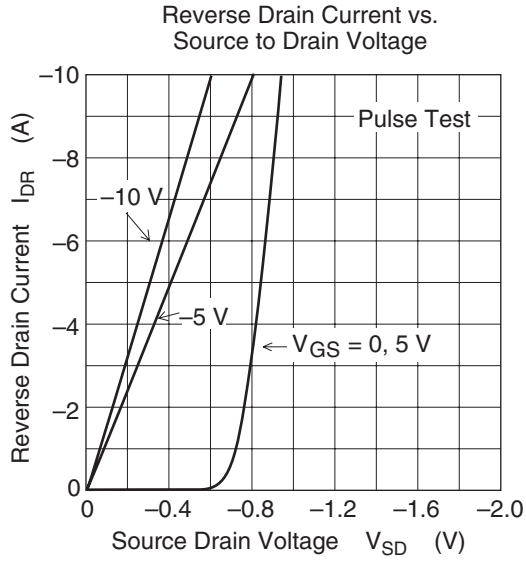
Notes: 5. Pulse test

Main Characteristics

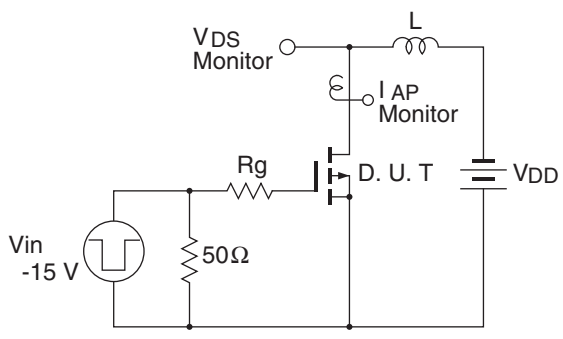






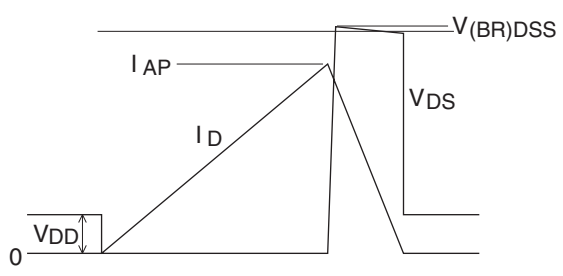


Avalanche Test Circuit

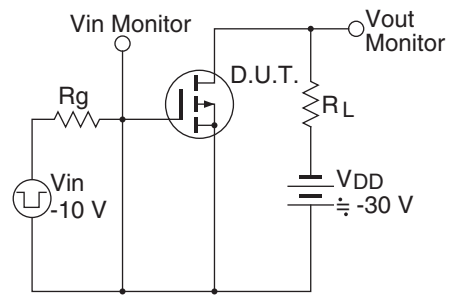


Avalanche Waveform

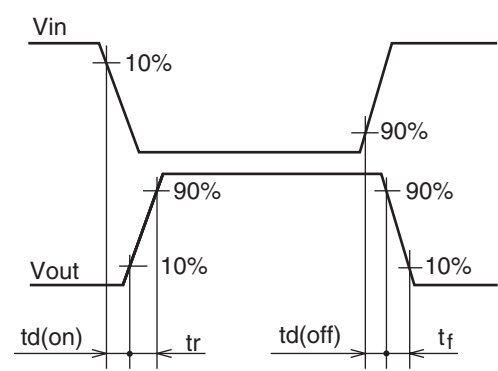
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

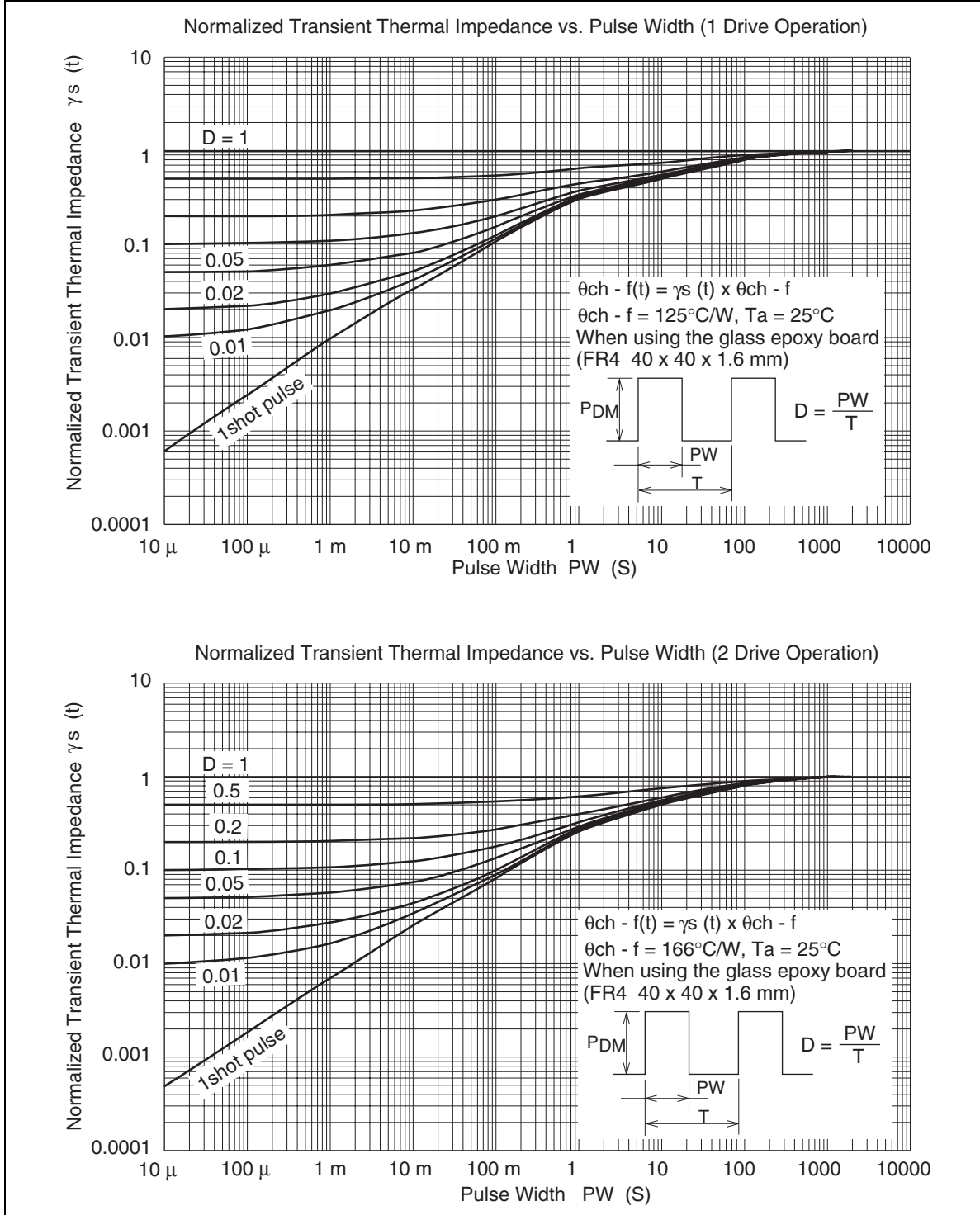


Switching Time Test Circuit



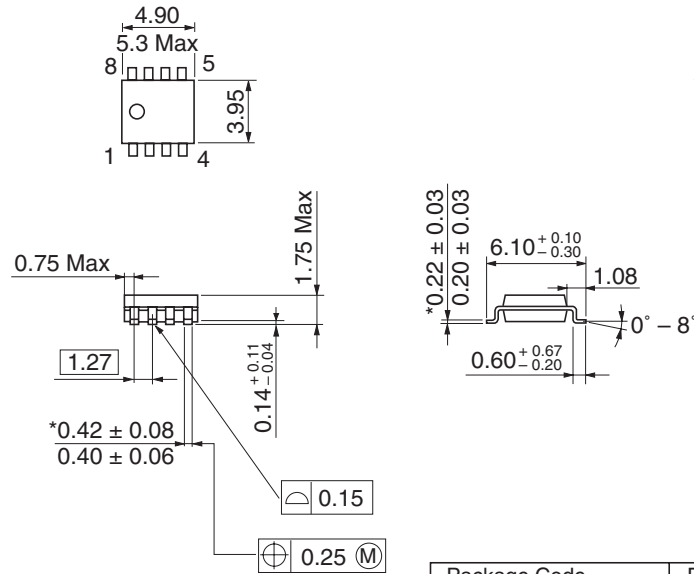
Switching Time Waveform





Package Dimensions

As of January, 2003
Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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