



HAT2139H

Silicon N Channel Power MOS FET Power Switching

REJ03G0055-0500

Rev.5.00

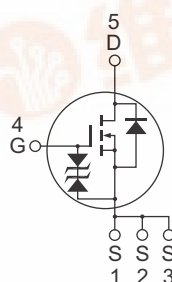
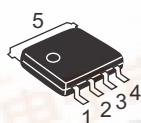
Sep 20, 2005

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 9 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTZZ0005DA-A)
(Package name: LFPAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	80	A
Body-drain diode reverse drain current	I_{DR}	20	A
Avalanche current	I_{AP} ^{Note 3}	10	A
Avalanche energy	E_{AR} ^{Note 3}	8	mJ
Channel dissipation	P_{ch} ^{Note 2}	15	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. $T_c = 25^\circ C$ 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$ 

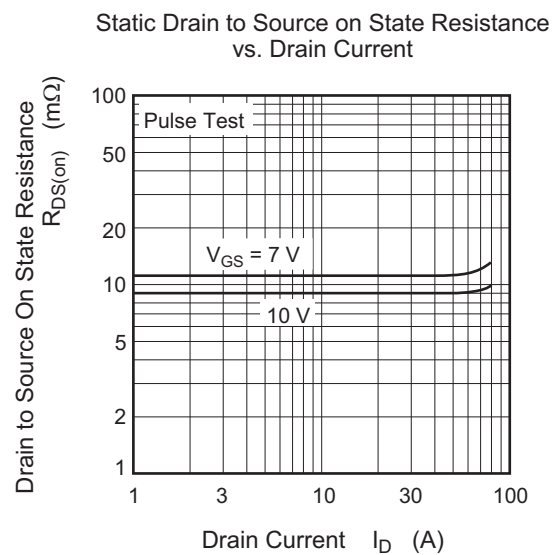
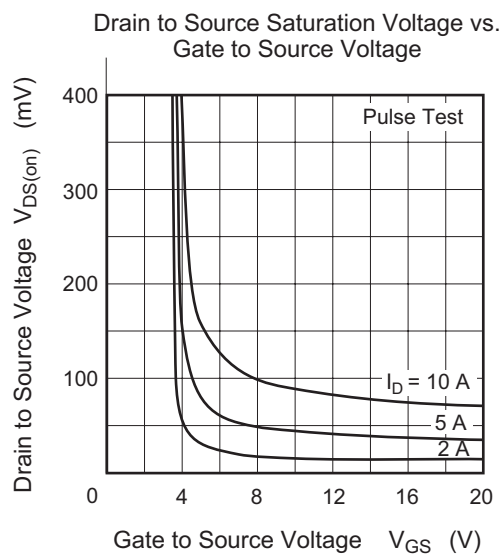
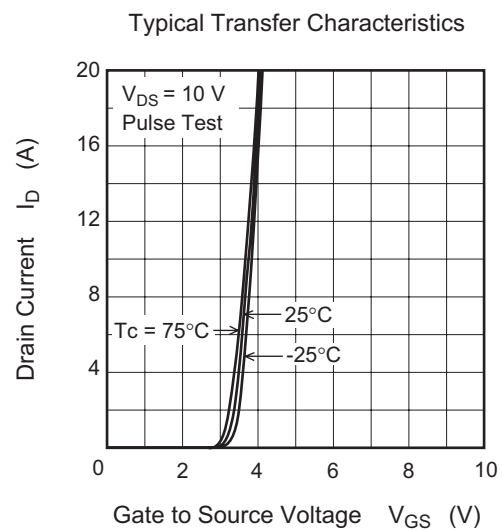
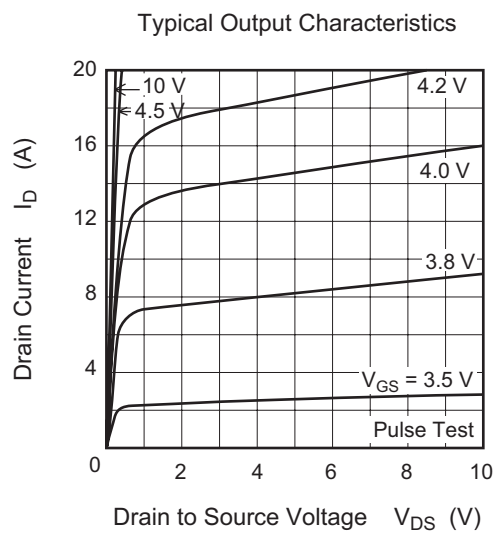
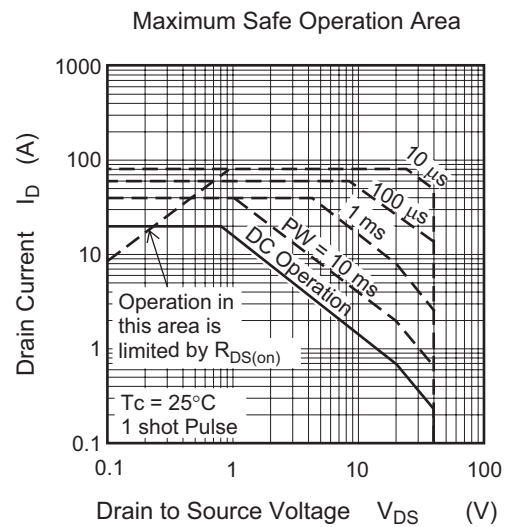
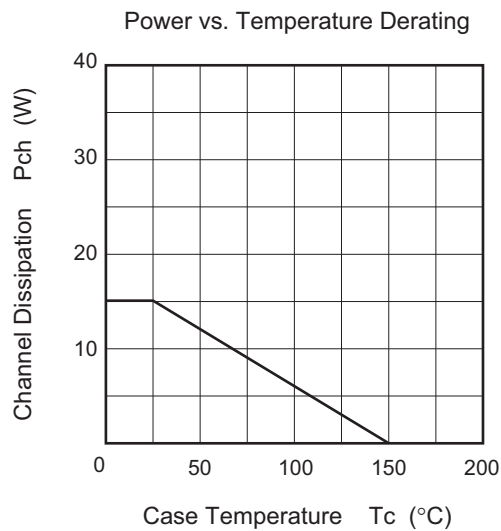
Electrical Characteristics

(Ta = 25°C)

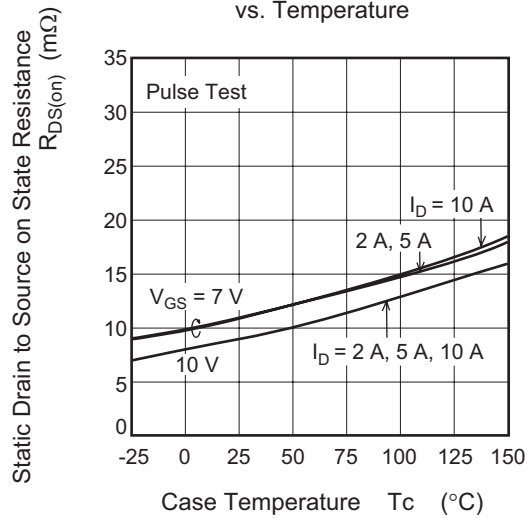
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	9.0	11.5	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	11.0	15.0	$\text{m}\Omega$	$I_D = 10 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	15	25	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	2000	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	290	—	pF	
Reverse transfer capacitance	C_{rss}	—	175	—	pF	
Total gate charge	Q_g	—	30	—	nC	$V_{DD} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$
Gate to source charge	Q_{gs}	—	8	—	nC	
Gate to drain charge	Q_{gd}	—	5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$, $V_{DD} \cong 10 \text{ V}$, $R_L = 1.0 \text{ }\Omega$, $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	23	—	ns	
Turn-off delay time	$t_{d(off)}$	—	58	—	ns	
Fall time	t_f	—	10	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

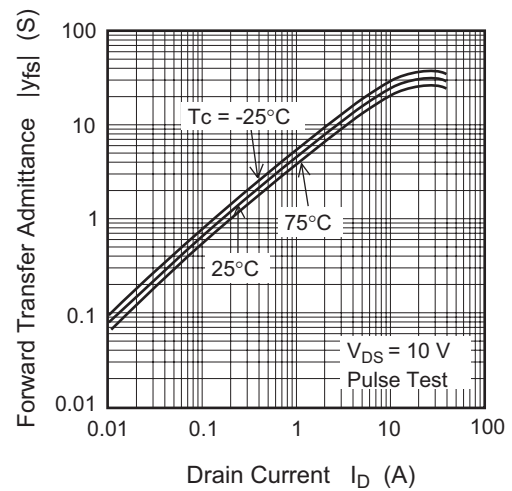
Main Characteristics



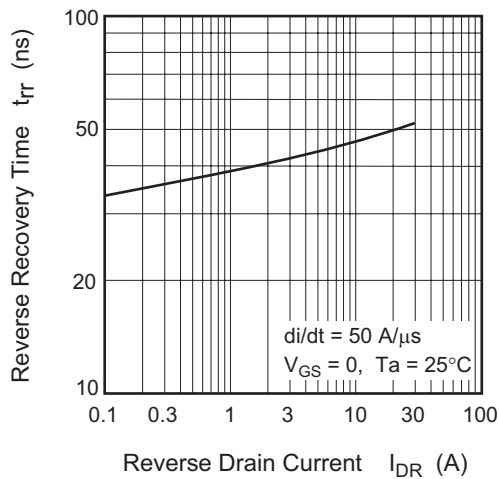
Static Drain to Source on State Resistance vs. Temperature



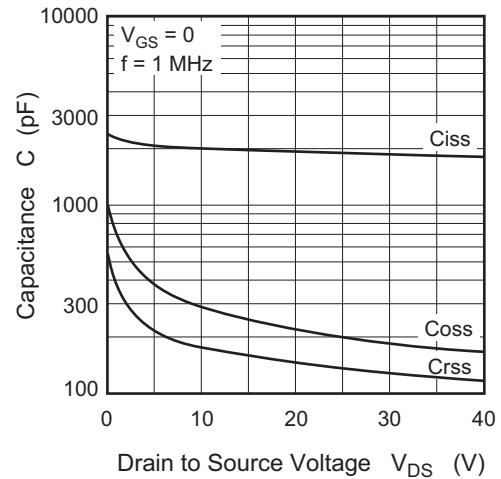
Forward Transfer Admittance vs. Drain Current



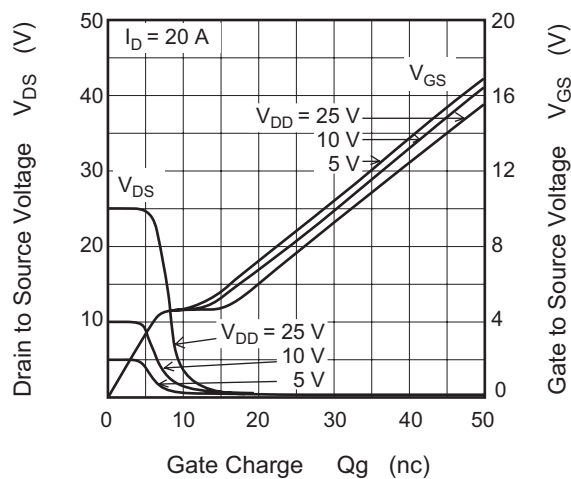
Body-Drain Diode Reverse Recovery Time



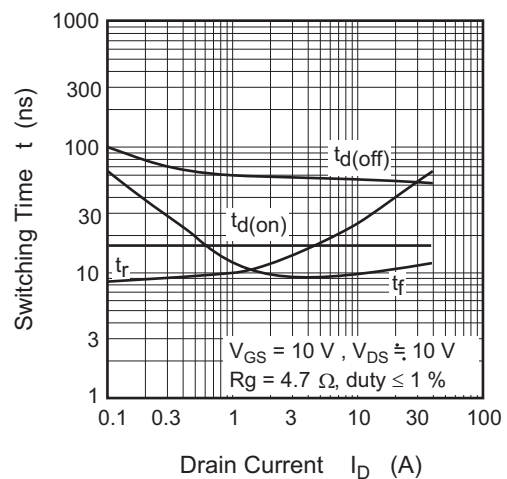
Typical Capacitance vs. Drain to Source Voltage

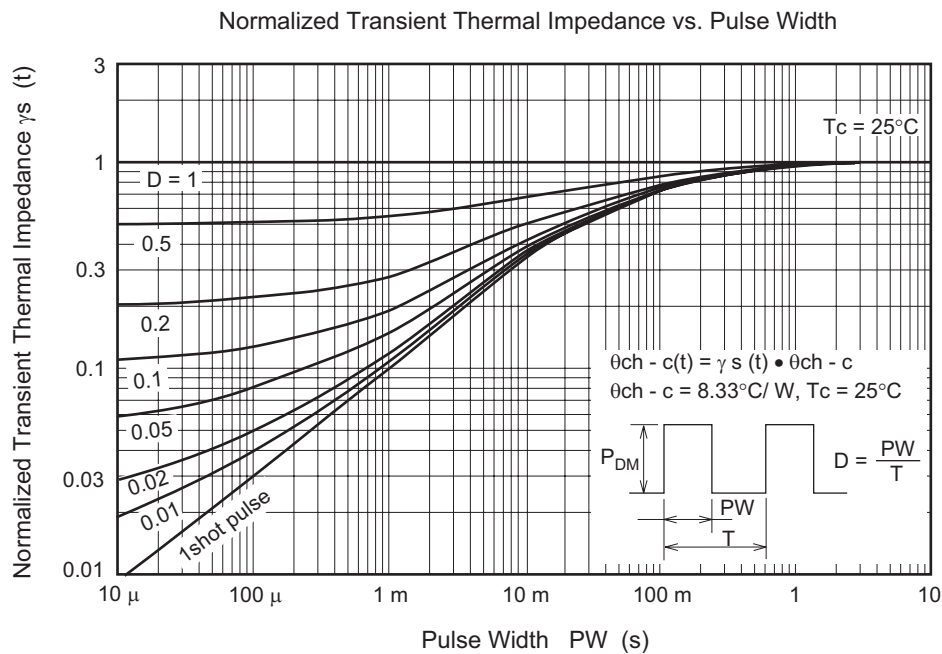
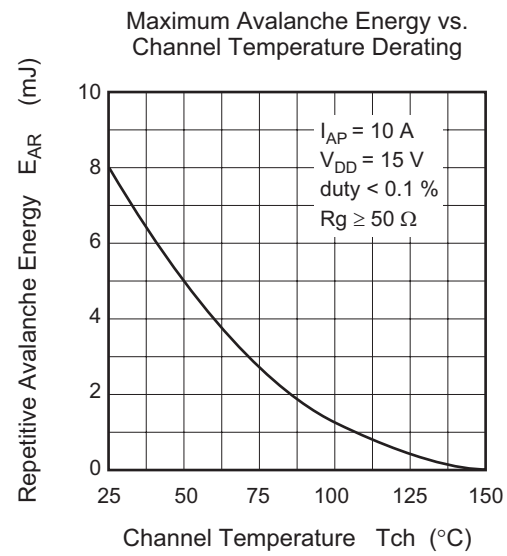
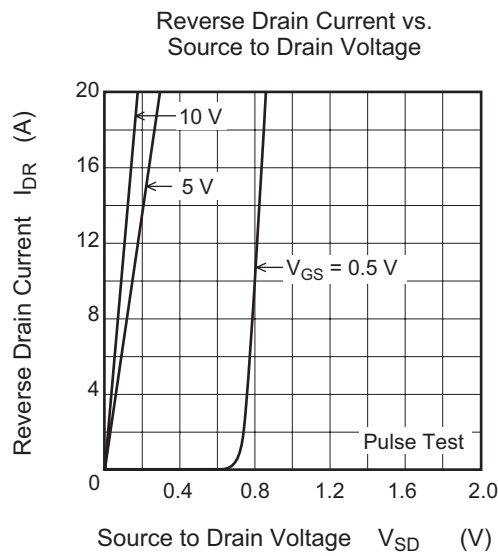


Dynamic Input Characteristics

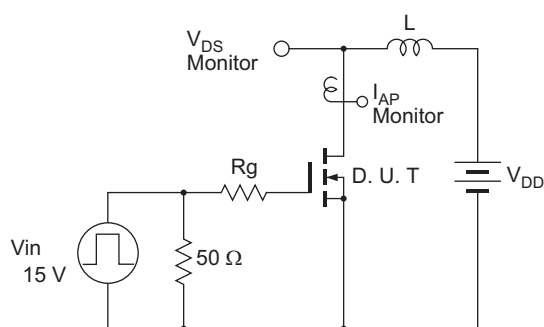


Switching Characteristics



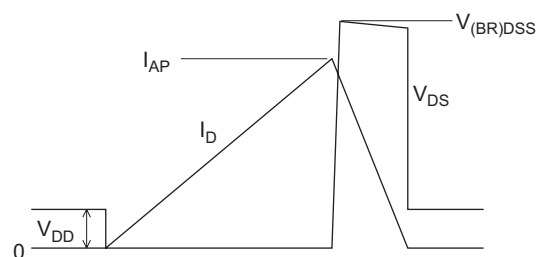


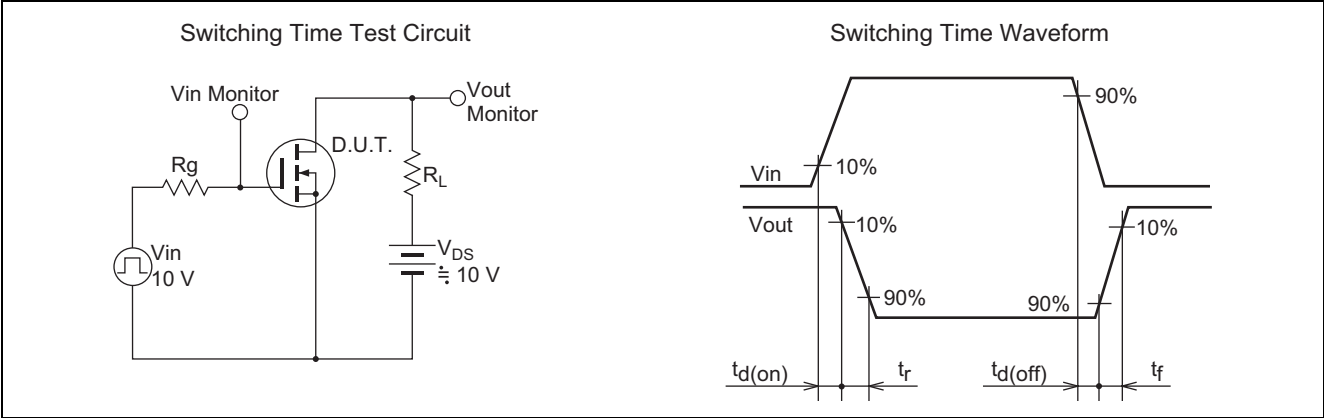
Avalanche Test Circuit



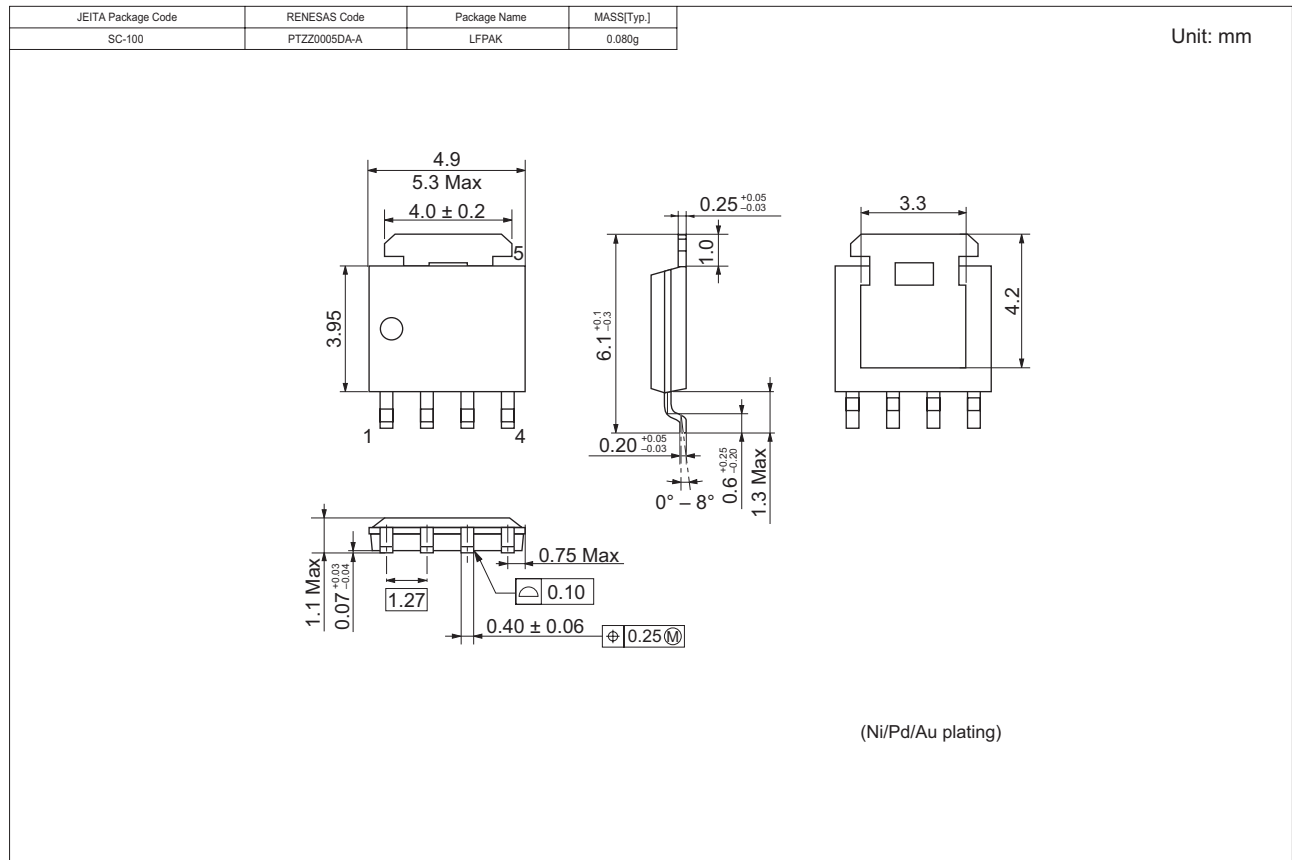
Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT2139H-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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