
HD66766R

Rev. 1.0-1 / September 2002

HD66766R

(132 x 176-dot Graphics LCD Controller/Driver for 65K Colors)

HITACHI

Rev.1.0-1
September, 2002

Description

The HD66766R, color-graphics LCD controller and driver LSI, displays 132-by-176-dot graphics for 65K STN colors. A 16-bit high-speed bus interface and high-speed RAM write function enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66766R has various functions for reducing the power consumption of a LCD system, such as low-voltage operation of 2.2 V/min., a step-up circuit to generate a maximum of 12-times the LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66766R is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bi-directional pagers, and small PDAs.

Features

- 132RGB x 176-dot graphics display LCD controller/driver for 65K STN colors
- low voltage drive and flickerless PWM grayscale drive
- 16-/8-bit high-speed bus interface and Clock Synchronized Serial Interface (SPI)
- High-speed burst-RAM write function
- Writing to a window-RAM address area by using a window-address function
- Bit-operation functions for graphics processing:
 - Write-data mask function in bit units.
 - Logical operation in pixel unit and conditional write function.



- Various color-display control functions
 - 65K out of 140K possible colors can be displayed at the same time (grayscale palette incorporated)
 - Vertical scroll display function in raster-row units
 - Partial LCD drive of two screens in any position
- Low-power operation supports:
 - Vcc = 2.2 to 3.6 V (low-voltage)
 - Common driving voltage = 8 to 44 V
 - Segment driving voltage = 2 to 4 V
 - VOUT power voltage = 4.0V to 5.75 V
 - Power-save functions such as the standby mode and sleep mode
 - Internal power supply circuit
 - Programmable drive duty ratios (1/8–1/176) and bias values (1/2–1/13) displayed on LCD
 - Maximum 12-times step-up circuit for liquid crystal drives voltage and voltage inverting circuit
 - 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
- Internal RAM capacity: 46,464 bytes
- 396-segment × 176-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Internal oscillation and hardware reset
- Shift change of segment and common drivers
- COM positioned on both sides in one chip for COG

Type Name

Types	External Dimensions
HCD667A66RBP	Au-bumped chip straight bump
HCD667B66RBP	Au-bumped chip laced bump

Difference between HCD667x66R and HCD667x66

Table 1

Difference	HCD667x66R		HCD667x66	
	Pad No.	Pad Name	Pad No.	Pad Name
Pad arrangement	63	Vcc	63	Vcc
	63	Vcc	63	Vcc
	64	Vcc	64	Vcc
	66	Vcc	66	Vcc
	67	AVcc	67	Vcc
	68	AVcc	68	Vcc
	69	AVcc	69	Vcc
	70	AVcc	70	Vcc

■ HD66766R PAD Arrangement (Straight Output Arrangement)

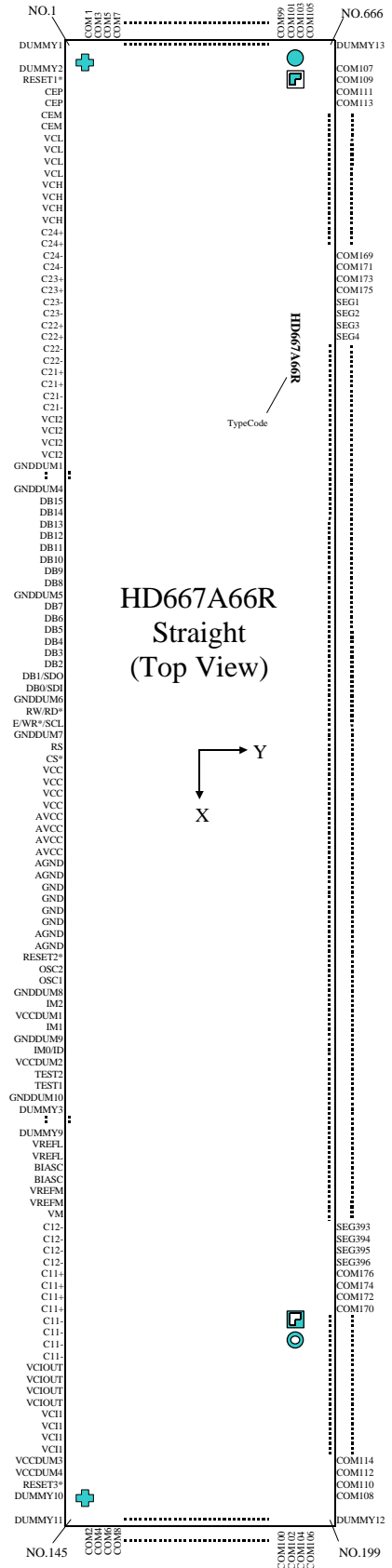
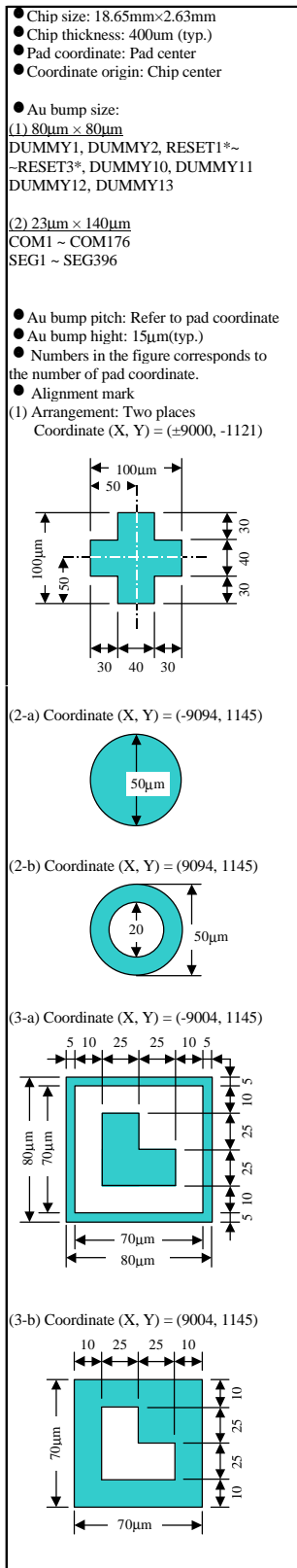


Figure 1 PAD arrangement (Straight)

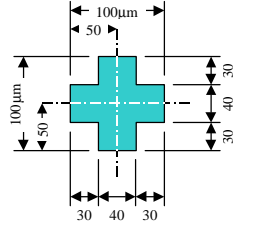
HD66766R PAD Arrangement (LacedOutput Arrangement)

- Chip size: 18.65mm×2.63mm
- Chip thickness: 400μm (typ.)
- Pad coordinate: Pad center
- Coordinate origin: Chip center

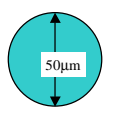
- Au bump size:
 (1) 80μm×80μm
 DUMMY1, DUMMY2, RESET1*~
 ~RESET3*, DUMMY10, DUMMY11
 DUMMY12, DUMMY13
 (2) 38μm×63μm
 COM1~COM176
 SEG1~SEG396

- Au bump pitch: Refer to pad coordinate
- Au bump height: 15μm (typ.)
- Numbers in the figure correspond to the number of pad coordinate.
- Alignment mark

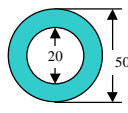
(1) Arrangement: Two places
 Coordinate (X, Y) = (±9000, -1121)



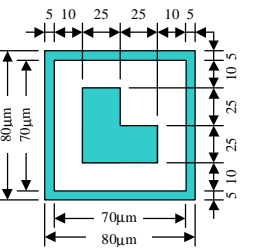
(2-a) Coordinate (X, Y) = (-9094, 1145)



(2-b) Coordinate (X, Y) = (9094, 1145)



(3-a) Coordinate (X, Y) = (-9004, 1145)



(3-b) Coordinate (X, Y) = (9004, 1145)

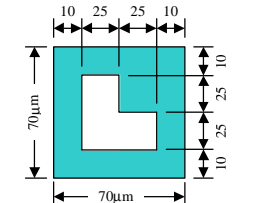
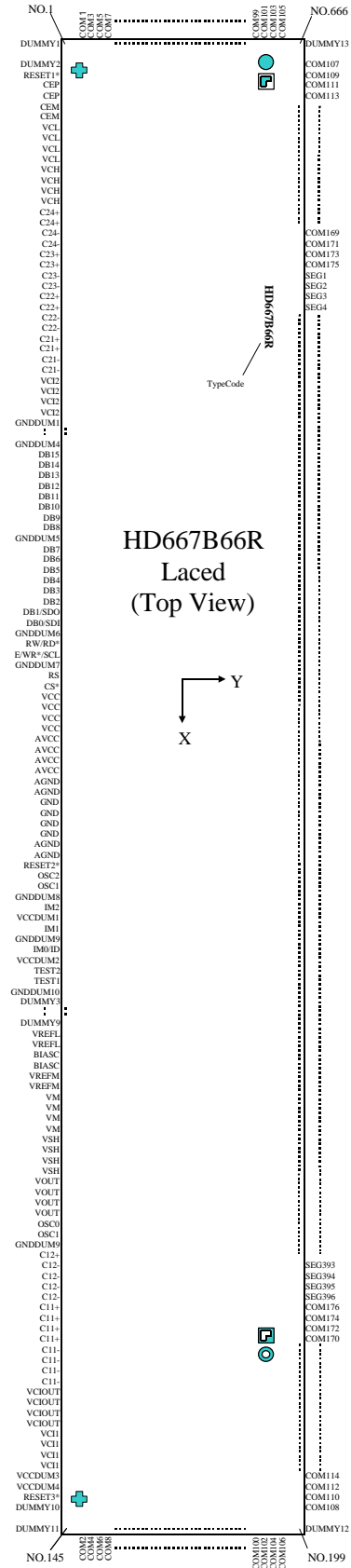



Figure 2 PAD arrangement (Laced)

HD66766R Block Diagram Description

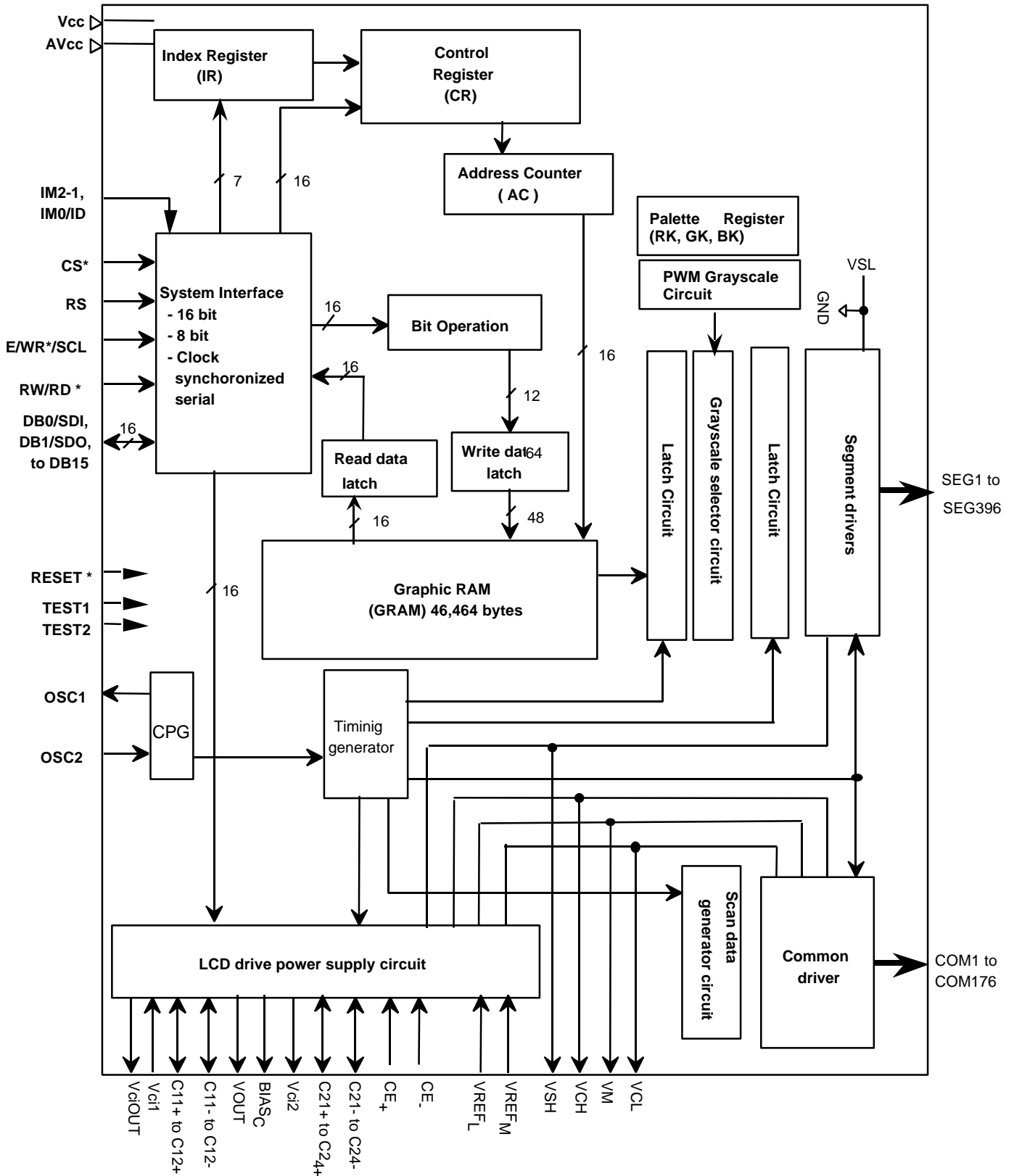


Figure 3 HD66766R Block Diagram Description

Pin Functions

Table 4 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions																								
IM2-1, IM0/ID	3	I	GND or V _{CC}	<p>Selects the MPU interface mode:</p> <table border="1"> <thead> <tr> <th>IM2</th> <th>IM1</th> <th>IM0/ID0</th> <th>MPU Interface mode</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>GND</td> <td>GND</td> <td>68 system 16-bit bus interface</td> </tr> <tr> <td>GND</td> <td>GND</td> <td>V_{CC}</td> <td>68 system 8-bit bus interface</td> </tr> <tr> <td>GND</td> <td>V_{CC}</td> <td>GND</td> <td>80 system 16-bit bus interface</td> </tr> <tr> <td>GND</td> <td>V_{CC}</td> <td>V_{CC}</td> <td>80 system 8-bit bus interface</td> </tr> <tr> <td>V_{CC}</td> <td>GND</td> <td>ID</td> <td>Clock synchronized serial interface</td> </tr> </tbody> </table> <p>When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.</p>	IM2	IM1	IM0/ID0	MPU Interface mode	GND	GND	GND	68 system 16-bit bus interface	GND	GND	V _{CC}	68 system 8-bit bus interface	GND	V _{CC}	GND	80 system 16-bit bus interface	GND	V _{CC}	V _{CC}	80 system 8-bit bus interface	V _{CC}	GND	ID	Clock synchronized serial interface
IM2	IM1	IM0/ID0	MPU Interface mode																									
GND	GND	GND	68 system 16-bit bus interface																									
GND	GND	V _{CC}	68 system 8-bit bus interface																									
GND	V _{CC}	GND	80 system 16-bit bus interface																									
GND	V _{CC}	V _{CC}	80 system 8-bit bus interface																									
V _{CC}	GND	ID	Clock synchronized serial interface																									
CS*	1	I	MPU	<p>Selects the HD66766R: Low: HD66766R is selected and can be accessed High: HD66766R is not selected and cannot be accessed Must be fixed at GND level when not in use.</p>																								
RS	1	I	MPU	<p>Selects the register. Low: Index/status High: Control For a register or a synchronous clock interface, fixed to the V_{CC} or GND level.</p>																								
E/WR*/SCL	1	I	MPU	<p>For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level. For a synchronous clock interface, serves as the synchronous clock signal.</p>																								
RW/RD*	1	I	MPU	<p>For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level. For a synchronous clock interface, fixed to the V_{CC} or GND level.</p>																								
DB0/SDI	1	I/O	MPU	<p>Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the V_{CC} or GND level. For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.</p>																								
DB1/SDO	1	I/O	MPU	<p>Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the V_{CC} or GND level. For a clock-synchronous serial interface, serves as a serial data output pin (SDO). Successive bit values are output on the falling edge of the SCL signal.</p>																								

Table 4 cont.

Signals	Number of Pins	I/O	Connected to	Functions
DB2-DB15	14	I/O	MPU	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level. For a synchronous clock interface or unused pins, fixed to the Vcc or GND level.
SEG1-SEG396	396	O	LCD	Output signals for segment drive. In the display-off period (D1-0 = 00, 01) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1. If SGS = 1, it is output from SEG396. SEG1, SEG4, SEG7, ... display red (R), SEG2, SEG5, SEG8, ... display green (G), and SEG3, SEG6, SEG9, ... display blue (B) (SGS = 0).
COM1-COM176	176	O	LCD	Output signals for common drive. In the display-off period (D1-0 = 00, 01) sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, driver outputs from COM1 to COM176. If CMS = 1, driver outputs COM176 to COM1. Note that start position of the common driver output is changed by screen diving position function.
VCH, VCL	2	—	Capacitor for stabilization, shot key barrier diode or external power supply	Selection level for the common signal. When internal power supply is used, connect the capacitors for stabilization to VCH AND VCL, and shot key barrier diode to VCL. When internal power supply is not used, supply external voltage.
VM	1	—	Capacitor for stabilization or external power supply	Non-selection level for the common signal. When internal operational amplifier is used, it is output of the internal operational amplifier and connect the capacitors for stabilization. When internal operational amplifier is not used, supply external voltage.
VSH	1	—	Capacitor for stabilization or external power supply	Selection level for the segment signal. When internal operational amplifier is used, it is output of the internal operational amplifier and connect the capacitors for stabilization. When internal operational amplifier is not used, supply external voltage.
VciOUT	1	—	Vci1 and capacitor for stabilization or open	Outputs a regulated voltage derived from Vcc. Connect a capacitor for stabilization. When this pin is not used, leave it open.
Vci1	1	—	VciOUT or power supply	Voltage-input pin for step-up circuit 1. When the Vci adjuster is used, input the power supply from VciOUT. When not used, input the external power supply.
Vci2	1	—	Capacitor for stabilization or open	Connect capacitor for stabilization. When the internal power supply circuit is not used, leave this pin open.
VOUT	1	—	Step-up capacitance	A voltage that doubles or triples the voltage between Vci1 and GND is output here. The step-up factor can be set in an internal register.
C11+, C11-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.

Table 4 cont.

Signals	Number of Pins	I/O	Connected to	Functions
C12+, C12-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C21+, C21-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C22+, C22-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C23+, C23-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
C24+, C24-	2	—	Step-up capacitance	When step-up circuit is used, connect a step-up capacitor.
CEP, CEM	2	—	Step-up capacitance or open	Connect a step-up capacitor to generate VCL level by VCH and VM. When step-up circuit is not used, leave this pin open.
VREFL	1	—	VCC or external power supply	Inputs reference voltage for LCD drives power supply. Input lower level than Vcc. Since input current does not run, level input, which is divided by resistors, is also possible.
VREFM	1	—	Capacitor for stabilization or external power supply	Connect capacitor for stabilization for internal power supply. When internal operational amplifier is not used, supply external voltage.
BIASC	1	—	Capacitor for stabilization or open	Connect capacitor for stabilization for internal power supply.
VCC, GND	2	—	Power supply	VCC: + 2.2 V to + 3.6 V; GND (logic): 0 V
AVCC	1	—	—	VCC for power supply circuit. Input the same level of voltage as VCC.
AGND	1	—	—	GND for power supply circuit.
OSC1, OSC2	2	I/O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When providing clocks from outside, input clock to OCS1 and leave OSC2 open.
RESET*	1	I	MPU or external R-C circuit Open unused pins	Reset pin. Initializes the LSI when low. Must be reset after power-on. Since HCD66766RBP has three RESET pins, use one pin and open unused two pins.
VccDUM	1	O	Input pins	Outputs the internal VCC level; shorting this pin sets the adjacent input pin to the VCC level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	1	—	—	Dummy pad. Must be left disconnected.
TEST1, TEST 2	2	I	GND	Test pin. Must be fixed at GND level.

Block Function Description

System Interface

The HD66766R has five high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, and a Clock synchronized serial interface. The IM2-0 pins select the interface mode. The HD66766R has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal.

Execution time for instruction excluding oscillation start is 0-clock cycle and instructions can be written in succession.

Table 5 Register Selection (8/16 Parallel Interface)

80-series Bus		68-series Bus		Operations
WR	RD	R/W	RS	
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Table 6 Register Selection (Clock synchronized Serial Interface)

Start bytes

R/W Bit	RS Bit	Operations
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers and GRAM through WDR
1	1	Reads from GRAM through RDR

Bit Operation

The HD66766R supports the following functions. A write data mask function that selects data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing load of the MPU graphics software the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns address to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. After writing into the GRAM, the AC is automatically incremented by 1 (or decrement by 1). After reading from the GRAM, the AC is not updated.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has twelve bits/pixel and stores the bit-pattern data of 132 x 176 bytes.

PWM Grayscale Palette Circuit

The grayscale palette generates a PWM signal, which corresponds to specified grayscale level. Any 65K out of the 140K possible colors can be displayed at the same time.

Grayscale Control Circuit

The grayscale control circuit performs 16-grayscale control with the pulse width modulation (PWM) method for grayscale display for each color.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access is generated separately to avoid interference with one another.

Oscillation Circuit (OSC)

The HD66766R can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 176 common signal drivers (COM1 to COM176) and 396 segment signal drivers (SEG1 to SEG396).

Display pattern data from GRAM is latched to the 396-bit latch circuit. The latched data then enables the segment signal drivers to generate drive waveform outputs. The common driver outputs one of the VCH, VM or VCL voltage level. The SGS bit can change the shift direction of 396-bit data for the segment. The CMS bit can also change the shift direction for the common by selecting an appropriate direction for the device-mounting configuration.

When display is off, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

LCD drive power supply circuit

LCD drive power supply circuit generates VCH, VSH, VM and VCL voltage level to drive LCD panel.

GRAM ADDRESS DIAGRAM (HD66766R)

Table 7 Relationship between GRAM address and display position (SGS = "0")

SEG/COM pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
CMS=0	CMS=1	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0		DB 15	DB 0	DB 15	DB 0	DB 15	DB 0	DB 15	DB 0
COM1	COM176	"0000"	H	"0001"	H	"0002"	H	"0003"	H	"0080"	H	"0081"	H	"0082"	H	"0083"	H								
COM2	COM175	"0100"	H	"0101"	H	"0102"	H	"0103"	H	"0180"	H	"0181"	H	"0182"	H	"0183"	H								
COM3	COM174	"0200"	H	"0201"	H	"0202"	H	"0203"	H	"0280"	H	"0281"	H	"0282"	H	"0283"	H								
COM4	COM173	"0300"	H	"0301"	H	"0302"	H	"0303"	H	"0380"	H	"0381"	H	"0382"	H	"0383"	H								
COM5	COM172	"0400"	H	"0401"	H	"0402"	H	"0403"	H	"0480"	H	"0481"	H	"0482"	H	"0483"	H								
COM6	COM171	"0500"	H	"0501"	H	"0502"	H	"0503"	H	"0580"	H	"0581"	H	"0582"	H	"0583"	H								
COM7	COM170	"0600"	H	"0601"	H	"0602"	H	"0603"	H	"0680"	H	"0681"	H	"0682"	H	"0683"	H								
COM8	COM169	"0700"	H	"0701"	H	"0702"	H	"0703"	H	"0780"	H	"0781"	H	"0782"	H	"0783"	H								
COM9	COM168	"0800"	H	"0801"	H	"0802"	H	"0803"	H	"0880"	H	"0881"	H	"0882"	H	"0883"	H								
COM10	COM167	"0900"	H	"0901"	H	"0902"	H	"0903"	H	"0980"	H	"0981"	H	"0982"	H	"0983"	H								
COM11	COM166	"0A00"	H	"0A01"	H	"0A02"	H	"0A03"	H	"0A80"	H	"0A81"	H	"0A82"	H	"0A83"	H								
COM12	COM165	"0B00"	H	"0B01"	H	"0B02"	H	"0B03"	H	"0B80"	H	"0B81"	H	"0B82"	H	"0B83"	H								
COM13	COM164	"0C00"	H	"0C01"	H	"0C02"	H	"0C03"	H	"0C80"	H	"0C81"	H	"0C82"	H	"0C83"	H								
COM14	COM163	"0D00"	H	"0D01"	H	"0D02"	H	"0D03"	H	"0D80"	H	"0D81"	H	"0D82"	H	"0D83"	H								
COM15	COM162	"0E00"	H	"0E01"	H	"0E02"	H	"0E03"	H	"0E80"	H	"0E81"	H	"0E82"	H	"0E83"	H								
COM16	COM161	"0F00"	H	"0F01"	H	"0F02"	H	"0F03"	H	"0F80"	H	"0F81"	H	"0F82"	H	"0F83"	H								
COM17	COM160	"1000"	H	"1001"	H	"1002"	H	"1003"	H	"1080"	H	"1081"	H	"1082"	H	"1083"	H								
COM18	COM159	"1100"	H	"1101"	H	"1102"	H	"1103"	H	"1180"	H	"1181"	H	"1182"	H	"1183"	H								
COM19	COM158	"1200"	H	"1201"	H	"1202"	H	"1203"	H	"1280"	H	"1281"	H	"1282"	H	"1283"	H								
COM20	COM157	"1300"	H	"1301"	H	"1302"	H	"1303"	H	"1380"	H	"1381"	H	"1382"	H	"1383"	H								
⋮	⋮	⋮		⋮		⋮		⋮			⋮		⋮		⋮		⋮									
COM169	COM8	"A800"	H	"A801"	H	"A802"	H	"A803"	H	"A880"	H	"A881"	H	"A882"	H	"A883"	H								
COM170	COM7	"A900"	H	"A901"	H	"A902"	H	"A903"	H	"A980"	H	"A981"	H	"A982"	H	"A983"	H								
COM171	COM6	"AA00"	H	"AA01"	H	"AA02"	H	"AA03"	H	"AA80"	H	"AA81"	H	"AA82"	H	"AA83"	H								
COM172	COM5	"AB00"	H	"AB01"	H	"AB02"	H	"AB03"	H	"AB80"	H	"AB81"	H	"AB82"	H	"AB83"	H								
COM173	COM4	"AC00"	H	"AC01"	H	"AC02"	H	"AC03"	H	"AC80"	H	"AC81"	H	"AC82"	H	"AC83"	H								
COM174	COM3	"AD00"	H	"AD01"	H	"AD02"	H	"AD03"	H	"AD80"	H	"AD81"	H	"AD82"	H	"AD83"	H								
COM175	COM2	"AE00"	H	"AE01"	H	"AE02"	H	"AE03"	H	"AE80"	H	"AE81"	H	"AE82"	H	"AE83"	H								
COM176	COM1	"AF00"	H	"AF01"	H	"AF02"	H	"AF03"	H	"AF80"	H	"AF81"	H	"AF82"	H	"AF83"	H								

Table 8 Relationship between GRAM data and output pin

GRAM DATA	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	PK palette				PK palette + FRC				PK palette							
Output pin	SEG (3n+1)				SEG (3n+2)				SEG (3n+3)							

Note: n = Lower 8 bits address (0 to 131)

Table 9 Relationship between GRAM address and display position (SGS = "1")

SEG/COM pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	...	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396	
CMS=0	CMS=1	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	DB ₀ ... DB ₁₅	
COM1	COM176	"0083"H	"0082"H	"0081"H	"0080"H	"0003"H	"0002"H	"0001"H	"0000"H																	
COM2	COM175	"0183"H	"0182"H	"0181"H	"0180"H	"0103"H	"0102"H	"0101"H	"0100"H																	
COM3	COM174	"0283"H	"0282"H	"0281"H	"0280"H	"0203"H	"0202"H	"0201"H	"0200"H																	
COM4	COM173	"0383"H	"0382"H	"0381"H	"0380"H	"0303"H	"0302"H	"0301"H	"0300"H																	
COM5	COM172	"0483"H	"0482"H	"0481"H	"0480"H	"0403"H	"0402"H	"0401"H	"0400"H																	
COM6	COM171	"0583"H	"0582"H	"0581"H	"0580"H	"0503"H	"0502"H	"0501"H	"0500"H																	
COM7	COM170	"0683"H	"0682"H	"0681"H	"0680"H	"0603"H	"0602"H	"0601"H	"0600"H																	
COM8	COM169	"0783"H	"0782"H	"0781"H	"0780"H	"0703"H	"0702"H	"0701"H	"0700"H																	
COM9	COM168	"0883"H	"0882"H	"0881"H	"0880"H	"08030"H	"0802"H	"0801"H	"0800"H																	
COM10	COM167	"0983"H	"0982"H	"0981"H	"0980"H	"0903"H	"0902"H	"0901"H	"0900"H																	
COM11	COM166	"0A83"H	"0A82"H	"0A81"H	"0A80"H	"0A03"H	"0A02"H	"0A01"H	"0A00"H																	
COM12	COM165	"0B83"H	"0B82"H	"0B81"H	"0B80"H	"0B03"H	"0B02"H	"0B01"H	"0B00"H																	
COM13	COM164	"0C83"H	"0C82"H	"0C81"H	"0C80"H	"0C03"H	"0C02"H	"0C01"H	"0C00"H																	
COM14	COM163	"0D83"H	"0D82"H	"0D81"H	"0D80"H	"0D03"H	"0D02"H	"0D01"H	"0D00"H																	
COM15	COM162	"0E83"H	"0E82"H	"0E81"H	"0E80"H	"0E03"H	"0E02"H	"0E01"H	"0E00"H																	
COM16	COM161	"0F83"H	"0F82"H	"0F81"H	"0F80"H	"0F03"H	"0F02"H	"0F01"H	"0F00"H																	
COM17	COM160	"1083"H	"1082"H	"1081"H	"1080"H	"1003"H	"1002"H	"1001"H	"1000"H																	
COM18	COM159	"1183"H	"1182"H	"1181"H	"1180"H	"1103"H	"1102"H	"1101"H	"1100"H																	
COM19	COM158	"1283"H	"1282"H	"1281"H	"1280"H	"1203"H	"1202"H	"1201"H	"1200"H																	
COM20	COM157	"1383"H	"1382"H	"1381"H	"1380"H	"1303"H	"1302"H	"1301"H	"1300"H																	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
COM169	COM8	"A883"H	"A882"H	"A881"H	"A880"H	"A803"H	"A802"H	"A801"H	"A800"H																	
COM170	COM7	"A983"H	"A982"H	"A981"H	"A980"H	"A903"H	"A902"H	"A901"H	"A900"H																	
COM171	COM6	"AA83"H	"AA82"H	"AA81"H	"AA80"H	"AA03"H	"AA02"H	"AA01"H	"AA00"H																	
COM172	COM5	"AB83"H	"AB82"H	"AB81"H	"AB80"H	"AB03"H	"AB02"H	"AB01"H	"AB00"H																	
COM173	COM4	"AC83"H	"AC82"H	"AC81"H	"AC80"H	"AC03"H	"AC02"H	"AC01"H	"AC00"H																	
COM174	COM3	"AD83"H	"AD82"H	"AD81"H	"AD80"H	"AD03"H	"AD02"H	"AD01"H	"AD00"H																	
COM175	COM2	"AE83"H	"AE82"H	"AE81"H	"AE80"H	"AE03"H	"AE02"H	"AE01"H	"AE00"H																	
COM176	COM1	"AF83"H	"AF82"H	"AF81"H	"AF80"H	"AF03"H	"AF02"H	"AF01"H	"AF00"H																	

Table 10 Relationship between GRAM data and output pin

GRAM DATA	DB ₁₅	DB ₁₄	DB ₁₃	DB ₁₂	DB ₁₁	DB ₁₀	DB ₉	DB ₈	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀
Selected palette	PK palette				PK palette + FRC				PK palette							
Output pin	SEG (396-3n)				SEG (395-3n)				SEG (394-3n)							

Note: n = Lower 8 bits address (0 to 131)

Instructions**Outline**

The HD66766R uses the 16-bit bus architecture. Before the internal operation of the HD66766R starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66766R is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66766R instructions.

- There are eight categories of instructions that:
 - Specify the index

- Read the status
- Control the display

- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index: IR

The index instruction specifies the RAM control indexes (R00h to R3Fh). It sets the register number in the range of 000000 to 111001 in binary form. However, R40 to R44 are disabled since they are test registers.

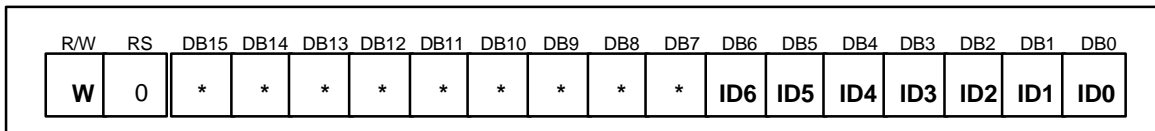


Figure 4 Index Instruction

Status Read: SR

The status read instruction reads the internal status of the HD66766R.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6-0)

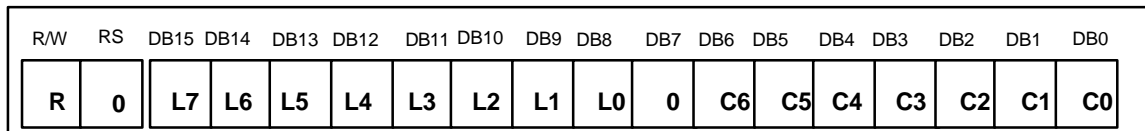


Figure 5 Status Read Instruction

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, “0766”H is read.

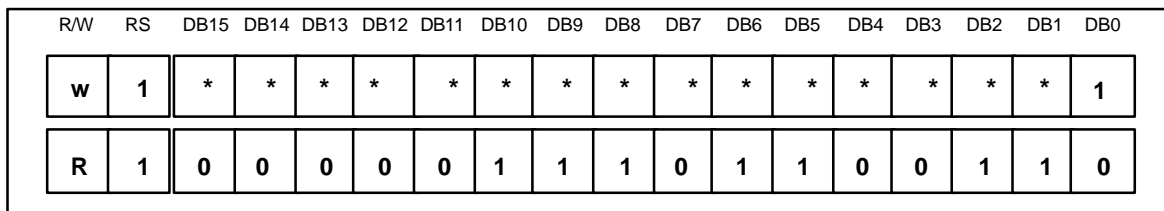


Figure 6 Start Oscillation Instruction

Driver Output Control (R01h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
w	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 7 Driver Output Control Instruction

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM176. When CMS = 1, COM176 shifts to COM1.

SGS: Selects the output shift direction of the segment driver. When SGS = 0, data are output SEG1 to SEG396. When SGS = 1, data are output SEG396 to SEG1. When SGS = 0, SEG1 pin assigns the color display to <R><G>. When SGS = 1, SEG396 pin assigns <R><G>. Re-write to the RAM when intending to change the SGS bit.

NL4-0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio.

Table 11 NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD drive duty cycle	Common driver used	
							CMS="0"	CMS="1"
0	0	0	0	0	396 x 8 dots	1/8 Duty	Com1 - Com8	Com176 - Com169
0	0	0	0	1	396 x 16 dots	1/16 Duty	Com1 - Com16	Com176 - Com161
0	0	0	1	0	396 x 24 dots	1/24 Duty	Com1 - Com24	Com176 - Com153
0	0	0	1	1	396 x 32 dots	1/32 Duty	Com1 - Com32	Com176 - Com145
0	0	1	0	0	396 x 40 dots	1/40 Duty	Com1 - Com40	Com176 - Com137
0	0	1	0	1	396 x 48 dots	1/48 Duty	Com1 - Com48	Com176 - Com129
0	0	1	1	0	396 x 56 dots	1/56 Duty	Com1 - Com56	Com176 - Com121
0	0	1	1	1	396 x 64 dots	1/64 Duty	Com1 - Com64	Com176 - Com113
0	1	0	0	0	396 x 72 dots	1/72 Duty	Com1 - Com72	Com176 - Com105
0	1	0	0	1	396 x 80 dots	1/80 Duty	Com1 - Com80	Com176 - Com97
0	1	0	1	0	396 x 88 dots	1/88 Duty	Com1 - Com88	Com176 - Com89
0	1	0	1	1	396 x 96 dots	1/96 Duty	Com1 - Com96	Com176 - Com81
0	1	1	0	0	396 x 104 dots	1/104 Duty	Com1 - Com104	Com176 - Com73
0	1	1	0	1	396 x 112 dots	1/112 Duty	Com1 - Com112	Com176 - Com65
0	1	1	1	0	396 x 120 dots	1/120 Duty	Com1 - Com120	Com176 - Com57
0	1	1	1	1	396 x 128 dots	1/128 Duty	Com1 - Com128	Com176 - Com49
1	0	0	0	0	396 x 136 dots	1/136 Duty	Com1 - Com136	Com176 - Com41
1	0	0	0	1	396 x 144 dots	1/144 Duty	Com1 - Com144	Com176 - Com33
1	0	0	1	0	396 x 152 dots	1/152 Duty	Com1 - Com152	Com176 - Com25
1	0	0	1	1	396 x 160 dots	1/160 Duty	Com1 - Com160	Com176 - Com17
1	0	1	0	0	396 x 168 dots	1/168 Duty	Com1 - Com168	Com176 - Com9
1	0	1	0	1	396 x 176 dots	1/176 Duty	Com1 - Com176	Com176 - Com1

LCD-Driving-Waveform Control (R02h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 8 LCD-Driving-Waveform Control Instruction

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

RST: When RST = 1, software reset function is started. This function is the same as hardware RESET pin. It takes 10 clock cycle period. This bit is automatically cleared after reset function is completed. Therefore, before 10-clock cycle other instruction can not be issued. Do not set the RST bit during stand-by mode.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Power Control 1 (R03h)

Power Control 2 (R0Ch)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
w	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP2	SLP	STB
w	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Figure 9 Power Control Instruction

BS3-0: The LCD drive bias value is set. The LCD drive bias value can be selected according to its drive duty ratio and voltage.

BT2–0: The output factor of step-up circuit is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

BT3: Operation/halt of voltage inverting circuit is set. BT3="0": voltage-inverting circuit is halted. BT3="1": voltage-inverting circuit is operated. See the Power-on/off Sequence section to be activated.

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit becomes high, but the current consumption is increased. Adjust the frequency considering the step-up ability and the current consumption.

AP1-0: The amount of fixed current from the fixed current source in the operational amplifier for the LCD is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP1-0 = "00", the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

VC2-0: Set an adjustment factor for the Vci1 voltage (VC2-0).

SLP: When SLP = 1, the HD66766R enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

Power control (BS2-0, BT3-0, DC2-0, AP1-0, SLP, STB)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66766R enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = "0")

b. Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

The VSH voltage should be controlled to be less than supply voltage or device proof voltage level since VCH voltage level is generated by bias amplifier ratio corresponding to LCD driving bias value and boosting ratio of the step-up circuit 2.

Table 12 Display bias setting table

Determine the LCD drive bias according to its display duty, and select combination of boosting ratio of the step-up circuit 2 and bias amplifier ratio so as not to exceed voltage control of Vci2 and VCH. See the LCD Voltage Generation Circuit regarding how to determine the LCD drive bias, VCH voltage and contrast adjustment for the following settings.

LCD driving bias	Booster ratio of the step-up circuit 2 (ND2)	BS3	BS2	BS1	BS0	Bias ratio (NB)	Vci2 (Vci2≤VOU T-0.5V)	VCH (VCH≤22V)
1/2	x 2	0	0	0	0	0.75	1.50 x VM	Vci2 x 2
	x 3	-	-	-	-	N/A	-	-
	x 4	-	-	-	-	N/A	-	-
1/4	x 2	0	1	0	0	1.25	2.50 x VM	Vci2 x 2
	x 3	0	0	0	1	0.825	1.75 x VM	Vci2 x 3
	x 4	-	-	-	-	N/A	-	-
1/6	x 2	1	0	1	1	1.75	3.50 x VM	Vci2 x 2
	x 3	0	0	1	1	1.165	2.33 x VM	Vci2 x 3
	x 4	-	-	-	-	N/A	-	-
1/8	x 2	-	-	-	-	N/A	-	-
	x 3	1	0	0	0	1.50	3.00 x VM	Vci2 x 3
	x 4	0	0	1	0	1.125	2.25 x VM	Vci2 x 4
1/9	x 2	-	-	-	-	N/A	-	-
	x 3	1	0	1	0	1.675	3.35 x VM	Vci2 x 3
	x 4	0	1	0	0	1.25	2.50 x VM	Vci2 x 4
1/10	x 2	-	-	-	-	N/A	-	-
	x 3	1	1	0	0	1.825	3.65 x VM	Vci2 x 3
	x 4	0	1	1	0	1.375	2.75 x VM	Vci2 x 4
1/11	x 2	-	-	-	-	N/A	-	-
	x 3	1	1	0	1	2.00	4.00 x VM	Vci2 x 3
	x 4	1	0	0	0	1.50	3.00 x VM	Vci2 x 4
1/12	x 3	-	-	-	-	N/A	-	-
	x 4	1	0	0	1	1.625	3.25 x VM	Vci2 x 4
	x 5	0	1	0	1	1.3	2.60 x VM	Vci2 x 5
1/13	x 3	-	-	-	-	N/A	-	-
	x 4	1	0	1	1	1.75	3.45 x VM	Vci2 x 4
	x 5	0	1	1	1	1.4	2.80 x VM	Vci2 x 5

Table 13 Display bias setting table

VC2	VC1	VC0	Vci1 control range
0	0	0	0.92 x Vcc
0	0	1	0.87 x Vcc
0	1	0	0.83 x Vcc
0	1	1	0.8 x Vcc
1	0	0	0.76 x Vcc
1	0	1	0.73 x Vcc
1	1	0	0.68 x Vcc
1	1	1	Vci1 control amplifier suspends. (Vci1 can be supplied externally.)

Table 14 AP bits and amount of fixed current

AP1	AP0	Amount of fixed current in the operational amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

Table 15 Output voltage ratio of the booster 1 and 2

BT2	BT1	BT0	VOUT output of the booster 1 (Use VOUT within the range of 4.0 to 5.75V.)	VCH output of the booster 2 (Set VCH lower than 22.0V.)
0	0	0	2 x Vci1	2 x Vci2
0	0	1	3 x Vci1	2 x Vci2
0	1	0	2 x Vci1	3 x Vci2
0	1	1	3 x Vci1	3 x Vci2
1	0	0	2 x Vci1	4 x Vci2
1	0	1	3 x Vci1	4 x Vci2
1	1	0	2 x Vci1	5 x Vci2
1	1	1	3 x Vci1	5 x Vci2

Set the factor of the booster 2 according to voltage of Vci2 and VCH.

When the factor is set low, current consumption can be lowered.

Table 16 Operating clock frequency of the Booster 1 and 2

DC2	DC1	DC0	Operating clock frequency in the booster 1	Operating clock frequency in the voltage inverting circuit and the booster 2
0	0	0	32-divided clock	32-divided clock
0	0	1	64-divided clock	32-divided clock
0	1	0	32-divided clock	64-divided clock
0	1	1	64-divided clock	64-divided clock
1	0	0	32-divided clock	96-divided clock
1	0	1	64-divided clock	96-divided clock
1	1	0	32-divided clock	128-divided clock
1	1	1	64-divided clock	128-divided clock

Operation of voltage inverting circuit

Table 17

BT3	VCL output of the voltage inverting circuit (Set VCL no lower than -22.0V.)
0	Halt boosting
1	Output voltage between VCH and VM by inverting

Set activation of voltage inverting circuit with output of the booster 2 stable. *See the Power-on/off Sequence section.

DB 15 Contrast Control (R04h)

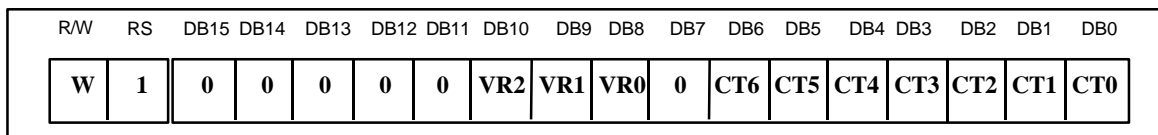


Figure 10 Contrast Control Instruction

CT6-0: These bits control the LCD drive voltage to adjust 128-step contrast.

Table 18 Contrast control

CT6	CT5	CT4	CT3	CT2	CT1	CT0	Contrast
0	0	0	0	0	0	0	1.016R (Minimum)
0	0	0	0	0	0	1	1.008R
0	0	0	0	0	1	0	1.000R
0	0	0	0	0	1	1	0.992R
0	0	0	0	1	0	0	0.984R
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0.008R
1	1	1	1	1	1	1	0.000R (Maximum)

VR2-0: These bits amplifies 1.1 to 3.4 times the VREFL as output voltage VREFM of LCD drive reference voltage generation circuit. The VREFM should be smaller than VOUT level.

Table 19 Contrast control

VR2	VR1	VR0	VREFM voltage
0	0	0	VREFL x 1.1
0	0	1	VREFL x 1.3
0	1	0	VREFL x 1.4
0	1	1	VREFL x 1.5
1	0	0	VREFL x 1.7
1	0	1	VREFL x 1.8
1	1	0	VREFL x 3.4

Entry Mode (R05h)

Compare register (R06h)

The write data sent from the microcomputer is modified in the HD66766R and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For detail, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SPR	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

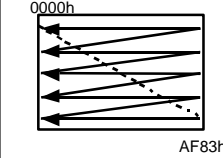
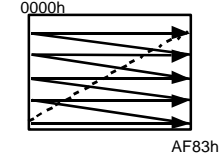
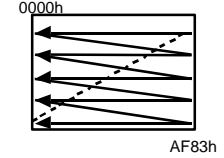
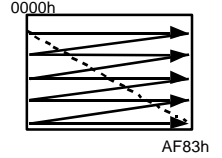
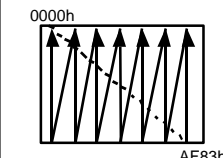
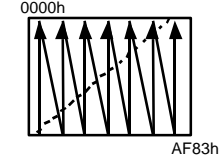
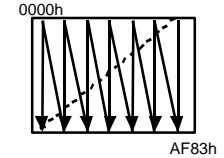
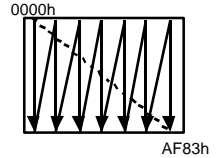
Figure 11 Compare Resister Instruction

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after the writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see the High-Speed RAM Write Mode section.

I/D1-0: When I/D1-0 = "1", the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = "0", the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD7-0) addresses. The AM bit sets the direction of moving through the addresses when the GRAM is written to.

AM set the automatic update method of the AC after the data is written to the GRAM. When AM= "0", the data is continuously written in parallel. When AM = "1", the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

SPR: When SPR=1, 4096colors are displayed. 12 bit (DB11-DB0) are used for this display. Refer to "4096 color display function" in page 57 for details.

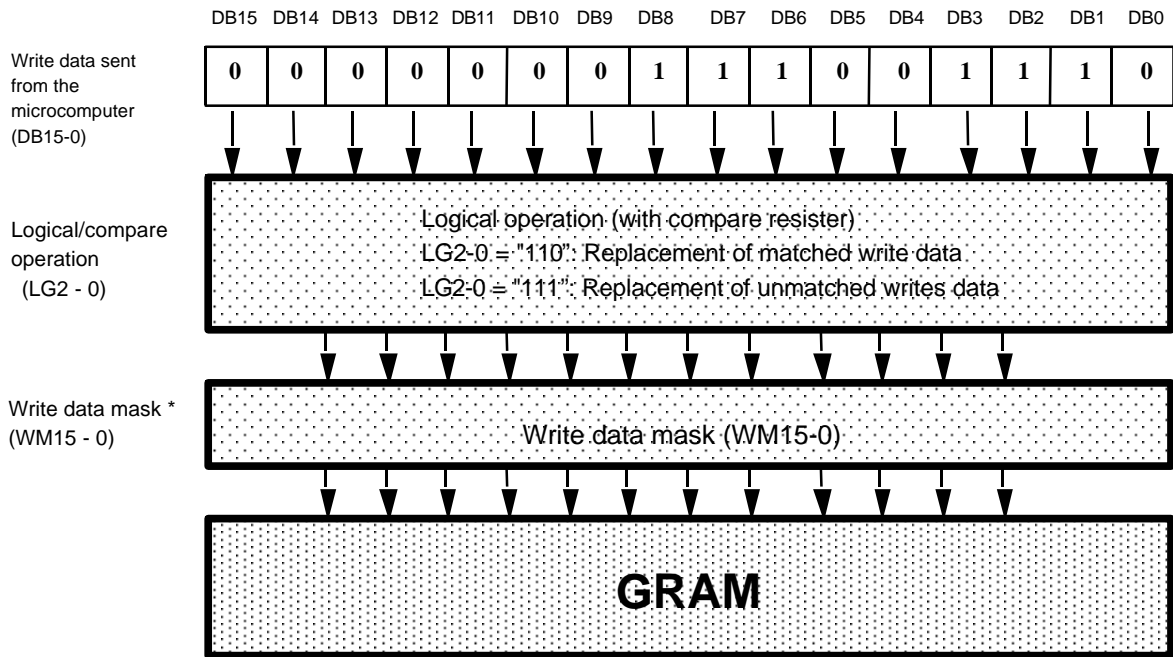
	I/D1-0="00" Horizontal: decrement Vertical: decrement	I/D1-0="01" Horizontal: increment Vertical: decrement	I/D1-0="10" Horizontal: decrement Vertical: increment	I/D1-0="11" Horizontal: increment Vertical: increment
AM="0" Horizontal				
AM="1" Vertical				

Note: When a window address range has been set the GRAM can only be written to within that range.

Figure 12 Address Direction Settings

LG2-0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP15-0) by a compare/logical operation and writes the results to GRAM. For details, see the Logical/Compare Operation Function.

CP15-0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.



Note: The write data mask (WM15-0) is set by the register in the (20) RAM Write Data Mask section.

Figure 13 Logical/Compare Operation for the GRAM

Display Control (R07h)

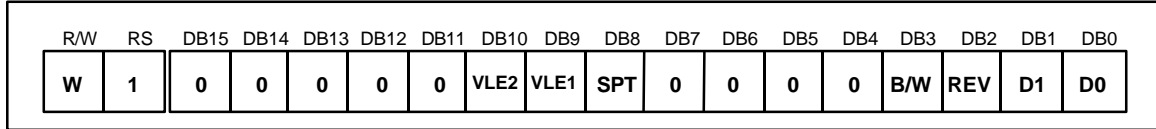


Figure 14 Display Control

VLE2-1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = “1”, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

B/W: When B/W = “1”, displayed data can be “all” or “all off” regardless GRAM contents. (B/W = “1”, REV = “0”: all pixel on, B/W = “1”, REV = “1”: all pixel off) When B/W = “1”, grayscale palette has to be default value.

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

D1-0: Display is on when D1 = “1” and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = “1”. When D1 is “0”, the display is off with all of the SEG/COM pin outputs set to the GND level. Because of this, the HD66766R can control the charging current for the LCD with AC driving.

When D1-0 = “01”, the internal display of the HD66766R is performed although the display is off. When D1-0 = “00”, the internal display operation halts and the display is off.

Table 20 D Bits and Operation

HD66766R Internal Display			
D1	D0	SEG/COM Output	Operation
0	0	GND	Halt
0	1	GND	Operate
1	0	Unlit display	Operate
1	1	Display	Operate

- Notes:
1. Writing from the microcomputer to the GRAM is independent from the state of D1-0.
 2. In the sleep and standby modes, D1-0 = 00. However, the register contents of D1-0 are not modified.

Frame Cycle Control (R0Bh)

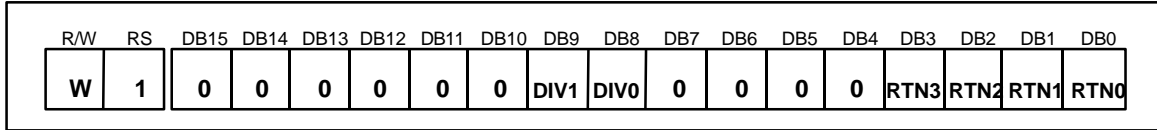


Figure 15

RTN3-0: Set the line retrace period (RTN3-0) to be added to raster-row cycles. The raster-row cycle becomes long according to the number of clocks set at RTN3-0.

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the line retrace period (RTN3-0). When changing the drive-duty, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

Table 21 RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Line retrace period (Clock Cycles)	Clock Cycles per one raster-row
0	0	0	0	0 clock	26 clock
0	0	0	1	1 clock	27 clock
0	0	1	0	2 clock	28 clock
0	0	1	1	3 clock	29 clock
:	:	:	:	:	:
1	1	1	0	14 clock	40 clock
1	1	1	1	15 clock	41 clock

Table 22 DIV Bits and Clock Frequency

DIV1	DIV0	Division ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

* fosc=R-C oscillation frequency

Formula for the frame frequency

Frame frequency = $\frac{fosc}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}}$ [Hz]

fosc: RC oscillation frequency
 Duty: Drive duty (NL bit)
 Division ratio: DIV bit
 Clock cycles per raster-row: (RTN+26) clock

Vertical Scroll Control (R11h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10

Figure 16 Vertical Scroll Control Instruction

VL17-10: Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 176th can be selected. After the 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL17-10) is valid only when VLE1 = “1”. The raster-row display is fixed when VLE1 = “0”. (VLE1 is the 1st-screen vertical-scroll enable bit.)

VL27-20: Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL27-20) is valid only when VLE2 = “1”. The raster-row display is fixed when VLE2 = “0”. (VLE2 is the 1st-screen vertical-scroll enable bit.)

Table 23

VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	Display start line
VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	
0	0	0	0	0	0	0	0	1'st raster - row
0	0	0	0	0	0	0	1	2'nd raster - row
0	0	0	0	0	0	1	0	3'rd raster - row
:	:	:	:	:	:	:	:	:
1	0	1	0	1	1	1	0	175'th raster -
1	0	1	0	1	1	1	1	176'th raster -

Note: Do not set over the 176th ("AF"H) raster - row

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 17

SS17-0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE17-0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17-10 = "07"H and SE17-10 = "10"H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed from COM1 to COM7, COM18 and others. Ensure that SS17-10 ≤ SE17-10 ≤ "AF"H. For details, see the Screen-division Driving Function section.

SS27-0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = "1".

SE27-0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = "1", SS27-20 = "20"H, and SE27-20 = "4F"H are set, the LCD driving is performed from COM33 to COM80. Ensure that SS17-10 ≤ SE17-10 ≤ SS27-20 ≤ SE27-20 ≤ "AF"H. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R16h)

Vertical RAM Address Position (R17h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 18 Horizontal/Vertical RAM Address Position Instruction

HSA5-0/HEA5-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA7-0 from the address specified by HSA5-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ 83h

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "AF"h.

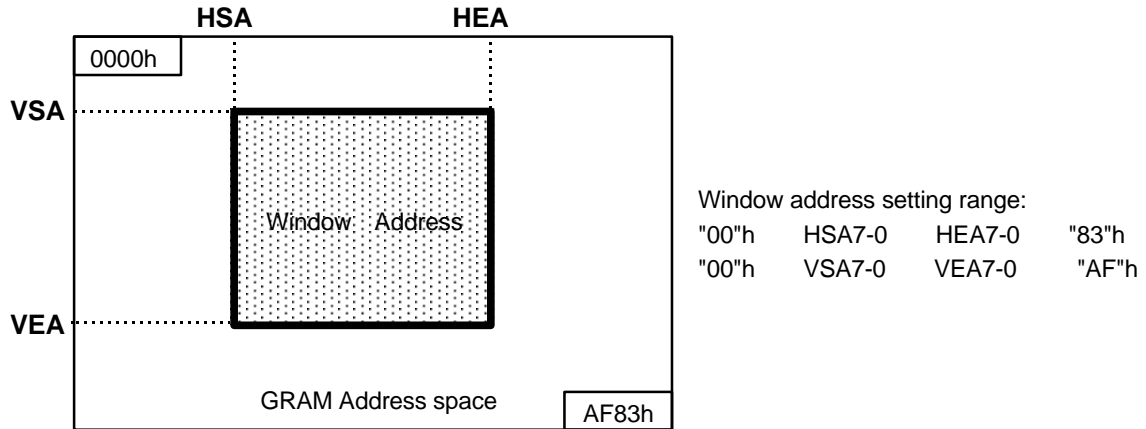


Figure 19 Window Address Setting Range

- Note:
1. Ensure that the window address area is within the GRAM address space.
 2. In high-speed write mode, data are written to GRAM in four-words.
Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.

RAM Write Data Mask (R20h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

Figure 20 RAM Write Data Mask Instruction

WM15-0: In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = "1", this bit masks the write data of DB11 and does not write to the GRAM. Similarly, the WM10 to 0 bits mask the write data of DB15 to 0 in a bit unit. When HDZ = "1", mask processing is performed for 12-bit data after dither processing. For details, see the Write Data Mask Function section.

RAM Address Set (R21h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 21 RAM Address Set Instruction

AD15-0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated.

GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 24 GRAM Address Range

AD15 to AD0	GRAM Setting
"0000"H to "0083"H	Bitmap data for COM1
"0100"H to "0183"H	Bitmap data for COM2
"0200"H to "0283"H	Bitmap data for COM3
"0300"H to "0383"H	Bitmap data for COM4
⋮	⋮
"AC00"H to "AC83"H	Bitmap data for COM173
"AD00"H to "AD83"H	Bitmap data for COM174
"AE00"H to "AE83"H	Bitmap data for COM175
"AF00"H to "AF83"H	Bitmap data for COM176

Write Data to GRAM (R22h)

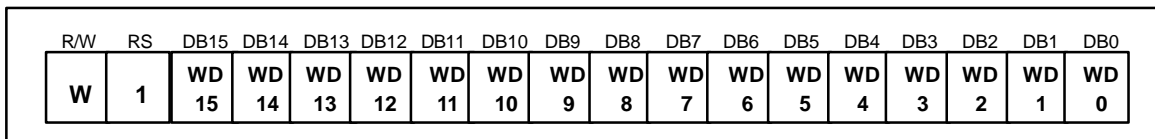


Figure 22 Write Data to GRAM Instruction

WD15-0 : Write 16-bit data to the GRAM; This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the stand by mode, the GRAM cannot be accessed.

GRAM write data during normal mode

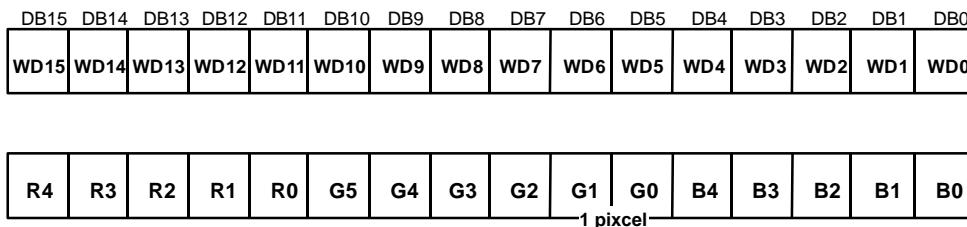


Figure 23

Table 25

GRAM data setting						Grayscale palette					
R4	R3	R2	R1	R0	G0						
G5	G4	G3	G2	G1							
B4	B3	B2	B1	B0							
0	0	0	0	0	0	PK05	PK04	PK03	PK02	PK01	PK00
0	0	0	0	1	0	PK15	PK14	PK13	PK12	PK11	PK10
0	0	0	1	0	0	PK25	PK24	PK23	PK22	PK21	PK20
0	0	0	1	1	0	PK35	PK34	PK33	PK32	PK31	PK30
0	0	1	0	0	0	PK45	PK44	PK43	PK42	PK41	PK40
0	0	1	0	1	0	PK55	PK54	PK53	PK52	PK51	PK50
0	0	1	1	0	0	PK65	PK64	PK63	PK62	PK61	PK60
0	0	1	1	1	0	PK75	PK74	PK73	PK72	PK71	PK70
0	1	0	0	0	0	PK85	PK84	PK83	PK82	PK81	PK80
0	1	0	0	1	0	PK95	PK94	PK93	PK92	PK91	PK90
0	1	0	1	0	0	PK105	PK104	PK103	PK102	PK101	PK100
0	1	0	1	1	0	PK115	PK114	PK113	PK112	PK111	PK110
0	1	1	0	0	0	PK125	PK124	PK123	PK122	PK121	PK120
0	1	1	0	1	0	PK135	PK134	PK133	PK132	PK131	PK130
0	1	1	1	0	0	PK145	PK144	PK143	PK142	PK141	PK140
0	1	1	1	1	0	PK155	PK154	PK153	PK152	PK151	PK150
1	0	0	0	0	0	PK165	PK164	PK163	PK162	PK161	PK160
1	0	0	0	1	0	PK175	PK174	PK173	PK172	PK171	PK170
1	0	0	1	0	0	PK185	PK184	PK183	PK182	PK181	PK180
1	0	0	1	1	0	PK195	PK194	PK193	PK192	PK191	PK190
1	0	1	0	0	0	PK205	PK204	PK203	PK202	PK201	PK200
1	0	1	0	1	0	PK215	PK214	PK213	PK212	PK211	PK210
1	0	1	1	0	0	PK225	PK224	PK223	PK222	PK221	PK220
1	0	1	1	1	0	PK235	PK234	PK233	PK232	PK231	PK230
1	1	0	0	0	0	PK245	PK244	PK243	PK242	PK241	PK240
1	1	0	0	1	0	PK255	PK254	PK253	PK252	PK251	PK250
1	1	0	1	0	0	PK265	PK264	PK263	PK262	PK261	PK260
1	1	0	1	1	0	PK275	PK274	PK273	PK272	PK271	PK270
1	1	1	0	0	0	PK285	PK284	PK283	PK282	PK281	PK280
1	1	1	0	1	0	PK295	PK294	PK293	PK292	PK291	PK290
1	1	1	1	0	0	PK305	PK304	PK303	PK302	PK301	PK300
1	1	1	1	1	0	PK315	PK314	PK313	PK312	PK311	PK310

Note: When G0 = 1, selective grayscale for G pixel is the middle grayscale between the upper grayscale and the selective grayscale.

Read Data from GRAM (R22h)

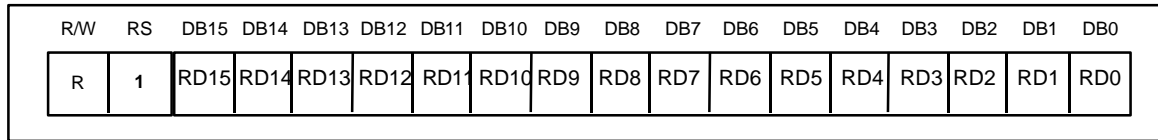


Figure 24 Read Data from GRAM Instruction

RD15-0: Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15-0) becomes invalid and the second-word read is normal.

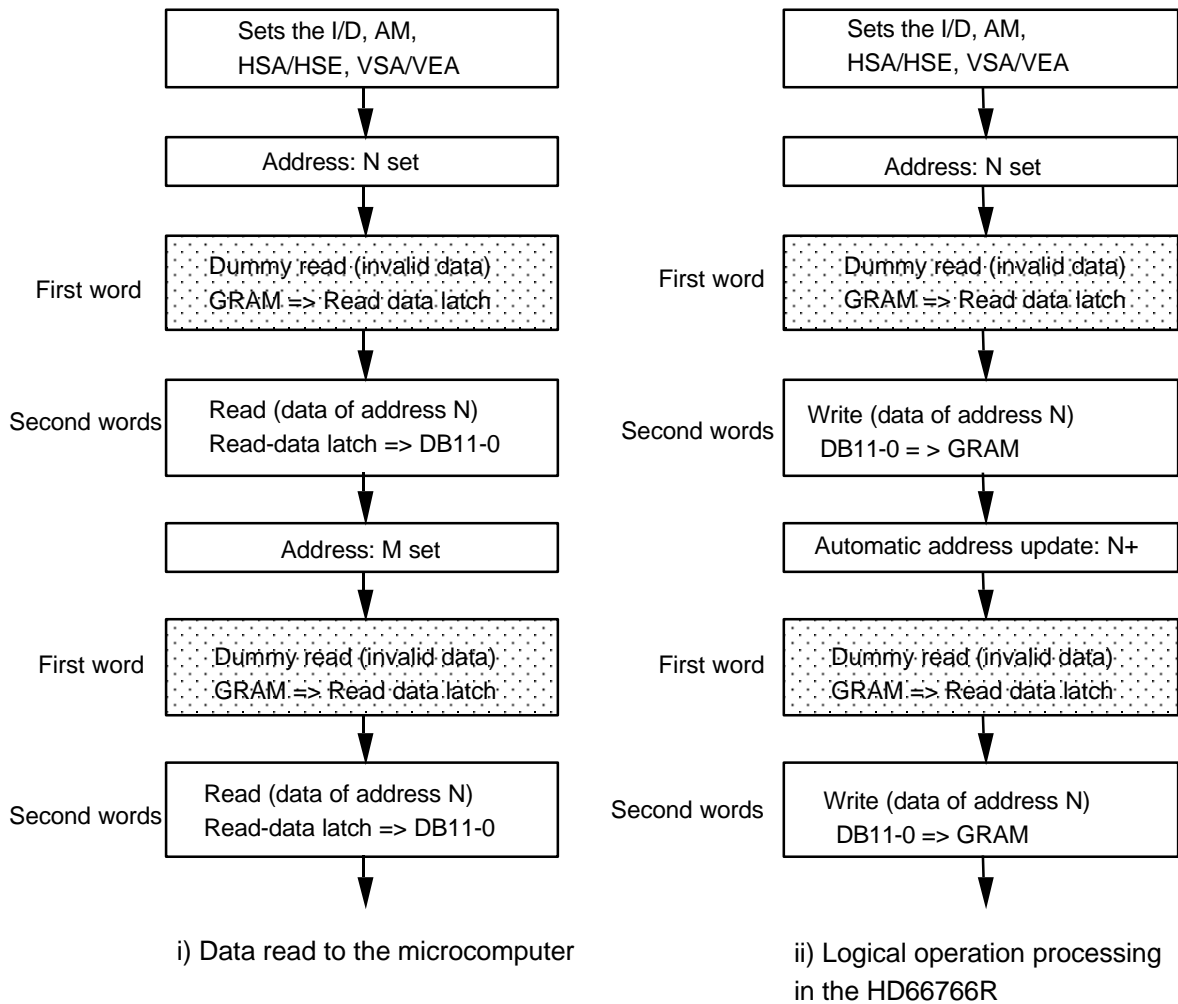


Figure 25 GRAM Read Sequence

Gray Scale Palette Control (R30h to R3Fh)

Table 26 Grayscale Palette Control Instruction

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	PK 15	PK 14	PK 13	PK 12	PK 11	PK 10	0	0	PK 05	PK 04	PK 03	PK 02	PK 01	PK 00
R31	W	1	0	0	PK 35	PK 34	PK 33	PK 32	PK 31	PK 30	0	0	PK 25	PK 24	PK 23	PK 22	PK 21	PK 20
R32	W	1	0	0	PK 55	PK 54	PK 53	PK 52	PK 51	PK 50	0	0	PK 45	PK 44	PK 43	PK 42	PK 41	PK 40
R33	W	1	0	0	PK 75	PK 74	PK 73	PK 72	PK 71	PK 70	0	0	PK 65	PK 64	PK 63	PK 62	PK 61	PK 60
R34	W	1	0	0	PK 95	PK 94	PK 93	PK 92	PK 91	PK 90	0	0	PK 85	PK 84	PK 83	PK 82	PK 81	PK 80
R35	W	1	0	0	PK 115	PK 114	PK 113	PK 112	PK 111	PK 110	0	0	PK 105	PK 104	PK 103	PK 102	PK 101	PK 100
R36	W	1	0	0	PK 135	PK 134	PK 133	PK 132	PK 131	PK 130	0	0	PK 125	PK 124	PK 123	PK 122	PK 121	PK 120
R37	W	1	0	0	PK 155	PK 154	PK 153	PK 152	PK 151	PK 150	0	0	PK 145	PK 144	PK 143	PK 142	PK 141	PK 140
R38	W	1	0	0	PK 175	PK 174	PK 173	PK 172	PK 171	PK 170	0	0	PK 165	PK 164	PK 163	PK 162	PK 161	PK 160
R39	W	1	0	0	PK 195	PK 194	PK 193	PK 192	PK 191	PK 190	0	0	PK 185	PK 184	PK 183	PK 182	PK 181	PK 180
R3A	W	1	0	0	PK 215	PK 214	PK 213	PK 212	PK 211	PK 210	0	0	PK 205	PK 204	PK 203	PK 202	PK 201	PK 200
R3B	W	1	0	0	PK 235	PK 234	PK 233	PK 232	PK 231	PK 230	0	0	PK 225	PK 224	PK 223	PK 222	PK 221	PK 220
R3C	W	1	0	0	PK 255	PK 254	PK 253	PK 252	PK 251	PK 250	0	0	PK 245	PK 244	PK 243	PK 242	PK 241	PK 240
R3D	W	1	0	0	PK 275	PK 274	PK 273	PK 272	PK 271	PK 270	0	0	PK 265	PK 264	PK 263	PK 262	PK 261	PK 260
R3E	W	1	0	0	PK 295	PK 294	PK 293	PK 292	PK 291	PK 290	0	0	PK 285	PK 284	PK 283	PK 282	PK 281	PK 280
R3F	W	1	0	0	PK 315	PK 314	PK 313	PK 312	PK 311	PK 310	0	0	PK 305	PK 304	PK 303	PK 302	PK 301	PK 300

PK31-0: Specify the grayscale level for thirty-two palettes from the 52-grayscale level. For details, see the Grayscale Palette and the Grayscale Palette Table sections.

Instruction List (HD66766R)

Table 27

Reg. No.	Register Name	R/W	RS	Upper Code								Lower Code								Description	Execution Cycle			
				DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0					
IR	Index	0	0	*	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0	Note1	
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L7-0) and contrast setting (C6-0).	0			
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms	Note1
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	1	0	0	1	1	0	Reads 0766H.	0			
R01h	Driver output control	0	1	0	0	0	0	0	0	CM	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS) and driving duty ratio (NL4-0).	0			
R02h	LCD-driving-waveform control	0	1	0	0	0	0	0	RST	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets LCD drive AC waveform (B/C), and EOR output (EOR) or the number of n-raster-rows (NW5-0) at C-pattern AC drive.	0			
R03h	Power control 1	0	1	BS3	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1-0), boosting cycle (DC2-0), boosting output multiplying factor (BT2-0), operation of voltage inverting circuit (BT3) and LCD drive bias value (BS3-0).	0			
R04h	Contrast control	0	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the regulator adjustment (VR2-0) and contrast adjustment (CT6-0).	0			
R05h	Entry mode	0	1	SPR	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	Specifies AC counter mode (AM), increment/decrement mode (I/D1-0), high-speed write mode (HWM).	0	Note2		
R06h	Compare Resister	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Specifies the compare resister (CP15-0).	0			
R07h	Display control	0	1	0	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	B/W	REV	DI	D0	Specifies display on (DI-0), black-and-white reversed display (REV), pixel on/off mode (ALB), screen division driving (SPT) and vertical scroll.(VLE2-1)	0		
R08h	Frame frequency control	0	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Specifies the line retrace period (RTN3-0) and operating clock frequency division ratio (DIV1-0).	0			
R0Ch	Power control 2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	Sets the adjustment factor for the Vci voltage (VC2-0).	0			
R11h	Vertical scroll control	0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Sets the 1 st screen display start raster-row (VL17-10) and 2 nd screen display start raster-row (VL27-20).	0			
R14h	1 st screen driving position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	Sets the 1 st screen driving start position (SS17-10) and 1 st screen driving end position (SE17-10).	0			
R15h	2 nd screen driving position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	Sets 2 nd screen driving start position (SS27-20) and 2 nd screen driving end position (SE27-20).	0			
R16h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	Sets start (HSA7-0) and end (HEA7-0) of the horizontal RAM address range.	0			
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets start (VSA7-0) and end (VEA7-0) of the vertical RAM address range.	0			
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15-0) at RAM write.	0			

Instruction List (cont.)

Reg. No.	Register Name	R/W	RS	Upper Code								Lower Code								Description	Execution Cycle		
				DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0				
R21h	RAM address set	0	1																	AD15-8 (upper)	AD6-0 (lower)	Initially set the RAM address to the address counter (AC).	0
R22	RAM data write	0	1																	Write data (upper)	Write data (lower)	Writes data to the RAM.	0
	RAM data read	1	1																	Read data (upper)	Read data (lower)	Reads data from the RAM.	0
R30h	Grayscale palette control (1)	0	1	0	0	PK15	PK14	PK13	PK12	PK11	PK10	0	0	PK05	PK04	PK03	PK02	PK01	PK00	Specifies the grayscale palette.	0		
R31h	Grayscale palette control (2)	0	1	0	0	PK35	PK34	PK33	PK32	PK31	PK30	0	0	PK25	PK24	PK23	PK22	PK21	PK20	Specifies the grayscale palette.	0		
R32h	Grayscale palette control (3)	0	1	0	0	PK55	PK54	PK53	PK52	PK51	PK50	0	0	PK45	PK44	PK43	PK42	PK41	PK40	Specifies the grayscale palette.	0		
R33h	Grayscale palette control (4)	0	1	0	0	PK75	PK74	PK73	PK72	PK71	PK70	0	0	PK65	PK64	PK63	PK62	PK61	PK60	Specifies the grayscale palette.	0		
R34h	Grayscale palette control (5)	0	1	0	0	PK95	PK94	PK93	PK92	PK91	PK90	0	0	PK85	PK84	PK83	PK82	PK81	PK80	Specifies the grayscale palette.	0		
R35h	Grayscale palette control (6)	0	1	0	0	PK115	PK114	PK113	PK112	PK111	PK110	0	0	PK105	PK104	PK103	PK102	PK101	PK100	Specifies the grayscale palette.	0		
R36h	Grayscale palette control (7)	0	1	0	0	PK135	PK134	PK133	PK132	PK131	PK130	0	0	PK125	PK124	PK123	PK122	PK121	PK120	Specifies the grayscale palette.	0		
R37h	Grayscale palette control (8)	0	1	0	0	PK155	PK154	PK153	PK152	PK151	PK150	0	0	PK145	PK144	PK143	PK142	PK141	PK140	Specifies the grayscale palette.	0		
R38h	Grayscale palette control (9)	0	1	0	0	PK175	PK174	PK173	PK172	PK171	PK170	0	0	PK165	PK164	PK163	PK162	PK161	PK160	Specifies the grayscale palette.	0		
R39h	Grayscale palette control (10)	0	1	0	0	PK195	PK194	PK193	PK192	PK191	PK190	0	0	PK185	PK184	PK183	PK182	PK181	PK180	Specifies the grayscale palette.	0		
R3Ah	Grayscale palette control (11)	0	1	0	0	PK215	PK214	PK213	PK212	PK211	PK210	0	0	PK205	PK204	PK203	PK202	PK201	PK200	Specifies the grayscale palette.	0		
R3Bh	Grayscale palette control (12)	0	1	0	0	PK235	PK234	PK233	PK232	PK231	PK230	0	0	PK225	PK224	PK223	PK222	PK221	PK220	Specifies the grayscale palette.	0		
R3Ch	Grayscale palette control (13)	0	1	0	0	PK255	PK254	PK253	PK252	PK251	PK250	0	0	PK245	PK244	PK243	PK242	PK241	PK240	Specifies the grayscale palette.	0		
R3Dh	Grayscale palette control (14)	0	1	0	0	PK275	PK274	PK273	PK272	PK271	PK270	0	0	PK265	PK264	PK263	PK262	PK261	PK260	Specifies the grayscale palette.	0		
R3Eh	Grayscale palette control (15)	0	1	0	0	PK295	PK294	PK293	PK292	PK291	PK290	0	0	PK285	PK284	PK283	PK282	PK281	PK280	Specifies the grayscale palette.	0		
R3Fh	Grayscale palette control (16)	0	1	0	0	PK315	PK314	PK313	PK312	PK311	PK310	0	0	PK305	PK304	PK303	PK302	PK301	PK300	Specifies the grayscale palette.	0		

Note: 1. “*” means doesn’t matter.
 2. High-speed write mode is available only for the RAM writing.

Reset Function

The HD66766R is internally initialized by RESET input. Reset the gate driver/Power supply IC as its settings are not automatically reinitialized when the HD66766R is reset. The reset input must be held for at least 200 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4-0 = "10101", SGS = "0", CMS = "0")
3. B-pattern waveform AC drive (B/C = "0", EOR = "0", NW5-0 = "000000")
4. Power control 1 (DC2-0 = "000", AP1-0 = "00": LCD power off, STB = "0": Standby mode off, SLP = "0", BS2-0 = "000", BT2-0 = "000")
5. Contrast control (Weak contrast VR3-0 = "0000", CT6-0 = "0000000")
6. Entry mode set (SPR= "0" , HWM = "0", I/D1-0 = "11": Increment by 1, AM = "0": Horizontal move, LG2-0="000":Replace mode)
7. Compare resistor : (CP15-0 = "0000000000000000")
8. Display control (VLE2-1 = "00": No vertical scroll, SPT = "0", REV = "0", D1-0 = "00": Display off)
9. Frame cycle control (DIV1-0 = "00": 1-divided clock, RTN3-0: No line retrace period)
10. Power control 2 (VC2-0 = "000")
11. Vertical scroll (VL27-20 = "00000000", VL17-10 = "00000000")
12. 1st screen division (SE17-10 = "11111111", SS17-10 = "00000000")
13. 2nd screen division (SE27-20 = "11111111", SS27-20 = "00000000")
14. Horizontal RAM address position (HEA7-0 = "10000011", HSA7-0 = "00000000")
15. Vertical RAM address position (VEA7-0 = "10101111", VSA7-0 = "00000000")
16. RAM write data mask (WM11-0 = "000"H: No mask)
17. RAM address set (AD15-0 = "0000"H)
18. Grayscale Palette
(PK0 = "000000", RK1= "000011", PK2= "000110", PK3= "001000" ,
PK4= "001010", PK5= "001100", PK6= "001110", PK7= "001111",
PK8= "010000", PK9= "010001", PK10= "010010", PK11= "010011",
PK12= "010100", PK13= "010101", PK14= "010110", PK15= "010111",
PK16= "011000", PK17= "011001", PK18= "011010", PK19= "011011",
PK20= "011100", PK21= "011101", PK22= "011110", PK23= "100000",
PK24= "100010", PK25= "100100", PK26= "100110", PK27= "101000",
PK28= "101011", PK29= "101110", PK30= "110001", PK31= "110100",)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = "00").

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Output GND level
2. Oscillator output pin (OSC2): Output oscillation signal

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the “GND”/“GND”/“GND” level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the “GND”/“Vcc”/“GND” level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

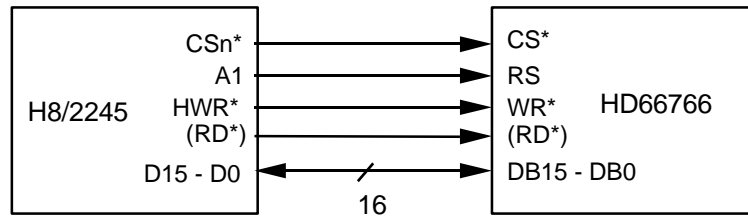


Figure 26 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the “GND”/“GND”/“Vcc” level allows 68-system E-clock-synchronized 8-bit parallel data transfer using DB15–DB8 pins. Setting the IM2/1/0 to the “GND”/“Vcc”/“Vcc” level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the “Vcc” or “GND” level. Note that the upper bytes must also be written when the index register is written to.

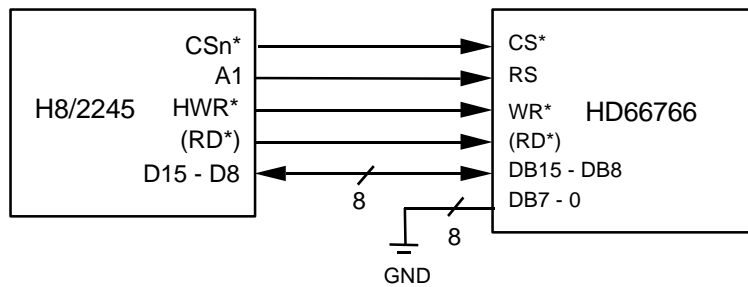


Figure 27 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface

The HD66766R supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a "00"H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system

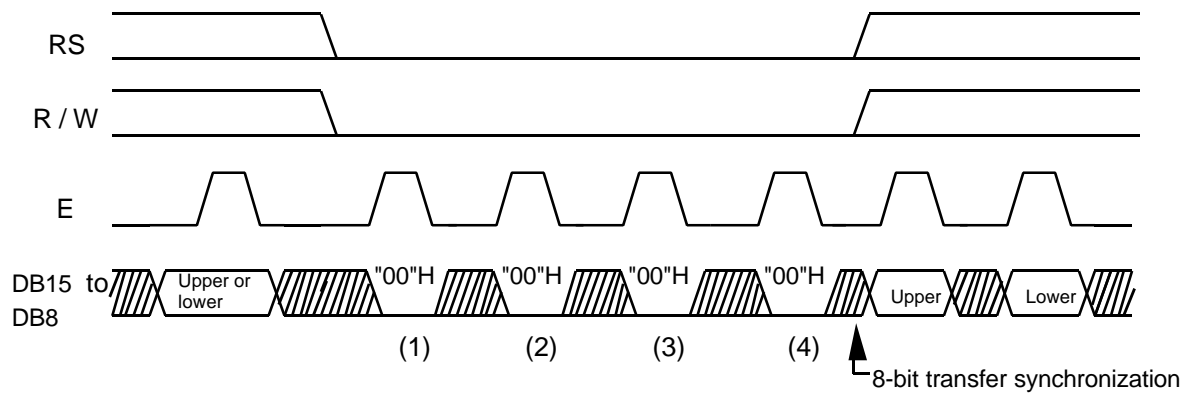


Figure 28 8-bit Transfer Synchronization

Serial Data Transfer

Setting the IM2 pin to the “Vcc” level and the IM1 pin to the “GND” level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data line (SDI), and serial output data line (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins which are not used must be fixed at “Vcc” or “GND”.

The HD66766R initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66766R is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66766R. The HD66766R, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be “01110”. Two different chip addresses must be assigned to a single HD66766R because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = “0”, data can be written to the index register or status can be read, and when RS = “1”, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is “0”, and is transmitted when the R/W bit is “1”.

After receiving the start byte, the HD66766R receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66766R instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Five bytes of RAM read data after the start byte are invalid. The HD66766R starts to read correct RAM data from the sixth byte.

Table 28 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The IM0/ID pin selects ID bit.

Table 29 RS and R/W Bit Function

RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads RAM data

a) Timing of basic data-transfer through clock synchronized serial interface

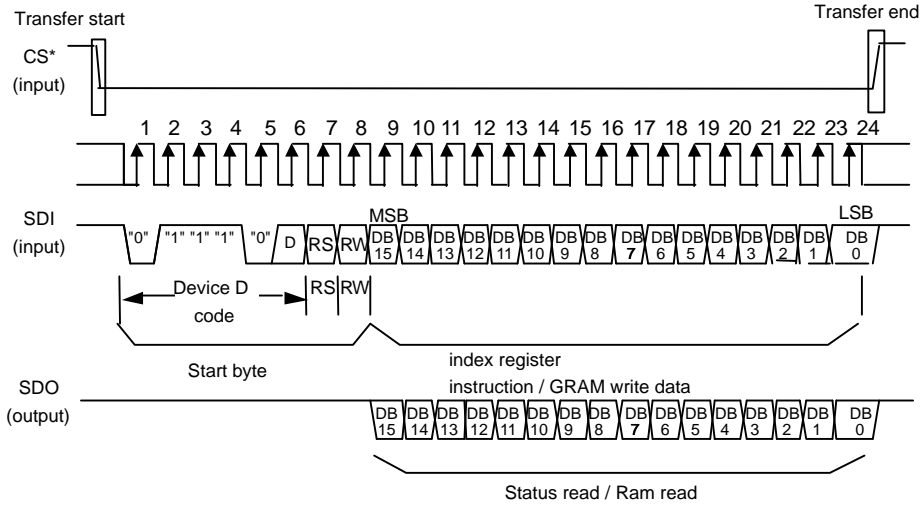


Figure 29 Procedure for transfer through the clock synchronized serial inface (a)

b) Timing of consecutive data transfer through clock synchronized serial interface

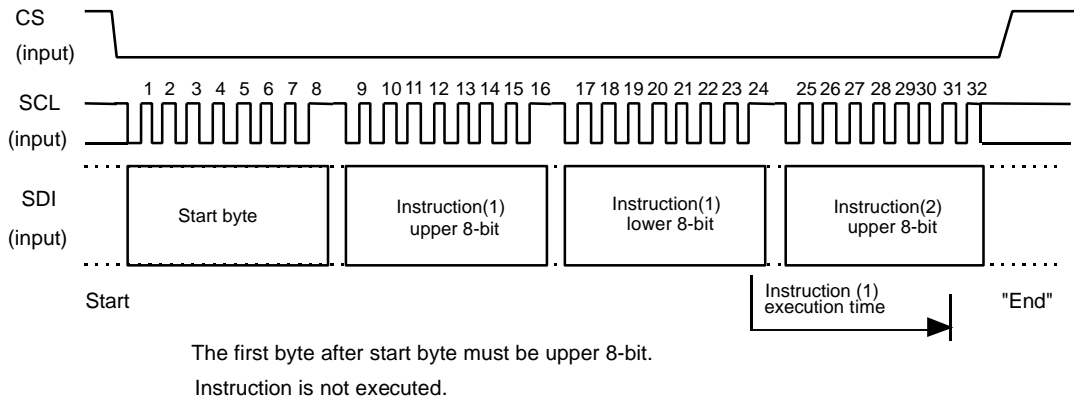


Figure 30 Procedure for transfer through the clock synchronized serial interface (b)

C) Transfer data read from GRAM

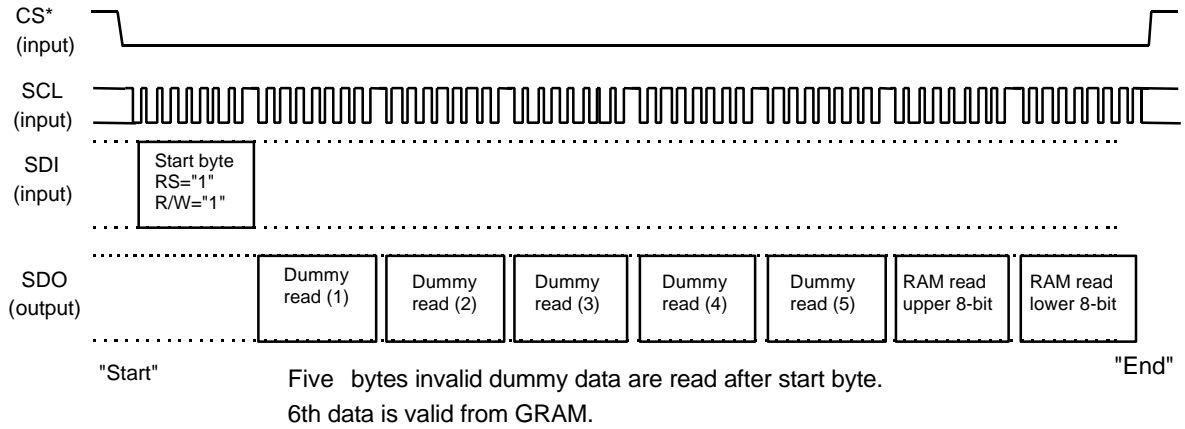


Figure 31 Procedure for transfer through the clock synchronized serial interface (c)

d) Status Read / Instruction Read

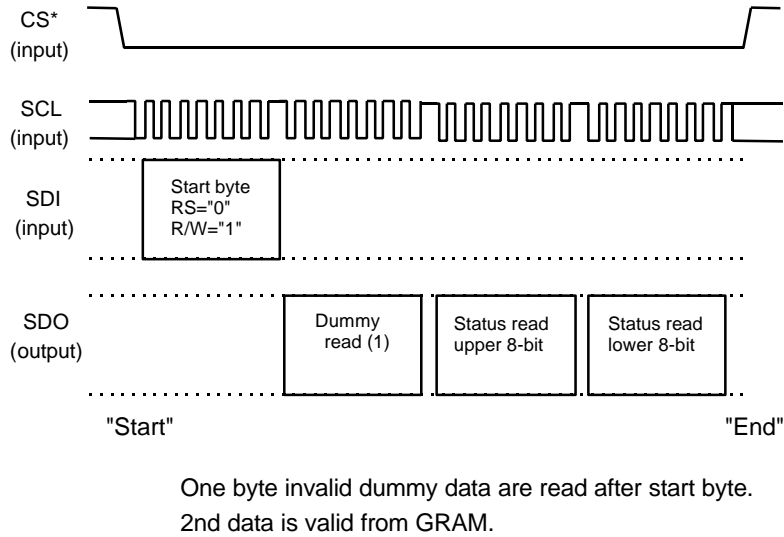


Figure 32 Procedure for transfer through the clock synchronized serial interface (d)

High-Speed Burst RAM Write Function

The HD66766R has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications that require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66766R internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

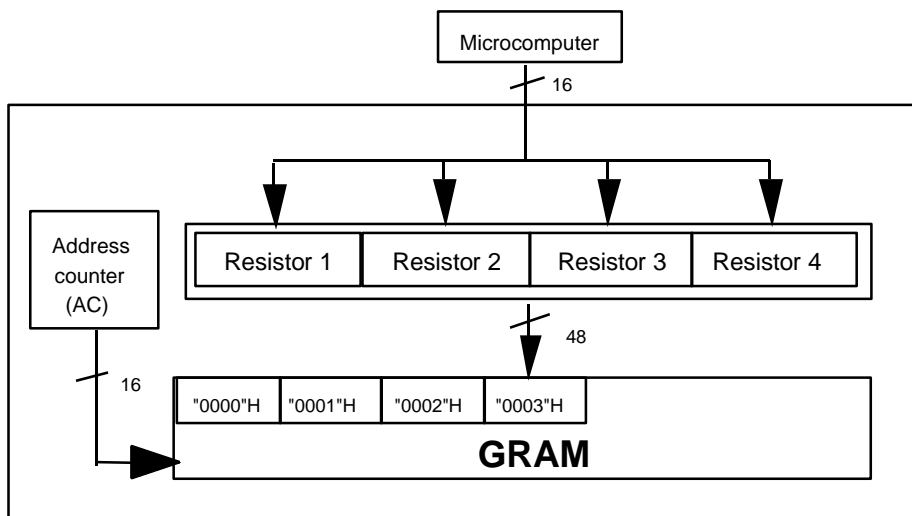
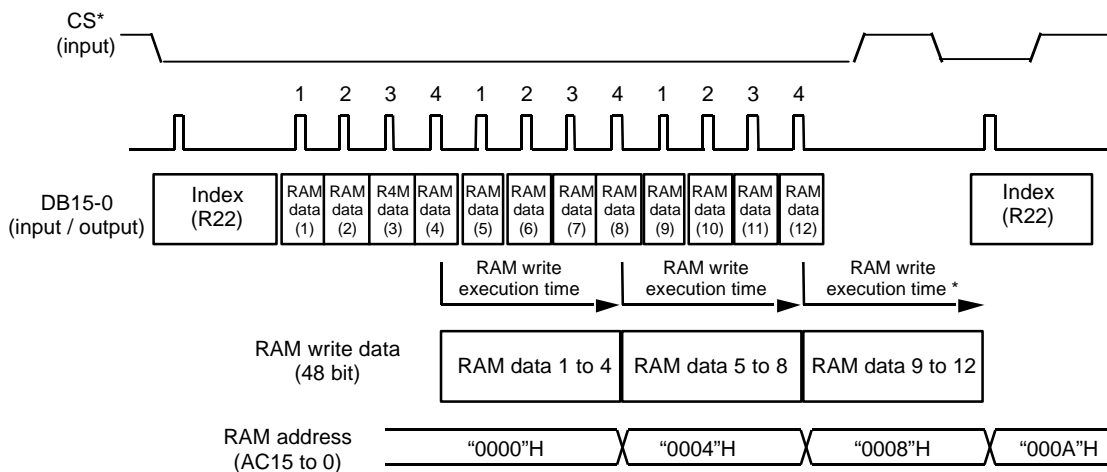


Figure 33 Flow of Operation in High-Speed Consecutive Writing to RAM



* The lower two bits of the address must be set in the following way in high-speed write mode.
 When D0 becomes 0, the lower two bits of the address must be set to "11".
 When D1 becomes 1, the lower two bits of the address must be set to "00".

Note: When a high-speed RAM write is canceled, the next instruction must only be executed after the RAM write execution time has elapsed.

Figure 34 Example of the Operation of High-Speed Consecutive Writing to RAM

Note the following when using high-speed RAM write mode.

- Notes:
1. The logical and compare operation cannot be used.
 2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.
 - *When I/D0=0, the lower two bits in the address must be set to “11” and be written to RAM.
 - *When I/D0=1, the lower two bits in the address must be set to “00” and be written to RAM.
 3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.
 4. When the index register and RAM data write (“22”H) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to “0” while RAM is being read.
 5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
 6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 30 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	High-Speed RAM Write (HWM=1)
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Can be set by four words

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). The number of dummy write operations of a row must be 4N.

Table 31 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

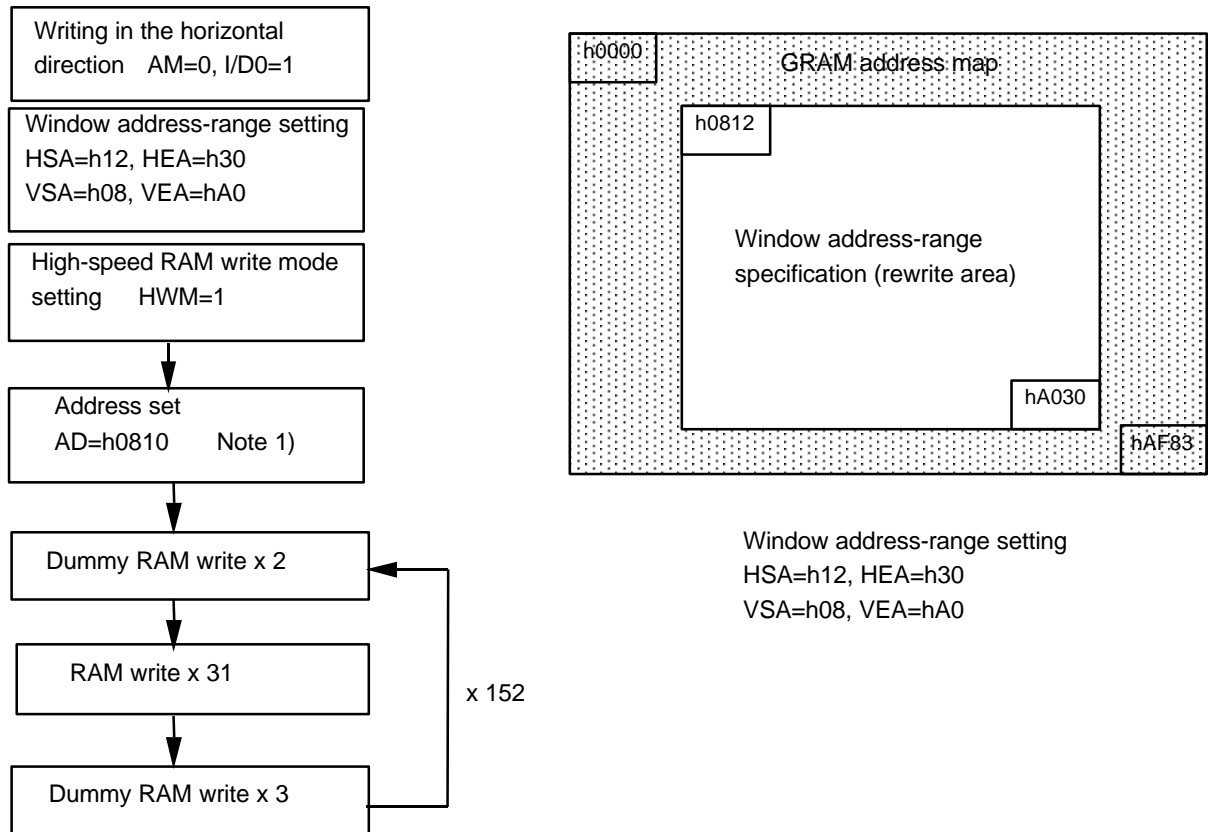
HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

Table 32 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of 4 x N operations, including the dummy writes.
 Horizontal access count = first dummy write count + write data count + last dummy write count = 4 x N

An example of high-speed RAM write with a window address-range specified is shown below. The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0= "10", HEA1 to 0= "00").



Note1) The address set for the high-speed RAM write must be 00 or 11 according to the value of I/D0 bit. Only RAM in the specified window address-range will be overwritten.

Figure 35 Example of the High-Speed RAM write with a window address-range specification

Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]

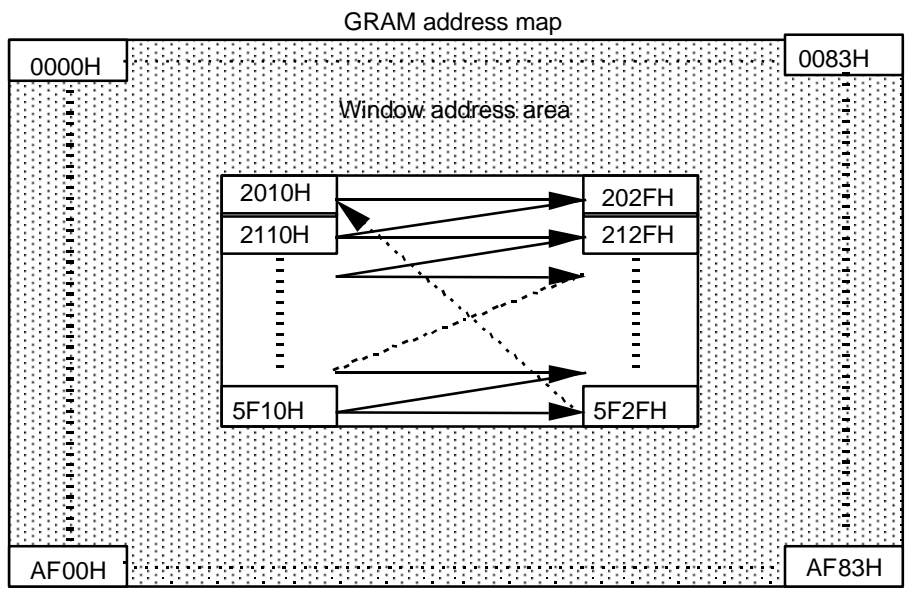
(horizontal direction) "00"H ≤ HSA7-0 ≤ HEA7-0 ≤ "83"H
 (vertical direction) "00"H ≤ VSA7-0 ≤ VEA7-0 ≤ "AF"H

[Restriction on address settings during the window address]

(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0
 VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.

ID0=0: The lower two bits of the address must be set to "11".
 ID0=1: The lower two bits of the address must be set to "00"



Window address-range specification area
 HSA5-0=10H, HSE5-0=2FH I/D0=1 (increment)
 VSA7-0=20H, VEA7-0=5FH AM=0 (horizontal writing)

Figure 36 Example of Address Operation in the Window Address Specification

Graphic Operation Function

The HD66766R can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A conditional write function that compares the write data and compare-bit data and writes the data sent from the microcomputer only when the conditions match. Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode register. The bit set value of the RAM-write –data mask register, and the write from the microcomputer.

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG2-0	
Write mode 1	0 /1	0	000	Horizontal data replacement, horizontal - border drawing
Write mode 2	0 /1	1	000	Vertical data replacement, vertical - border drawing
Write mode 3	0 /1	0	110,111	Conditional horizontal data replacement, horizontal - border drawing
Write mode 4	0 /1	1	110,111	Conditional vertical data replacement, vertical - border drawing

Table 33 Graphics operation

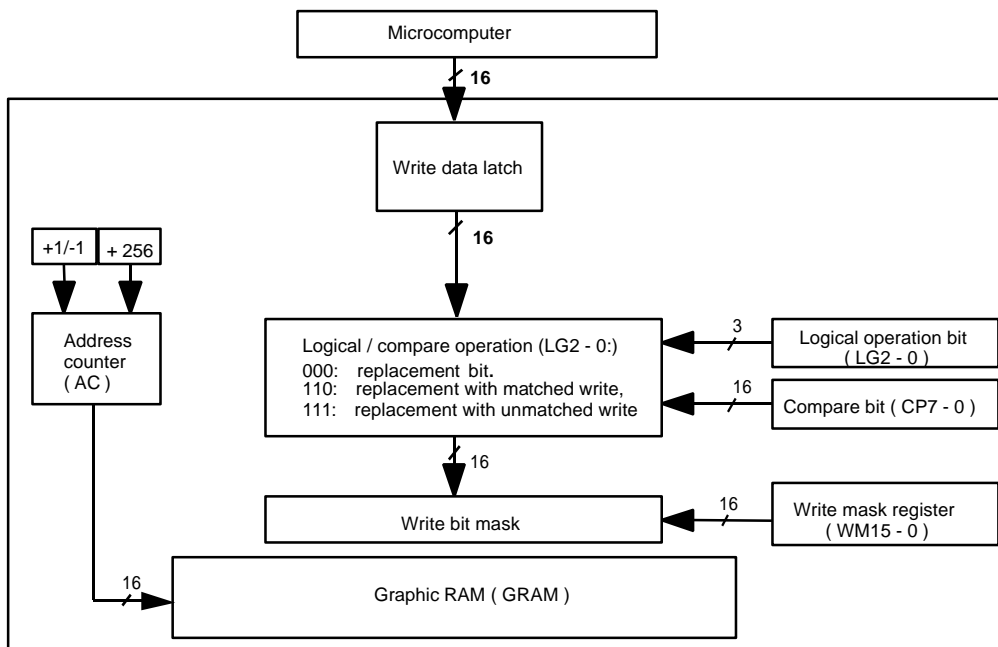


Figure 37 Graphics Operation flow

Write-data Mask Function

The HD66766R has a bit-wise write-data mask function that controls writing the 16-bit data from the microcomputer to the GRAM. Bits that are “0” in the write-data mask register (WM15–0) cause the corresponding DB bit to be written to the GRAM. Bits that are “1” prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

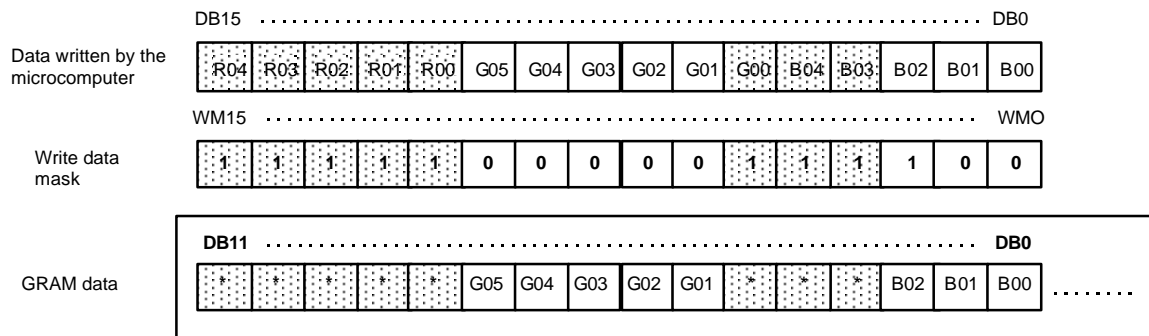


Figure 38 Write-data Mask Function Operation

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2-0 = "000"

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster below after it has reached the left or right edge of the GRAM.

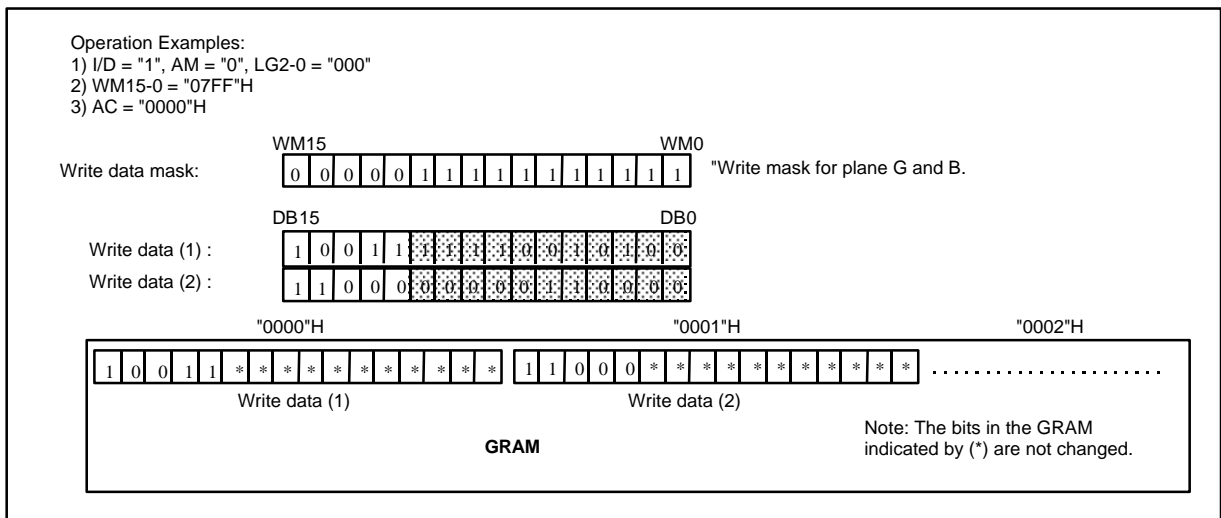


Figure 39 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2-0 = "000"

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM15-0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

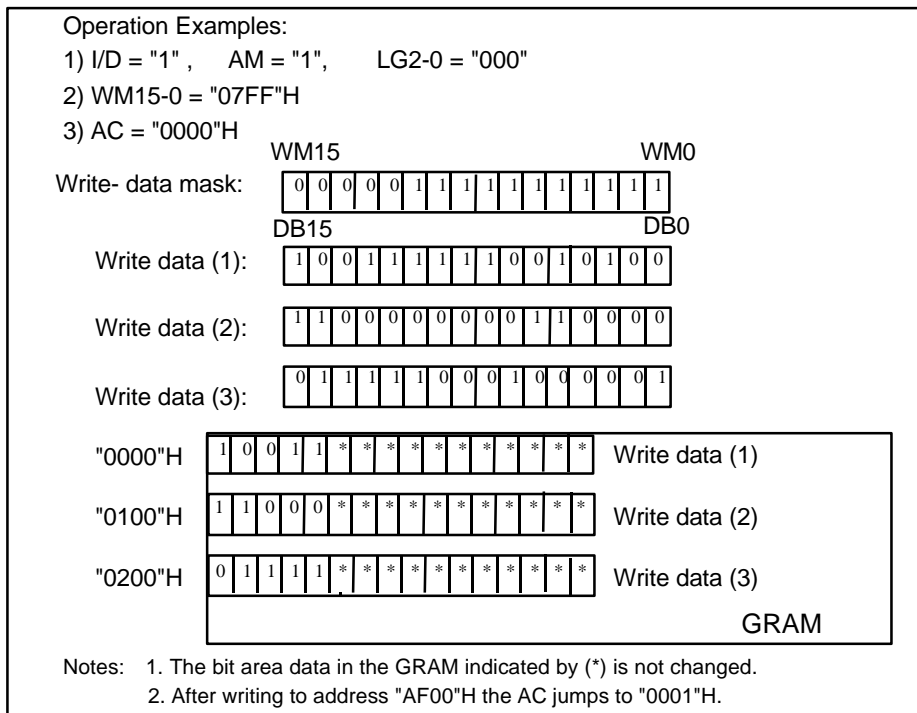


Figure 40 Operation of Write Mode 2

3. Write mode 3: AM = 0, LG2-0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP7-0). When the result of the comparison in a byte unit satisfies the condition write-data mask function (WM15-0) are also enabled. After writing , the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

Operation Examples:

- 1) I/D = "1", AM = "0", LG2-0 = "110" (Matched write)
- 2) CP15-0 = "2860"H
- 2) WM15-0 = "0000"H
- 3) AC = "0000"H

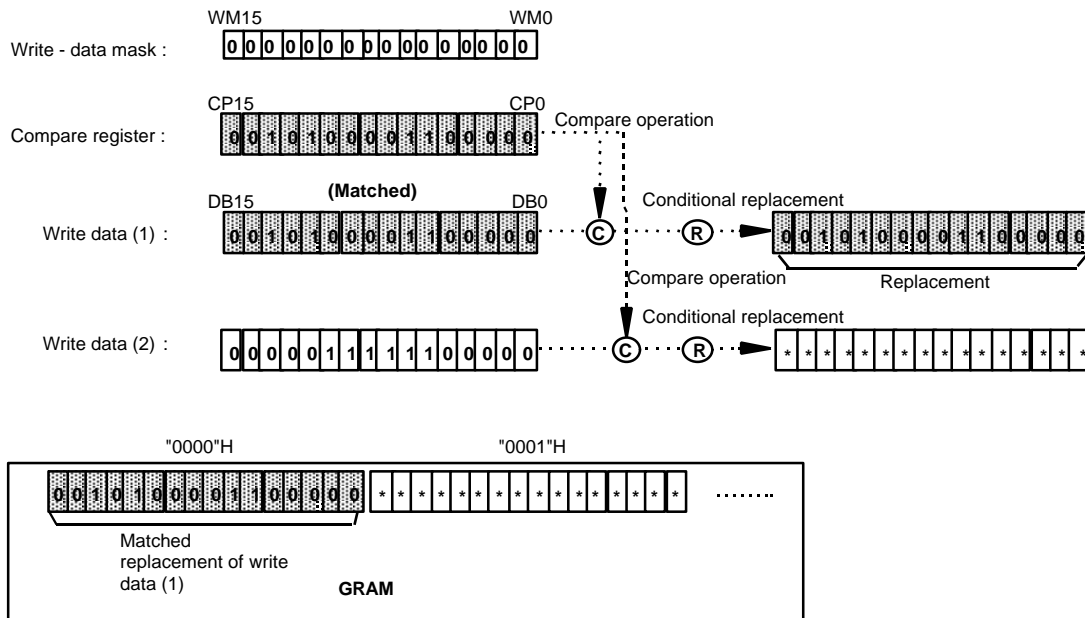


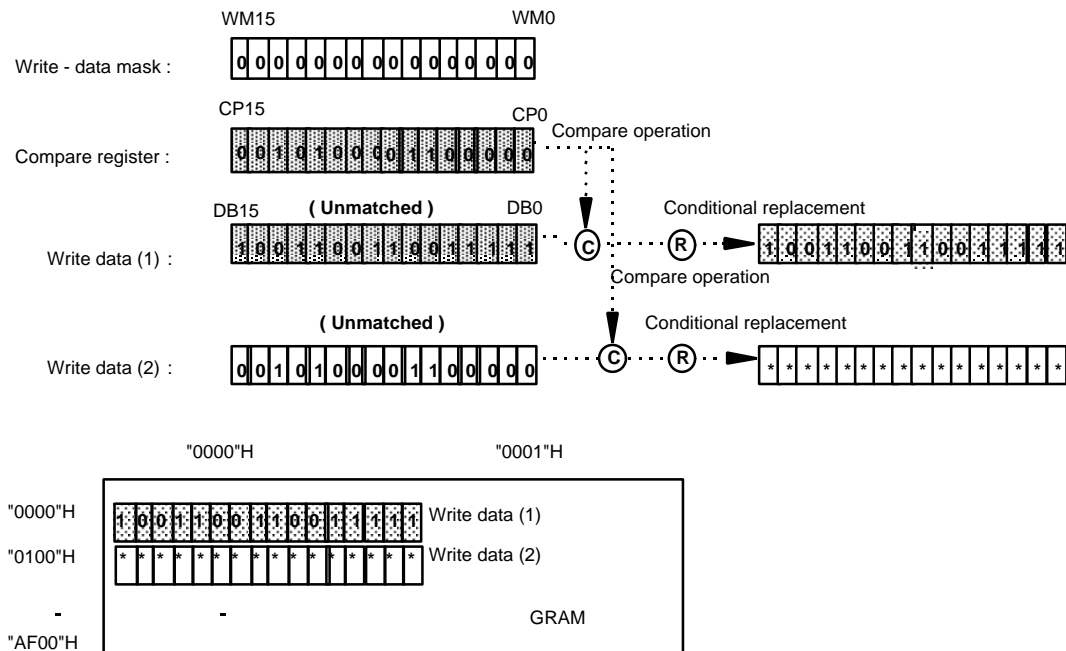
Figure 41 Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2-0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP15-0) to write the data . When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, write data mask function (WM15-0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

- 1) I/D = "1", AM = "1", LG2-0 = "111" (Unmatched write)
- 2) WM15-0 = "0000"H
- 2) CP15-0 = "2860"H
- 3) AC = "0000"H



- Notes: 1. The bit area data in the GRAM indicated by (*) is not changed.
- 2. After writing to address "AF00"H the AC jumps to "0001"H.

Figure 42 Writing Operation of Write Mode 4

4096 colors Display Function

HD66766R is equipped with 4096 colors display function. When setting SPR bit = 1, it operates 4096 color display function, and uses 16 bits instead of 12 bits. Upper 4 bits are invalid when operating 4096 colors display function. While operating 4096 colors display function, write mode 3 and 4 in graphic operation are not usable.

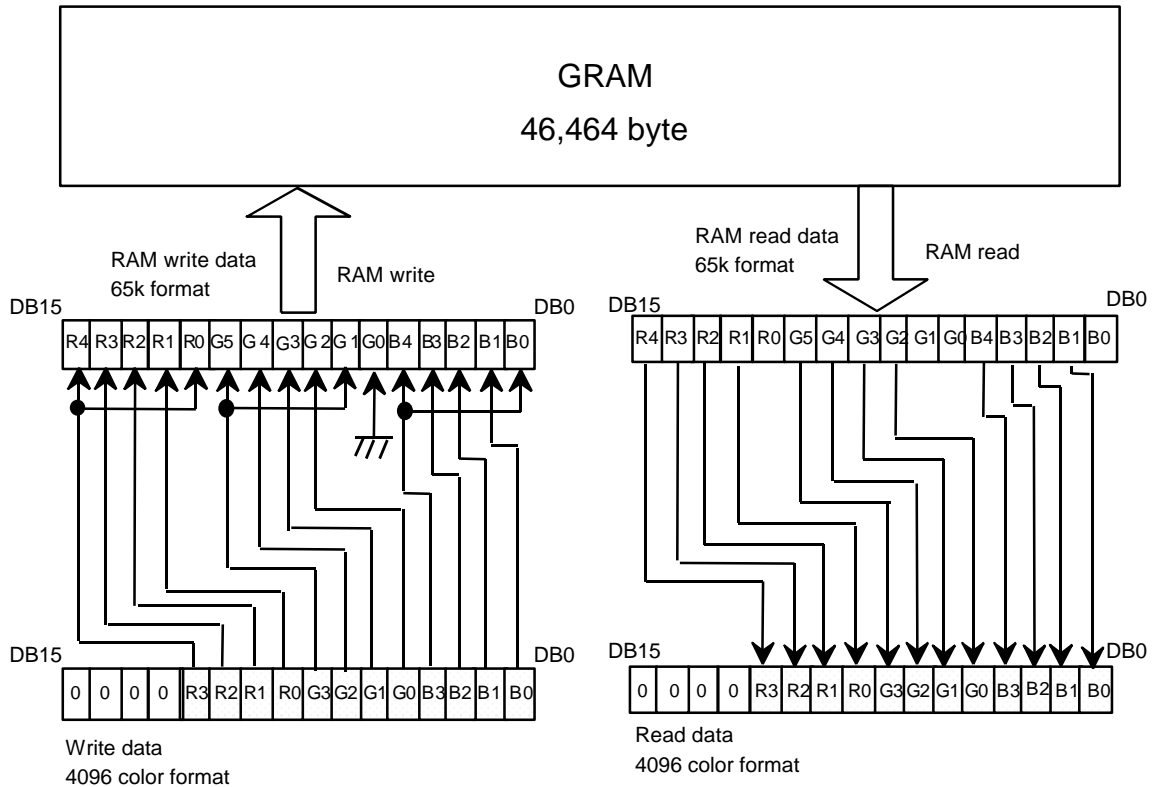


Figure 43 4096 color display data write and read format

Table 34 4,096 color R, G, B data and selective grayscale palette

R, G, B data	Selective grayscale palette	R, G, B data	Selective grayscale palette
0000	PK0	1000	PK17
0001	PK2	1001	PK19
0010	PK4	1010	PK21
0011	PK6	1011	PK23
0100	PK8	1100	PK25
0101	PK10	1101	PK27
0110	PK12	1110	PK29
0111	PK14	1111	K31

Grayscale Palette

The HD66766R incorporates a grayscale palette to simultaneously display 65K of the 140,608 possible colors. The grayscales consist of 32 6-bit palettes. The 52-stage grayscale levels can be selected from the 6-bit palette data.

For the display data, the four-bit data in the GRAM written from the microcomputer is used.

In this palette, a pulse-width control system (PWM) is used to eliminate flicker in the LCD display. The time over which the LCDs are switched on is adjusted according to the level and grayscales are displayed so that flicker is reduced and grayscales are clearly displayed.

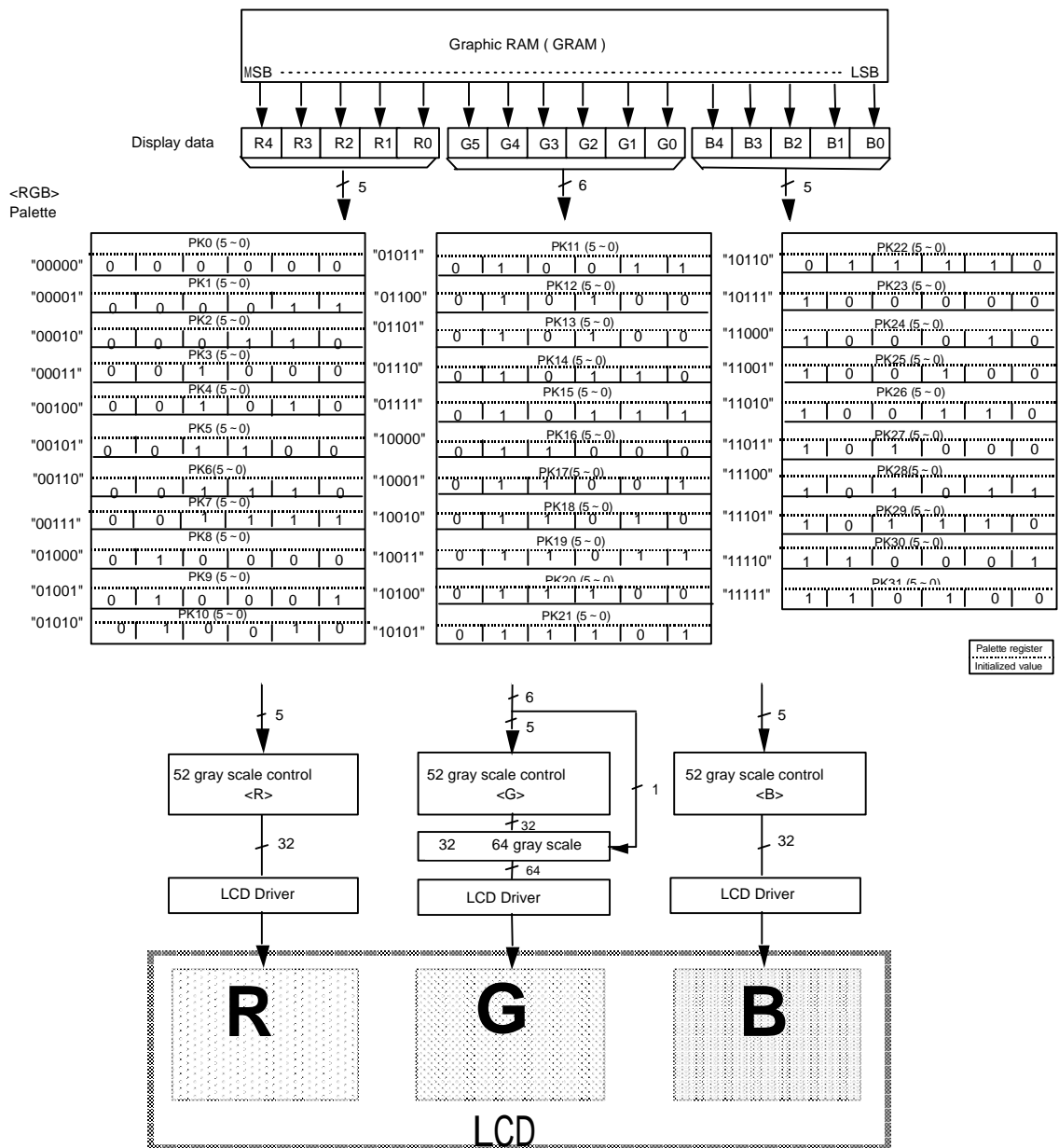


Figure 44 Grayscale Palette Control

Grayscale Palette Table

The grayscale register that is set for each palette register (PK) can be set to any level. 52-grayscale lighting levels can be set according to palette values (“000000” to “110100”).

Table 35 Grayscale Control Level

Palette Register Value (PK)						Grayscale Control Level
0	0	0	0	0	0	Unlit level* ¹
0	0	0	0	0	1	1/52level
0	0	0	0	1	0	2/52level
0	0	0	0	1	1	3/52level
0	0	0	1	0	0	4/52level
0	0	0	1	0	1	5/52level
0	0	0	1	1	0	6/52level
0	0	0	1	1	1	7/52level
0	0	1	0	0	0	8/52level
0	0	1	0	0	1	9/52level
0	0	1	0	1	0	10/52level
0	0	1	0	1	1	11/52level
0	0	1	1	0	0	12/52level
0	0	1	1	0	1	13/52level
0	0	1	1	1	0	14/52level
0	0	1	1	1	1	15/52level
0	1	0	0	0	0	16/52level
0	1	0	0	0	1	17/52level
0	1	0	0	1	0	18/52level
0	1	0	0	1	1	19/52level
0	1	0	1	0	0	20/52level
0	1	0	1	0	1	21/52level
0	1	0	1	1	0	22/52level
0	1	0	1	1	1	23/52level
0	1	1	0	0	0	24/52level
0	1	1	0	0	1	25/52level
0	1	1	0	1	0	26/52level
0	1	1	0	1	1	27/52level
0	1	1	1	0	0	28/52level
0	1	1	1	0	1	29/52level
0	1	1	1	1	0	30/52level
0	1	1	1	1	1	31/52level
1	0	0	0	0	0	32/52level

→ Next Page continued

1	0	0	0	0	1	33/52level
1	0	0	0	1	0	34/52level
1	0	0	0	1	1	35/52level
1	0	0	1	0	0	36/52level
1	0	0	1	0	1	37/52level
1	0	0	1	1	0	38/52level
1	0	0	1	1	1	39/52level
1	0	1	0	0	0	40/52level
1	0	1	0	0	1	41/52level
1	0	1	0	1	0	42/52level
1	0	1	0	1	1	43/52level
1	0	1	1	0	0	44/52level
1	0	1	1	0	1	45/52level
1	0	1	1	1	0	46/52level
1	0	1	1	1	1	47/52level
1	1	0	0	0	0	48/52level
1	1	0	0	0	1	49/52level
1	1	0	0	1	0	50/52level
1	1	0	0	1	1	51/52level
1	1	0	1	0	0	All lit level*2

- Notes: 1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.
2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used

RGB pixel data and Grayscale level

Table 36 G pixel data and output level

G pixel data	Output level	G pixel data	Output level
000000	PK0	100000	PK16
000001	(PK0+PK1)/2	100001	(PK16+PK17)/2
000010	PK1	100010	PK17
000011	(PK1+PK2)/2	100011	(PK17+PK18)/2
000100	PK2	100100	PK18
000101	(PK2+PK3)/2	100101	(PK18+PK19)/2
000110	PK3	101100	PK19
0000111	(PK3+PK4)/2	100111	(PK19+PK20)/2
001000	PK4	101000	PK20
001001	(PK4+PK5)/2	101001	(PK20+PK21)/2
001010	PK5	101010	PK21
001011	(PK5+PK6)/2	101011	(PK21+PK22)/2
001100	PK6	101100	PK22
001101	(PK6+PK7)/2	101101	(PK22+PK23)/2
001110	PK7	101110	PK23
001111	(PK7+PK8)/2	101111	(PK23+PK24)/2
010000	PK8	110000	PK24
0100001	(PK8+PK9)/2	110001	(PK24+PK25)/2
010010	PK9	110010	PK25
010011	(PK9+PK10)/2	110011	(PK25+PK26)/2
010100	PK10	110100	PK26
010101	(PK10+PK11)/2	110101	(PK26+PK27)/2
010110	PK11	110110	PK27
010111	(PK11+PK12)/2	110111	(PK27+PK28)/2
011000	PK12	111000	PK28
011001	(PK12+PK13)/2	111001	(PK28+PK29)/2
011010	PK13	111010	PK29
011011	(PK13+PK14)/2	111011	(PK29+PK30)/2
011100	PK14	111100	PK30
011101	(PK14+PK15)/2	111101	(PK30+PK31)/2
011110	PK15	111110	PK31
011111	(PK15+PK16)/2	111111	PK31

Table 37 R, B pixel data and output level

R, B pixel data	Output level	R, B pixel data	Output level
00000	PK0	10000	PK16
00001	PK1	10001	PK17
00010	PK2	10010	PK18
00011	PK3	10011	PK19
00100	PK4	10100	PK20
00101	PK5	10101	PK21
00110	PK6	10110	PK22
00111	PK7	10111	PK23
01000	PK8	11000	PK24
01001	PK9	11001	PK25
01010	PK10	11010	PK26
01011	PK11	11011	PK27
01100	PK12	11100	PK28
01101	PK13	11101	PK29
01110	PK14	11110	PK30
01111	PK15	11111	PK31

Setting flow for low power consumption instruction

Sleep Mode

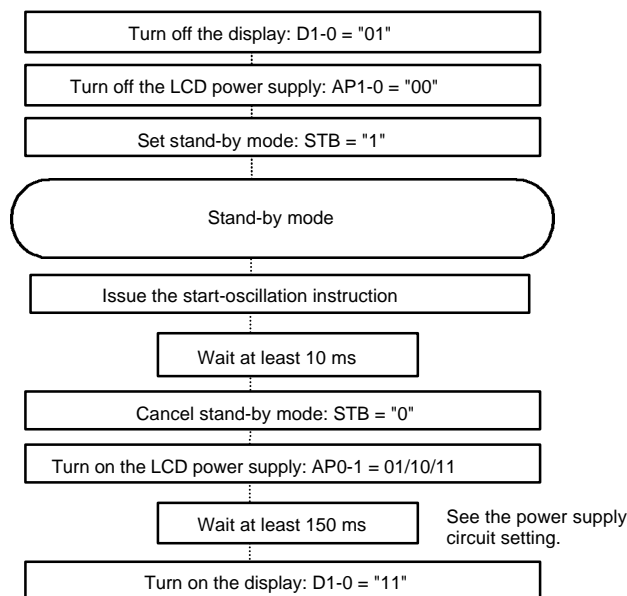
Setting the sleep mode bit (SLP) to “1” puts the HD66766R in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG396) and COM (COM1 to COM176) pins output the “GND” level, resulting in no display. If the AP1-0 bits in the power control register are set to “00” in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 38 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = “1”)	Standby Mode (STB = “1”)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped
Master/slave signal	Operation stopped	Operation stopped

Standby Mode

Setting the standby mode bit (STB) to “1” puts the HD66766R in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG396) and COM (COM1 to COM176) pins for the time-sharing drive output the GND level, resulting in no display. If the AP1-0 bits are set to “00” in the standby mode, the LCD drive power supply can be turned off. During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to “0”. When multi-chips are operated, be sure to be set to the standby mode from the slave level.



Procedure for Setting and Canceling Standby Mode

Figure 45 Procedure for Setting and Canceling Standby Mode

Setting flow for power supply and display instruction

Power-on / off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

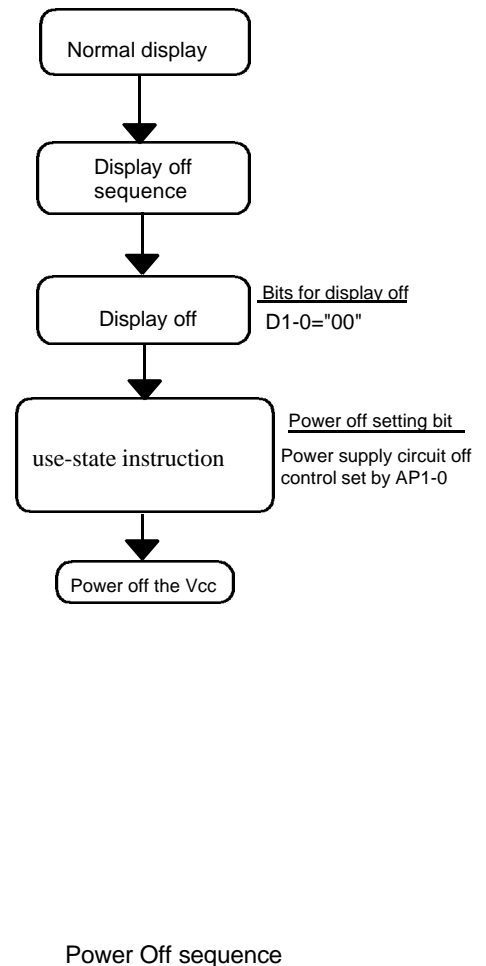
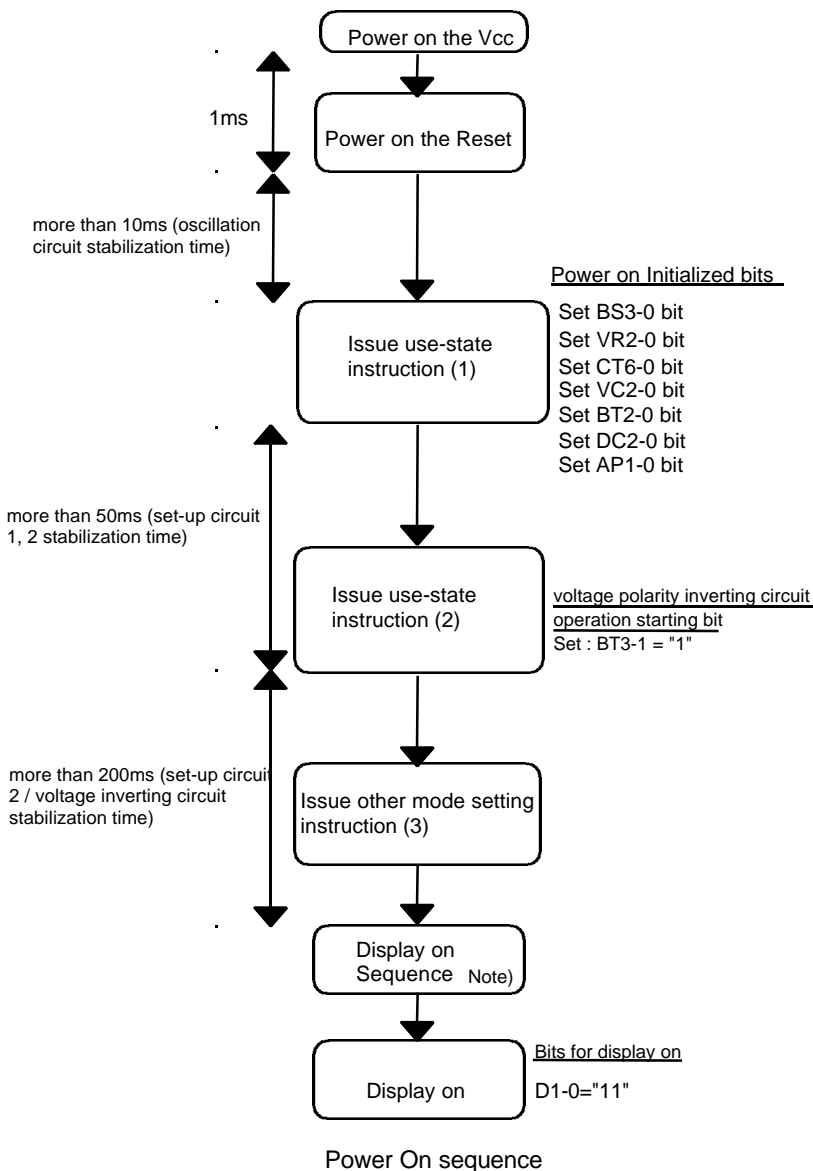
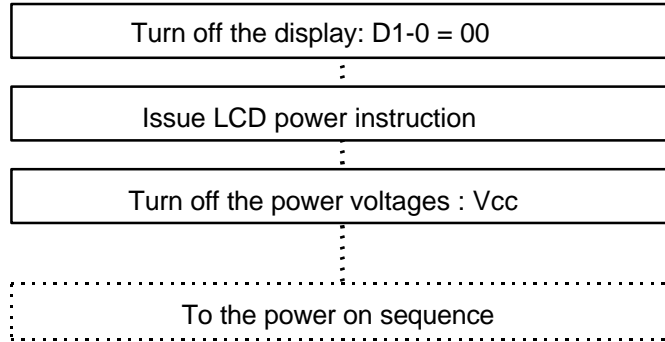


Figure 46 Power-on Sequence

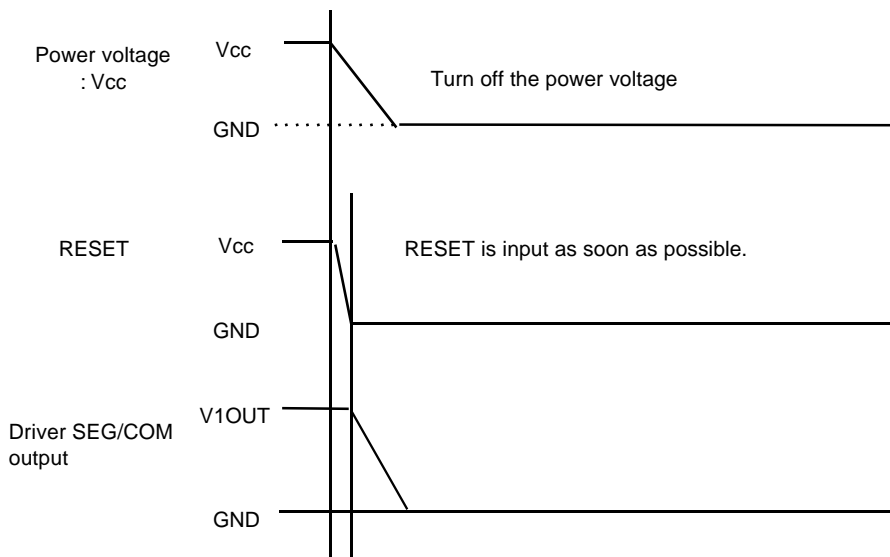
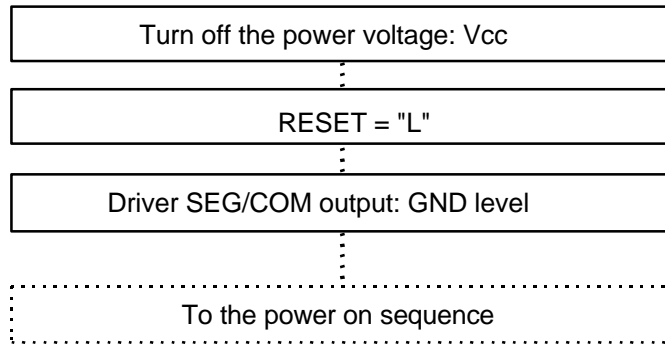
Figure 47 Power-off Sequence

Power-off sequence

Normal case



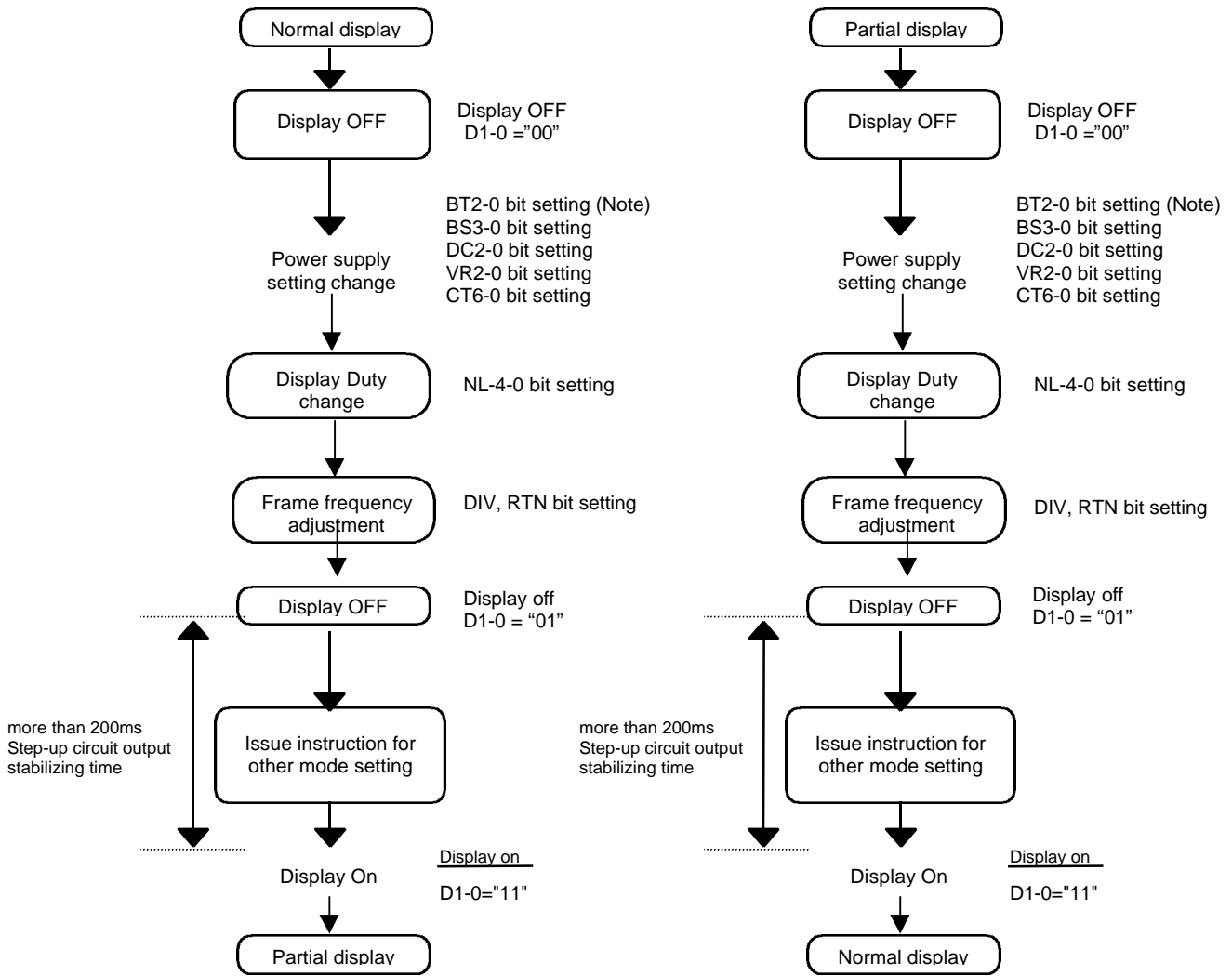
Emergency case



Note: When hardware reset is input during the power-off period, the D1-0 bits are cleared to "00" and SEG/COM output is forcibly lowered to the GND levels.

Figure 48 Power-off sequence

Partial Sequence Setting Flow



Note: Change only BT2-0 with BT3-0 = "1"

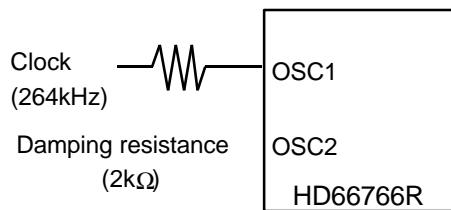
Figure 49 Normal to partial display

Figure 50 Partial to normal display

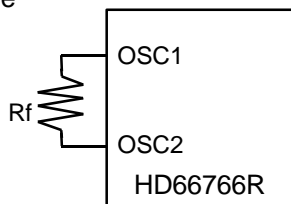
Oscillation Circuit

The HD66766R can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

1) External clock mode



2) External resistance oscillation mode



Note: The resistance must be located near the OSC1/OSC2 pins.

Figure 51 Oscillation Circuits

The relationship between the SEG and COM output levels is as shown in the following figure. While the display is off, SEG and COM outputs go to GND level.

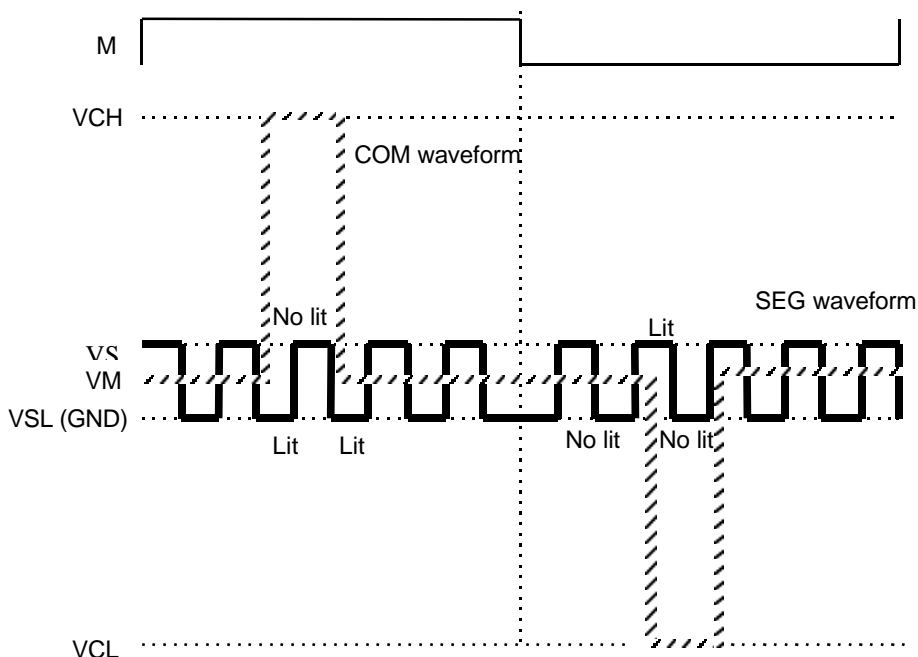


Figure 52 Relationship with SEG/COM Output Level

Frame-Frequency Adjustment Function

The HD66766R has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive as the oscillation frequency is always the same. When the display duty is changed, the frame frequency can be adjusted to be the same. If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the retrace-line period bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)	
Frame frequency =	$\frac{f_{osc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \quad [\text{Hz}]$
<p style="text-align: center;">f_{osc}: R-C oscillation frequency Duty: drive duty (NL bit) Clock cycles per raster-row: (RTN + 26) clock cycles Division ratio: DIV bit</p>	

Example Calculation 1 Setting the maximum frame frequency to 60 Hz

Display duty: 1/176
 Retrace-line period: 0 clock (RTN3-0 = "0000")
 Operation clock division ratio: 1 division

$$f_{osc} = 60 \text{ Hz} \times (0 + 26) \text{ clock} \times 1 \text{ division} \times 176 \text{ lines} = 275 \text{ (kHz)}$$

In this case, the R-C oscillation frequency becomes 275 kHz. The external resistance value of the R-C oscillator must be adjusted to be 275 kHz. The display duty can be changed by the partial display, etc. and the frame frequency can be the same by setting the RNT bit and DIV bit to achieve the following.

(Partial display): Display duty: 1/40
 Retrace-line period: 1 clock (RTN3-0 = "0002")
 Operation clock division ratio: 3 division
 Frame frequency = 275 kHz / ((3 + 26) clock × 4 division × 40 lines) = 59.2 (Hz)

Example Calculation 2 Switching the frame frequency to suit animation/static image display

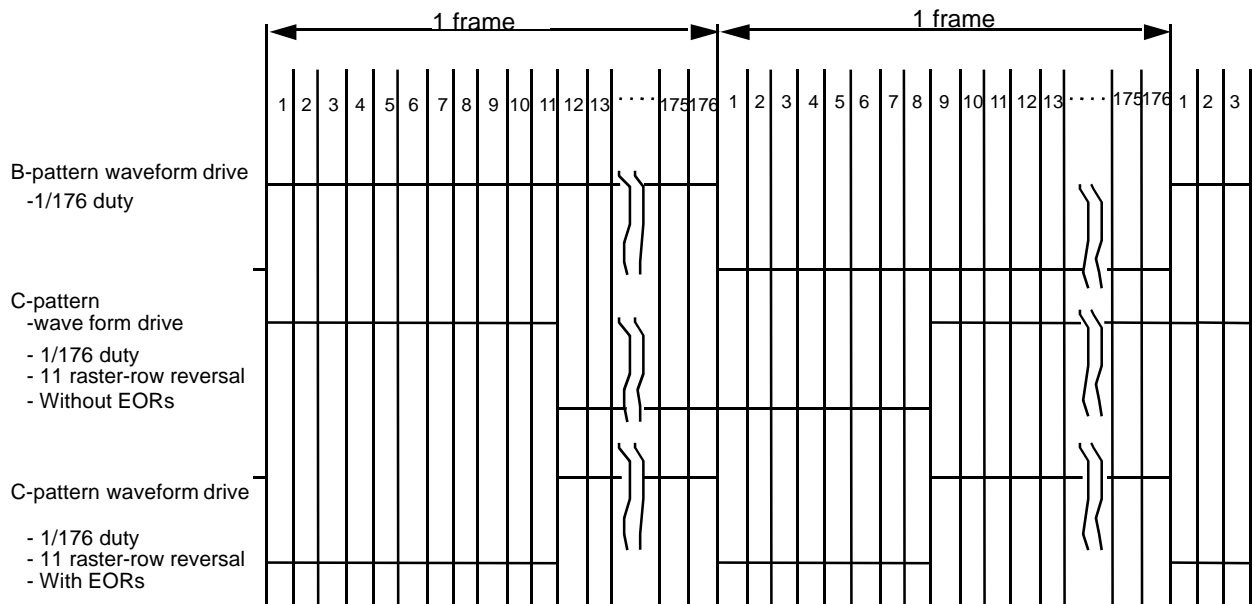
(Animation display): Frame frequency: 90 Hz
 Display duty: 1/176
 Retrace-line period: 0 clock (RTN3-0 = "0000")
 Operation clock division ratio: 1 division
 f_{osc} = 90 Hz × (0 + 26) clock × 1 division × 176 lines = 412 (kHz)

(Static image display): Frame frequency: 90 Hz
 Display duty: 1/176
 Retrace-line period: 1 clock (RTN3-0 = "1101")
 Operation clock division ratio: 1 division
 Frame frequency: 412 kHz / ((13 + 26) clock × 1 division × 176 lines) = 60.0 (Hz)

n-raster-row Reversed AC Drive

The HD66766R supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as cross-talk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



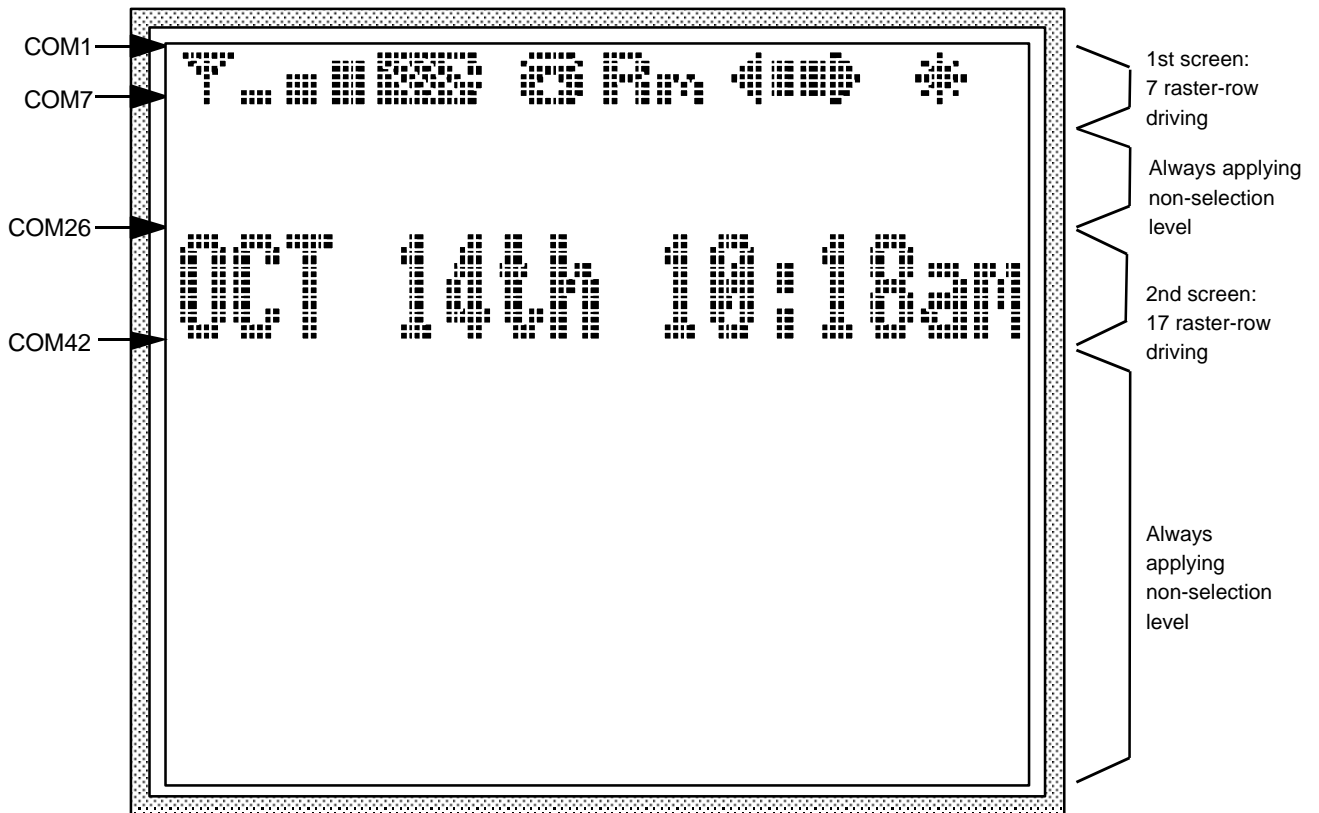
Notice : Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated to the LCD.

Figure 53 Example of an AC Signal under n-raster-row Reversed AC Drive

Screen-division Driving Function

The HD66766R can select and drive two screens at any position with the screen-driving position registers (R14h and R15h). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL4-0), thus reducing LCD-driving voltage and power consumption. For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R14h). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R15h). The 2nd screen control is effective when the SPT bit is "1". The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

1/24 duty driving on 2 screen



- Driving duty: NL4-0 = "00010" (1/24 duty)
- 1st screen setting: SS17-10 = "00"H, SE17-10 = "06" H
- 2nd screen setting: SS27-20 = "19"H, SE27-20 = "29" H, SPT = "1"

Figure 54 Display example in 2-screen division driving

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R14h) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R15h) for the HD66766R. Note that incorrect display may occur if the restrictions are not satisfied.

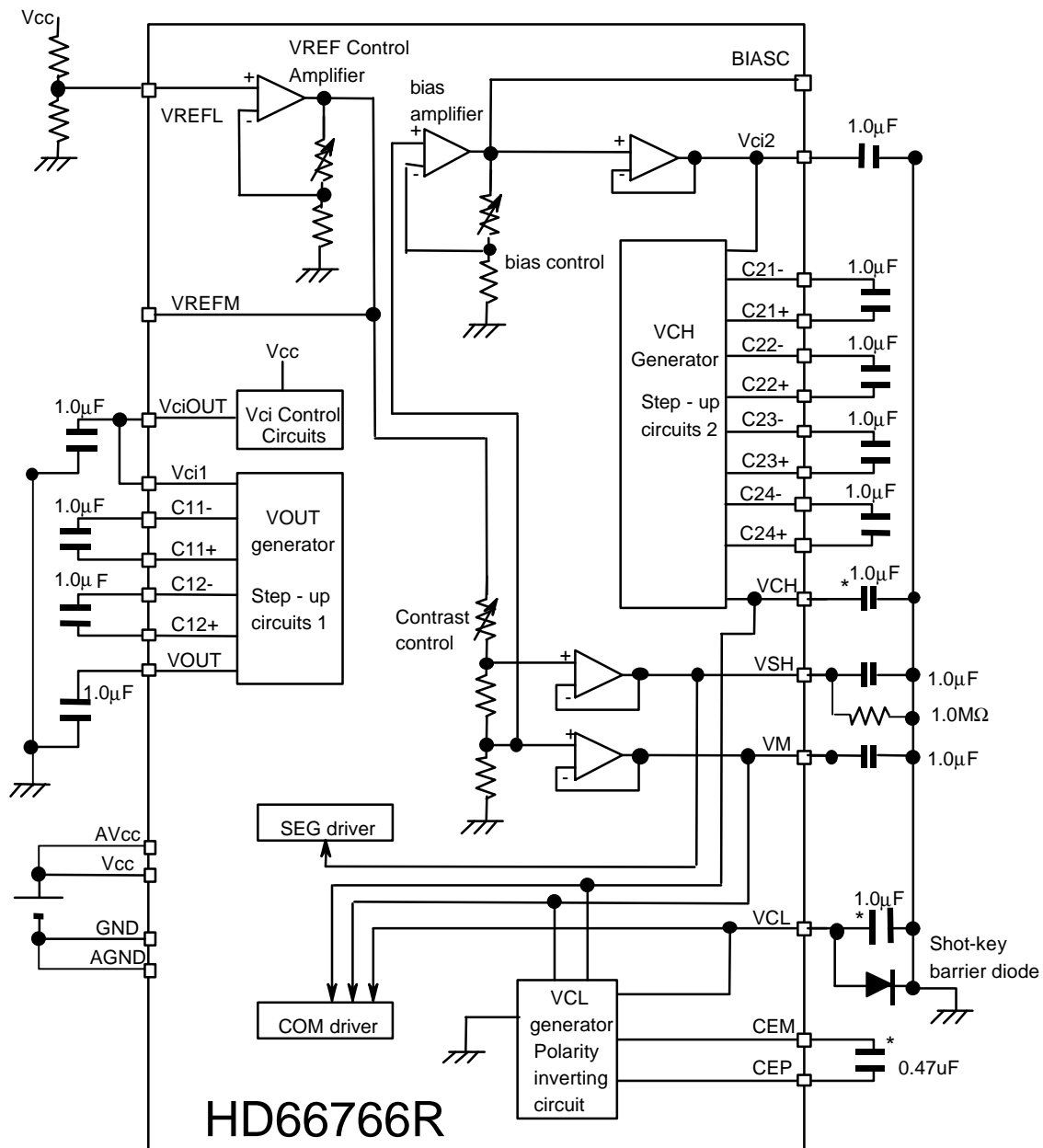
Table 39 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (SPT = 0)	2nd Screen Driving (SPT = 1)
Register setting	$SS17-10 \leq SE17-0 \leq \text{"AF"}H$	$SS17-10 \leq SE17-10 < SS27-20 \leq SE27-20 \leq \text{"AF"}H$
Display operation	<ul style="list-style-type: none"> • Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others 	<ul style="list-style-type: none"> • Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

- Notes:
1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
 2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line and the lines between them are displayed and non-selection level driving is performed for other lines.
 3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.

LCD Voltage Generation Circuit

Figure 58 shows a configuration of the HD66766R LCD drive voltage generation circuit. It consists of step-up circuit 1 that doubles or triples the voltage that is applied to Vci1, step-up circuit 2 that multiplies the voltage from step-up circuit 1 by two to five times, and polarity circuit that generates a VCL level by inverting the VCH level centered around the VM level. These circuits generate VCH and VCL that are power supply for COM outputs. The LCD driving level for SEG outputs (VSH and VM) are generated by dividing resistance at the VREF level.



- Note: 1) Use condenser with character B.
 2) Condensers with asterisk (*) need resist pressure more than 25V.
 3) Insert shot-key barrier diode.
 (VF = 0.6V / 20mA, VR>=30V)

Figure 55 Configuration of internal power circuit

- Notes: 1. Generate an output voltage (VOUT) from step-up circuit 1 within the range from 4.0 to 5.75V.
 2. Do not allow the output voltage (VCH) from step-up circuit 2 to exceed 22 V.
 3. Do not allow the output from Vci2 to exceed VOUT voltage .
 4. When capacitor with polarity is used, be sure that an inverted voltage is not applied to it in any state of the system.
 5. Vci1 is used as both the reference voltage input and power supply in the step-up circuit. Keep sufficient LCD drive current.
 6. Rated voltage of capacitors possible to be used are as described below. Required voltage depends on used panels. When actual voltage is less than 16V, capacitors with 16V rated voltage can be used.
 6.3V: VREFM, VciOUT, C11, C12, VOUT, BIASC, Vci2, C21, C22, C23, VSH, VM
 25V(16V): VCH, CE, VCL

LCD Drive Voltage

The required voltage can be calculated by applying the following expressions. Drive voltages are standard; generate a voltage to suit the panel to be used.

$$VSH-VM, VM-VSL = \frac{1}{2} \sqrt{\frac{2\sqrt{N}}{\sqrt{N}-1}} \times V_{th}$$

$$VCH-VM, VM-VCL = \frac{1}{2} \sqrt{\frac{2\sqrt{N}}{\sqrt{N}-1}} \times V_{th}$$

Vth: Threshold voltage of the LCD panel to be used.
 N: Display duty cycle.

LCD Drive Bias

An optimal bias can be calculated by applying the following expression. The value that has been calculated is theoretically optimal. If a lower bias value than the optimal value is used to drive the LCD, contrast may be reduced depending on lighting conditions. However, the power consumption can be reduced by lowering the drive voltage. Adjust the value according to the system to be used.

$$\text{Bias value} = \frac{1}{\sqrt{N}}$$

How to determine the VCH voltage

$$VCH = N_B \times N_{D2} \times VSH$$

N_B : Bias ratio

N_{D2} : Step-up factor of the step-up circuit 2

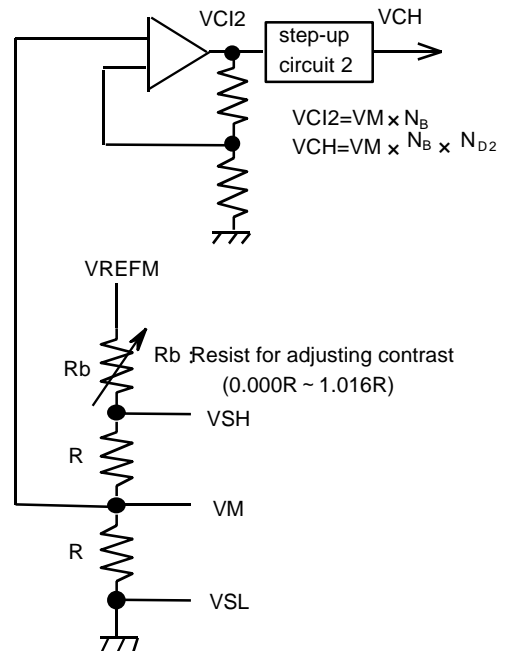
Contrast adjustment

R_B : Contrast resistance (0.000R to 1.016R)

$$VSH = VREFM \times 2R / (Rb + 2R)$$

Table 40

CT setting value							Rb resist value
CT6	CT5	CT4	CT3	CT2	CT1	CT0	
0	0	0	0	0	0	0	1.016R
0	0	0	0	0	0	1	1.008R
0	0	0	0	0	1	0	1.000R
0	0	0	0	0	1	1	0.992R
0	0	0	0	1	0	0	0.984R
		⋮			⋮		
1	1	1	1	1	1	0	0.008R
1	1	1	1	1	1	1	0.000R



How to determine the power setting value

1. Determine LCD drive bias

Determine LCD drive bias first. LCD drive bias is theoretically (1/SQRT (display duty)) optimal; however, the total drive voltage can be reduced by lowering bias ratio. Consider the display quality, the drive voltage and the current consumption.

2. Determine VOUT voltage

Determine factor of Vc1 regulator and step-up factor so as to set output voltage, VOUT of step-up circuit 1 4.0 to 5.75V, setting input voltage Vci2 of step-up circuit 2 more than +0.5V. Since the entire electric power for driving LCD is supplied from step-up circuit, subsequent voltage fall need to be considered.

3. Segment drive voltage calculation

Segment output drive voltage is calculated by the following expression.

$$V_{seg} = \sqrt{\frac{2 \times B}{B-1}} \times V_{TH}$$

B : LCD drive bias ratio
Vth: LCD threshold voltage

4. Common drive voltage calculation

Common output drive voltage is calculated by the following expression.

$$V_{com} = \frac{V_{seg}}{2} \times (B+1)$$

B : LCD drive bias ratio

5. Determine input voltage of step-up circuit 2

Determine input voltage of step-up circuit 2. This voltage is determined by dividing Vcom voltage by step-up factor; lower factors are used for low current consumption. Vci2 voltage need to be less than VOUT voltage (4.0 to 5.75 V)- 0.5V.

Example of register setting on power supply

Examples of register setting values on power supply are described below.

Example 1: 1/176 duty ratio, Vcc = VREFL = 3.0V, 1/13 bias

BS3-0 = H'8	: bias adjustment 1.4 times
BT2-0 = H'4	: step-up circuit 1 2 times step-up circuit 2 5 times
BT3 = H'1	: operate voltage inverting circuit
DC2-0 = H'6	step-up circuit 1 frequency 32 clocks step-up circuit 2 frequency 128 clocks
TBD	
AP1-0 = H'1	: low fixed current in the amplifier
VC2-0 = H'0	: Vci1 = 0.92 x Vcc = 2.75V
VR2-0 = H'0	: VREFM = 1.1 x VREFL
CT6-0	: appropriate contrast setting values

Example 2: 1/176 duty ratio, $V_{cc} = V_{REFL} = 2.4V$, $V_{ci} = 2.8V$, 1/13 bias

BS2-0 = H'8 : bias adjustment 1.4 times
BT2-0 = H'4 : step-up circuit 1 2 times step-up circuit 2 5 times
BT3 = H'1 : operate voltage inverting circuit
DC2-0 = H'6 : step-up circuit 1 frequency 32 clocks step-up circuit 2 frequency 128 clocks
TBD
AP1-0 = H'1 : low fixed current in the amplifier
VC2-0 = H'4 : internal V_{ci1} regulator off 2.8V directly supplied to V_{ci1}
VR3-0 = H'2 : $V_{REFM} = 1.4 \times V_{REFL}$
CT6-0 : appropriate contrast setting values

Example 3: Partial display, 1/24 duty ratio, $V_{cc} = 2.4V$, $V_{ci} = 2.8V$, 1/4 bias

BS2-0 = H'0 : bias adjustment 1.25 times
BT2-0 = H'0 : step-up circuit 1 2 times step-up circuit 2 2 times
BT3 = H'1 : operate voltage inverting circuit
DC2-0 = H'6 : step-up circuit 1 frequency 64 clocks step-up circuit 2 frequency 128 clocks
TBD
AP1-0 = H'1 : low fixed current in the amplifier
VC2-0 = H'4 : internal V_{ci1} regulator off
VR3-0 = H'2 : $V_{REG 1} = 1.4 \times V_{REFL}$
CT6-0 : appropriate contrast setting values

HD66766R power supply level correlation

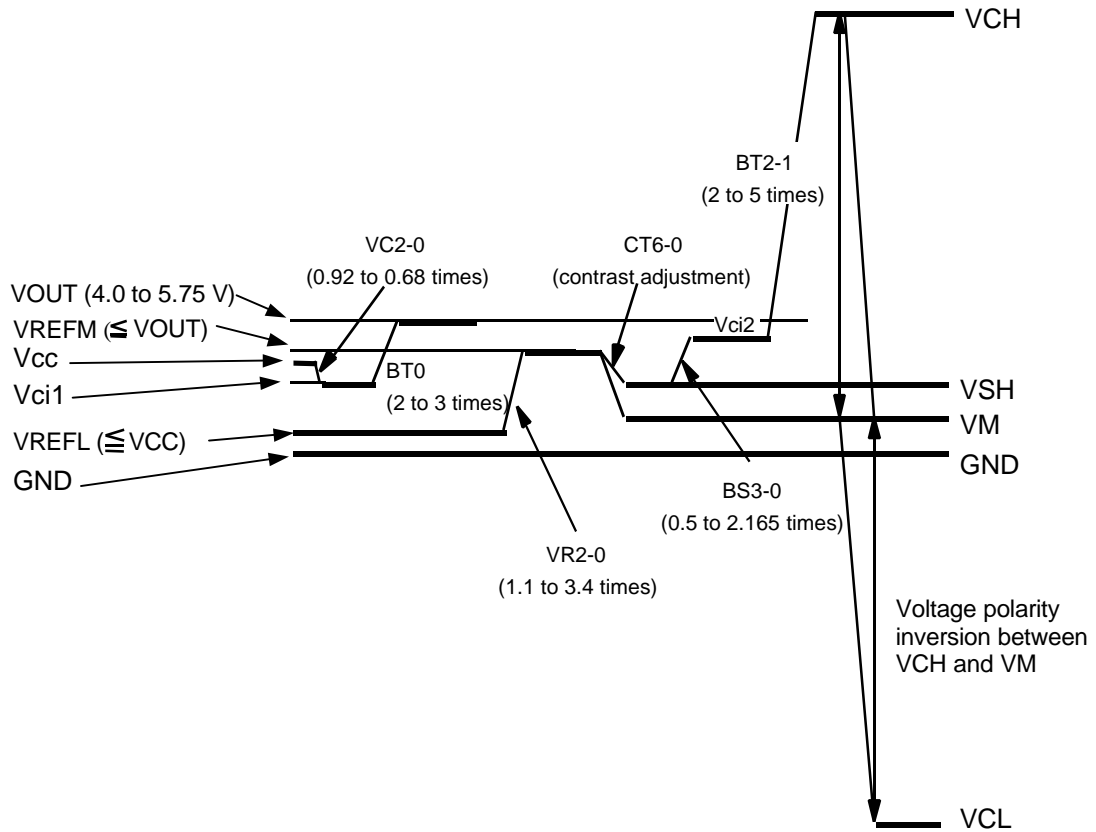
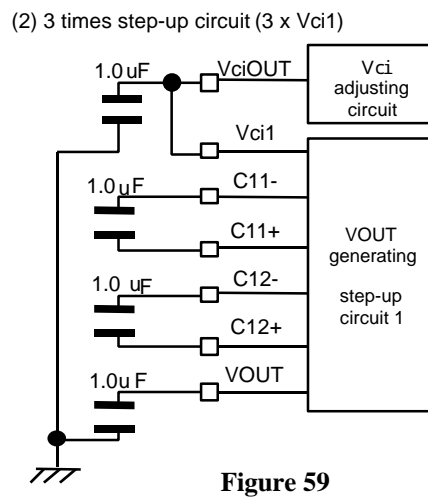
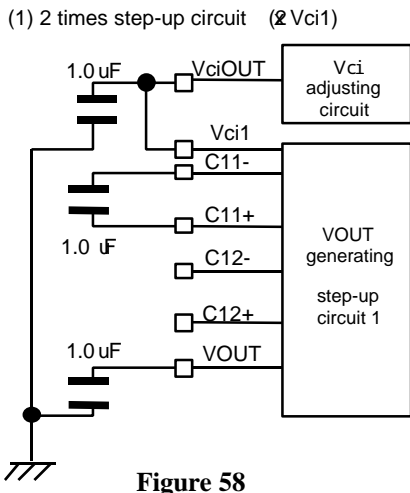
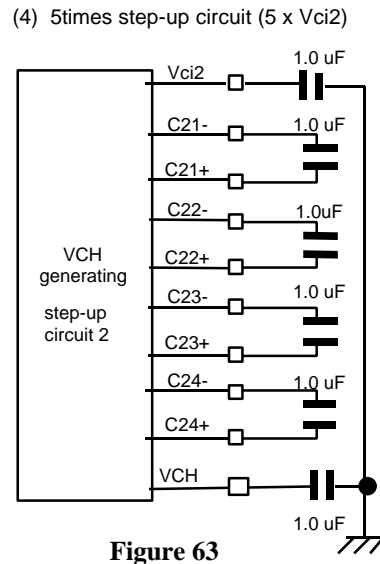
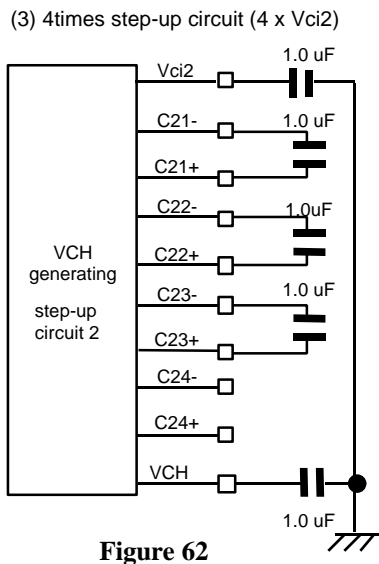
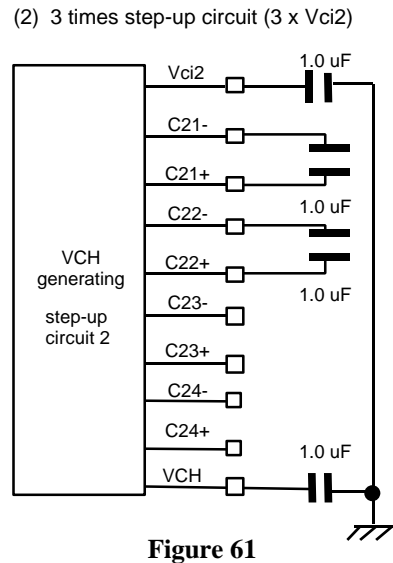
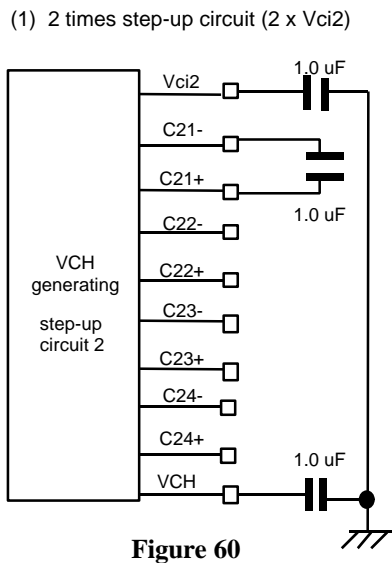


Figure 57 HD66766R Power supply level correlation

Connection of condenser related to the magnification of step up circuit 1



Connection of condenser related to the magnification of step up circuit 2



Absolute Maximum Ratings

Table 41

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	Vcc	V	-0.3 to + 4.6	1, 2
Power supply voltage (2)	Vcil	V	-0.3 to + 4.6	1, 3
Power supply voltage (3)	VCH-VCL	V	-0.3 to + 46	1, 4
Input voltage	Vt	V	-0.3 to Vcc + 0.3	1
Operating temperature	Topr	°C	-40 to + 85	1, 5
Storage temperature	Tstg	°C	-55 to + 110	1

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged.

Using the LSI within the following electrical characteristic limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. $V_{cc} \geq GND$ must be maintained
3. $V_{cil} \geq GND$ must be maintained.
4. $V_{CH} \geq GND$ must be maintained
 $GND \geq V_{CL}$ must be maintained
5. For die and wafer products, specified up to 85 °C.

DC Characteristics ($V_{CC} = 2.2$ to 3.6 V, $V_{CH}-V_{CL}=8$ V to 44 V, $T_a = -40$ to $+85^{\circ}\text{C}^{*1}$)

Table 42

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	$V_{CC} = 2.2$ to 3.6 V	$0.7 V_{CC}$	—	V_{CC}	2, 3
Input low voltage	V_{IL}	V	$V_{CC} = 2.2$ to 3.6 V	-0.3	—	$0.15V_{CC}$	2, 3
Output high voltage (1) (DB0-15 pins)	V_{OH1}	V	$I_{OH} = -0.1$ mA	$0.75V_{CC}$	—	—	2
Output low voltage (1) (DB0-15 pins)	V_{OL1}	V	$V_{CC} = 2.2$ to 2.4 V, $I_{OL} = 0.1$ mA	—	—	$0.2 V_{CC}$	2
			$V_{CC} = 2.4$ to 3.6 V, $I_{OL} = 0.1$ mA	—	—	$0.15V_{CC}$	2
Driver ON resistance (SEG pins)	R_{SEG}	k Ω	$\pm I_d = 0.05$ mA, $V_{LCD} = 3$ V	—	0.35	3	4
Driver ON resistance (COM pins)	R_{COM}	k Ω	$\pm I_d = 0.05$ mA, $V_{CH} - V_{CL} = 44$ V	—	0.90	3	4
I/O leakage current	I_{Li}	μA	$V_{in} = 0$ to V_{CC}	-1	—	1	5
Current consumption during normal operation ($V_{CC} - \text{GND}$)	I_{OP}	μA	R-C oscillation $V_{CC} = 3.0$ V, $V_{CH} = 20$ V, $V_M = 1.6$ V, $V_{CL} =$ -16.8 V, $T_a = 25^{\circ}\text{C}$ $f_{osc} = 276$ Khz (1/176 duty), 1/12 Bias CT minimum AP minimum, display all 0 Step-up 1 = two times Step-up 2 = five times $V_{CI1} = 0.92 \times V_{CC}$	—	480.	600	6
Current consumption during standby mode ($V_{CC} - \text{GND}$)	I_{ST}	μA	$V_{CC} = 3$ V, $T_a = 25^{\circ}\text{C}$	—	0.1	5	
			$V_{CC} = 3$ V, $T_a = 85^{\circ}\text{C}$	—	—	50	
VREFL input voltage	VREFL	V	$V_{CC} = 2.2$ V ~ 3.6 V	—	—	V_{CC}	
VREFM output voltage	VREFM	V	$V_{OUT} = 4.0$ V~ 5.75 V	—	—	$V_{OUT} - 0.5$	
Step up circuit 1 output voltage	V_{OUT}	V		4.0	—	5.75	
Step up circuit 2 output voltage	V_{CI2}	V		—	—	$V_{OUT} - 0.5$	

Step up circuit characteristics

Table 43

Item	Terminal	Unit	Test Condition	Min	Typ	Max	Notes
Step up circuit 1	VOUT	V	VCC = 3.0 [V] Vci step up factor = 0.92 Step up factor : two times Step up cycle: 32 divided cycle Load voltage = 400 [μA]	5.25	5.48	—	—
Step up circuit 2	VCH	V	VCC = 3.0 [V] VOUT = 5.5 [V] VREFL = 3.0 [V] VREFM = 1.1 x VREFL Constant current of operation amplifier: small Contrast adjustment value = 0.000R 1/12 bias Step up cycle of step up circuit 2: 96 divided cycle Step up factor: Five times Load current = 20 [uA]	21.2	21.3	—	(9)
Step up circuit 3	VCL	V	VCC = 3.0 [V] VOUT = 5.5 [V] VREFL = 3.0 [V] VREFM = 1.1 x VREFL Constant current of operation amplifier: small Contrast adjustment value = 0.000R 1/12 bias Step up cycle of polarity inversion circuit: 96 divided cycle Step up factor: Five times Load current = 20 [uA]	-21.0	-21.2	—	(9)

AC Characteristics ($V_{CC} = 2.2$ to 3.6 V, $T_a = -40$ to $+85^{\circ}\text{C}^{*1}$)

Table 44 Clock Characteristics ($V_{CC} = 2.2$ to 3.6 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	fcp	kHz	$V_{CC} = 2.2$ to 3.6 V	151	275	640	7
External clock duty ratio	Duty	%	$V_{CC} = 2.2$ to 3.6 V	45	50	55	7
External clock rise time	trcp	μs	$V_{CC} = 2.2$ to 3.6 V	—	—	0.2	7
External clock fall time	tfcf	μs	$V_{CC} = 2.2$ to 3.6 V	—	—	0.2	7
R-C oscillation clock	f _{osc}	kHz	Rf = 200k Ω , $V_{CC} = 3$ V	220	275	330	8

68-system Bus Interface Timing Characteristics

Table 45 Normal Write Mode (HWM=0)

($V_{CC} = 2.2$ to 2.4 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Enable cycle time	Write	t _{CYCE}	ns	Figure 1	600	—	—
	Read	t _{CYCE}	ns	Figure 1	800	—	—
Enable high-level pulse width	Write	PW _{EH}	ns	Figure 1	90	—	—
	Read	PW _{EH}	ns	Figure 1	350	—	—
Enable low-level pulse width	Write	PW _{EL}	ns	Figure 1	300	—	—
	Read	PW _{EL}	ns	Figure 1	400	—	—
Enable rise/fall time		t _{Er} , t _{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W to E, CS*)		t _{ASE}	ns	Figure 1	10	—	—
Address hold time		t _{AHE}	ns	Figure 1	5	—	—
Write data set up time		t _{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t _{HE}	ns	Figure 1	15	—	—
Read data delay time		t _{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t _{DHRE}	ns	Figure 1	5	—	—

Table 46 High-Speed Write Mode (HWM=1)

($V_{CC} = 2.2$ to 2.4 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Enable cycle time	Write	t _{CYCE}	ns	Figure 1	200	—	—
	Read	t _{CYCE}	ns	Figure 1	800	—	—
Enable high-level pulse width	Write	PW _{EH}	ns	Figure 1	90	—	—
	Read	PW _{EH}	ns	Figure 1	350	—	—
Enable low-level pulse width	Write	PW _{EL}	ns	Figure 1	90	—	—
	Read	PW _{EL}	ns	Figure 1	400	—	—
Enable rise/fall time		t _{Er} , t _{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W to E, CS*)		t _{ASE}	ns	Figure 1	10	—	—
Address hold time		t _{AHE}	ns	Figure 1	5	—	—
Write data set up time		t _{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t _{HE}	ns	Figure 1	15	—	—
Read data delay time		t _{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t _{DHRE}	ns	Figure 1	5	—	—

Normal Write Mode (HWM=0)

Table 47 (Vcc = 2.4 to 3.6 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Note
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	200	—	—	—
	Read	t_{CYCE}	ns	Figure 1	300	—	—	—
Enable high-level pulse width	Write	PW_{EH}	ns	Figure 1	40	—	—	—
	Read	PW_{EH}	ns	Figure 1	150	—	—	—
Enable low-level pulse width	Write	PW_{EL}	ns	Figure 1	100	—	—	—
	Read	PW_{EL}	ns	Figure 1	100	—	—	—
Enable rise/fall time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25	—
Set up time (RS, R/W to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—	Using status read
					0	—	—	Not using status read
Address hold time		t_{AHE}	ns	Figure 1	2	—	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—	—
Write data hold time		t_{HE}	ns	Figure 1	2	—	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	100	—
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—	—

High-Speed Write Mode (HWM=1)

Table 48 (Vcc = 2.4 V to 3.6 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Note
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	100	—	—	—
	Read	t_{CYCE}	ns	Figure 1	300	—	—	—
Enable high-level pulse width	Write	PW_{EH}	ns	Figure 1	40	—	—	—
	Read	PW_{EH}	ns	Figure 1	150	—	—	—
Enable low-level pulse width	Write	PW_{EL}	ns	Figure 1	40	—	—	—
	Read	PW_{EL}	ns	Figure 1	100	—	—	—
Enable rise/fall time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25	—
Set up time (RS, R/W to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—	Using status read
					0	—	—	Not using status read
Address hold time		t_{AHE}	ns	Figure 1	2	—	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—	—
Write data hold time		t_{HE}	ns	Figure 1	2	—	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	100	—

80-system Bus Interface Timing Characteristics**Normal Write Mode (HWM=0)****Table 49 (Vcc = 2.2 to 2.4 V)**

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	600	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	300	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Setup time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_H	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

High-Speed Write Mode (HWM=1)**Table 50 (Vcc = 2.2 to 2.4 V)**

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	90	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_H	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

Normal Write Mode (HWM = 0)

Table 51 (Vcc = 2.4 to 3.6 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Note
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—	
	Read	t_{CYCR}	ns	Figure 2	300	—	—	
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—	
Read low-level pulse width		PW_{LR}	ns	Figure 2	150	—	—	
Write high-level pulse width		PW_{HW}	ns	Figure 2	100	—	—	
Read high-level pulse width		PW_{HR}	ns	Figure 2	100	—	—	
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—	Using status read
					0	—	—	Not using status read
Address hold time		t_{AH}	ns	Figure 2	2	—	—	
Write data setup time		t_{DSW}	ns	Figure 2	60	—	—	
Write data hold time		t_H	ns	Figure 2	2	—	—	
Read data delay time		t_{DDR}	ns	Figure 2	—	—	100	
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—	

High-Speed Write Mode (HWM=1)

Table 52 (Vcc = 2.4 to 3.6 V)

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Note
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	100	—	—	
	Read	t_{CYCR}	ns	Figure 2	300	—	—	
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—	
Read low-level pulse width		PW_{LR}	ns	Figure 2	150	—	—	
Write high -level pulse width		PW_{HW}	ns	Figure 2	40	—	—	
Read high -level pulse width		PW_{HR}	ns	Figure 2	100	—	—	
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—	Using status read
					0	—	—	Not using status read
Address hold time		t_{AH}	ns	Figure 2	2	—	—	
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—	
Write data hold time		t_H	ns	Figure 2	2	—	—	
Read data delay time		t_{DDR}	ns	Figure 2	—	—	100	
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—	

Clock Synchronized Serial Interface Timing Characteristics

Table 53 (Vcc = 2.2 to 2.4 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	
Serial clock cycle time	Write (received)	t _{SCYC}	us	Figure 3	0.1	—	20
	Read (transmitted)	t _{SCYC}	us	Figure 3	0.25	—	20
Serial clock high-level pulse width	Write (received)	t _{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t _{SCH}	ns	Figure 3	120	—	—
Serial clock low-level pulse width	Write (received)	t _{SCL}	ns	Figure 3	40	—	—
	Read (transmitted)	t _{SCL}	ns	Figure 3	120	—	—
Serial clock rise/fall time	t _{scr, scf}	ns	Figure 3	—	—	20	
Chip select set up time	t _{CSU}	ns	Figure 3	20	—	—	
Chip select hold time	t _{CH}	ns	Figure 3	60	—	—	
Serial input data set up time	t _{SISU}	ns	Figure 3	30	—	—	
Serial input data hold time	t _{SIH}	ns	Figure 3	30	—	—	
Serial input data delay time	t _{SOD}	ns	Figure 3	—	—	130	
Serial input data hold time	t _{SOH}	ns	Figure 3	5	—	—	

Table 54 (Vcc = 2.4 to 3.6 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	
Serial clock cycle time	Write (received)	t _{SCYC}	us	Figure 3	0.076	—	20
	Read (transmitted)	t _{SCYC}	us	Figure 3	0.15	—	20
Serial clock high-level pulse width	Write (received)	t _{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t _{SCH}	ns	Figure 3	70	—	—
Serial clock low-level pulse width	Write (received)	t _{SCL}	ns	Figure 3	35	—	—
	Read (transmitted)	t _{SCL}	ns	Figure 3	70	—	—
Serial clock rise/fall time	t _{scr, scf}	ns	Figure 3	—	—	20	
Chip select set up time	t _{CSU}	ns	Figure 3	20	—	—	
Chip select hold time	t _{CH}	ns	Figure 3	60	—	—	
Serial input data set up time	t _{SISU}	ns	Figure 3	30	—	—	
Serial input data hold time	t _{SIH}	ns	Figure 3	30	—	—	
Serial output data delay time	t _{SOD}	ns	Figure 3	—	—	130	
Serial output data hold time	t _{SOH}	ns	Figure 3	5	—	—	

Reset Timing Characteristics ($V_{CC} = 2.2$ to 3.6 V)

Table 55

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 4	1	—	—
Reset rise time	$t_{r,RES}$	ms	Figure 4	—	—	10

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85°C.
2. The following three circuits are I pin, I/O pin, O pin configurations.

Pins: RESET*, CS*, E/WR, RW/RD, RS,
OSC1, IM2-1, IM0/ID, TEST1, TEST2

Pins: OSC2

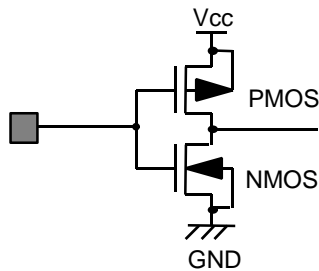


Figure 64

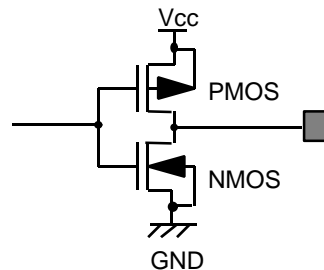


Figure 65

Pins: DB15 -DB2,
DB1/SD0, DB0/SD1

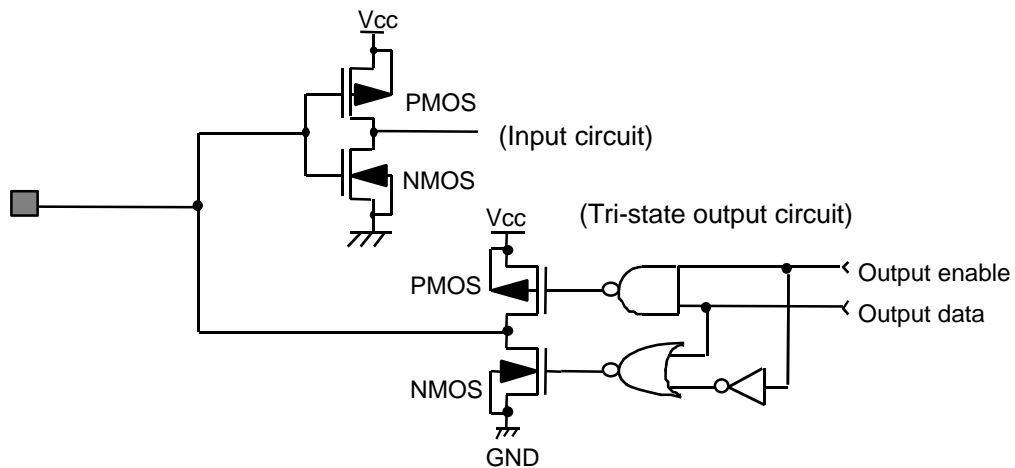


Figure 66 I/O Pin Configuration

3. The TEST1, TEST2 pins must be grounded and the IM2/1 and IM0/ID pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RSEG) between VSH, GND pins and segment signal pins.
5. This excludes the current flowing through output drive MOSs.

- 6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.
- 7. Applies to the external clock input (figure).

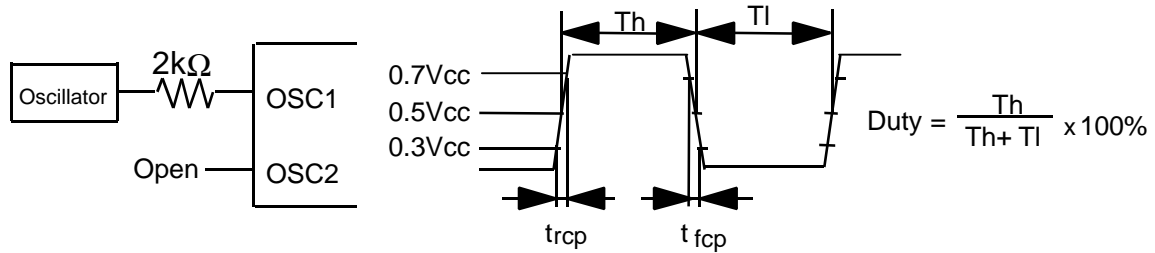


Figure 67 External Clock Supply

- 8. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).
- 9. Set VCI2 to maintain the relation VCI2 =< VOUT-0.5V.

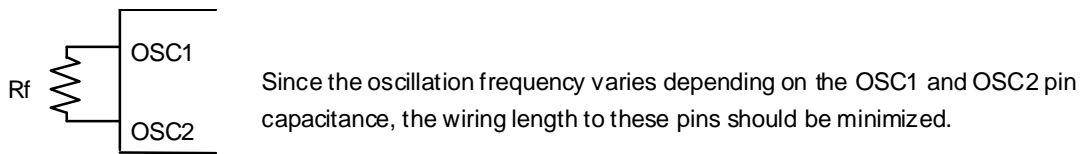


Figure 68 Internal Oscillation

External Resistance (Rf)	R-C Oscillation Frequency: fosc				
	Vcc = 1.8V	Vcc = 2.2 V	Vcc = 2.4 V	Vcc = 3.0 V	Vcc = 3.6 V
75 kΩ	364	495	559	631	687
130 kΩ	263	345	381	421	453
180 kΩ	210	270	295	323	344
200 kΩ	193	245	266	290	307
240 kΩ	174	218	236	256	270
280 kΩ	156	194	210	226	238
360 kΩ	129	158	170	182	191
470 kΩ	102	122	129	137	142

Table 56 External Resistance Value and R-C Oscillation Frequency (Referential Data)

Step-up circuit loading characteristics (Reference data)

(1) Step-up circuit 1 – loading characteristic

Measuring condition

Ta = 25C, VCC = 3.0 [V], Oscillation frequency = 250 [kHz]

(2) Vci1 step-up magnification = 0.92, Step-up magnification two times

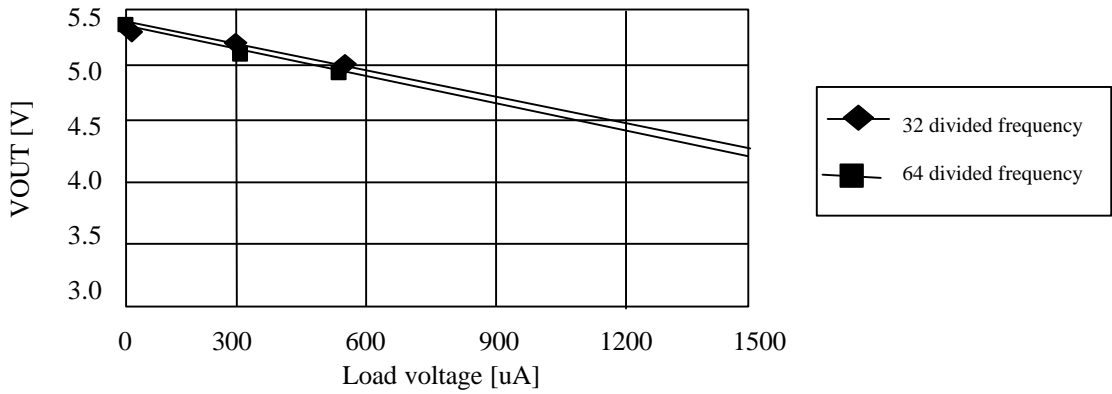


Figure 69 Step-up circuit 1- load characteristic (AP=01 amplifier constant voltage: small)

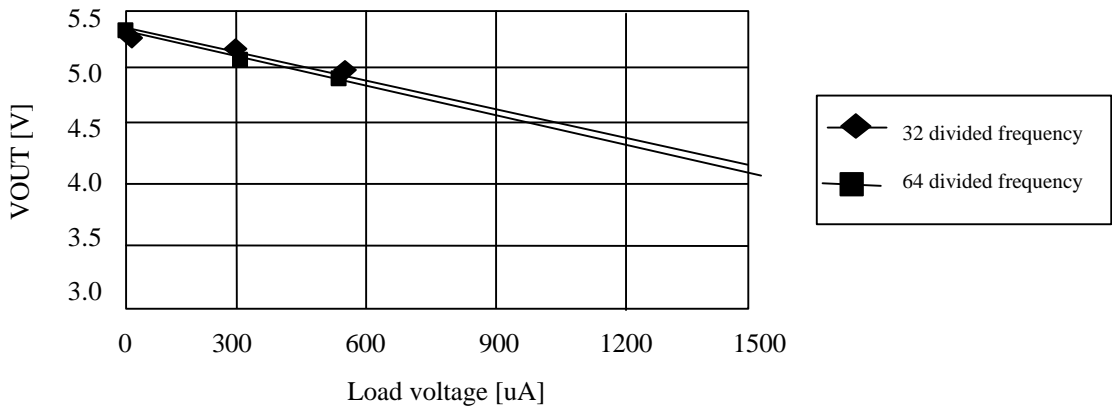


Figure 70 Step-up circuit 1- load characteristic (AP=10 amplifier constant voltage: medium)

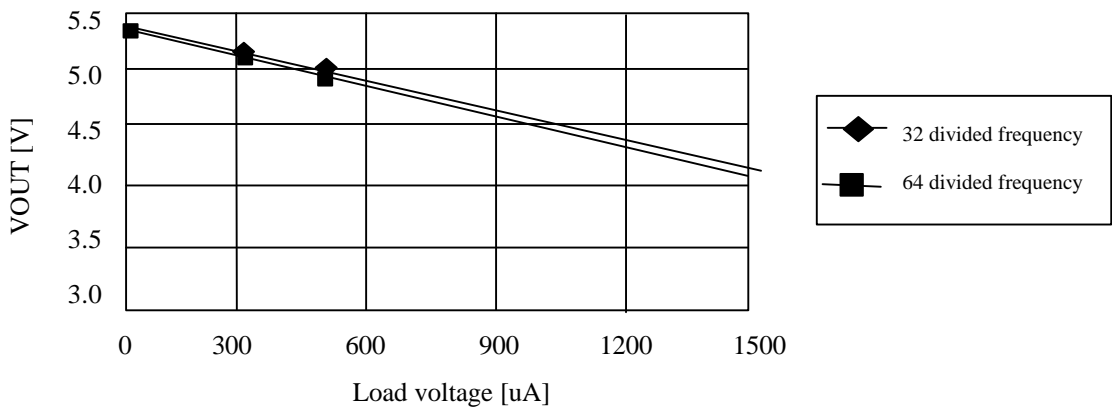


Figure 71 Step-up circuit 1- load characteristic (AP=11 amplifier constant voltage: large)

(2) Step-up circuit 2 – loading characteristic

Measuring condition

Ta = 25C, VCC = 3.0 [V], Oscillation frequency = 250 [kHz]

Vci1 step-up magnification = 0.92, Step-up circuit 1: step-up magnification two times

32 divided frequency, VREFM = 1.1 x VREFL, CT = 0.00R1/12 Bias

Step-up circuit 2: Five times step-up

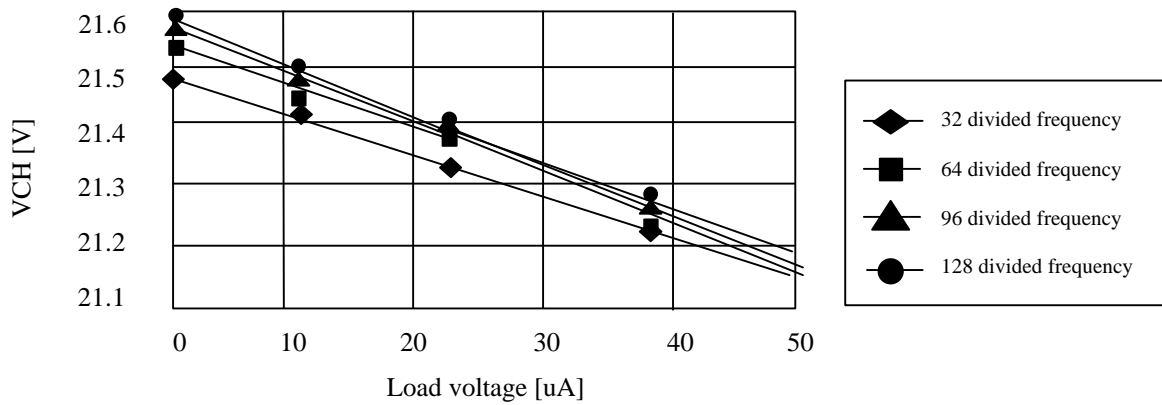


Figure 72 Step-up circuit 2- load characteristic (AP=01 amplifier constant voltage: small)

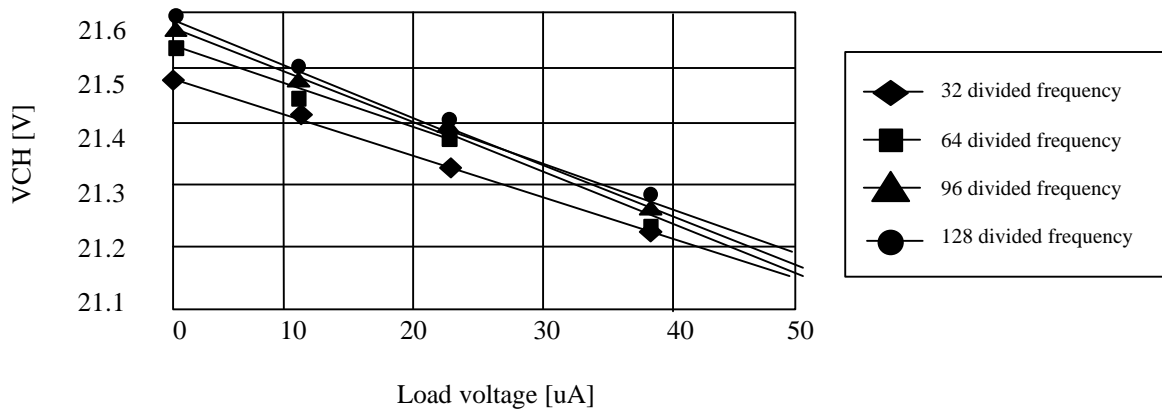


Figure 73 Step-up circuit 2- load characteristic (AP=10 amplifier constant voltage: medium)

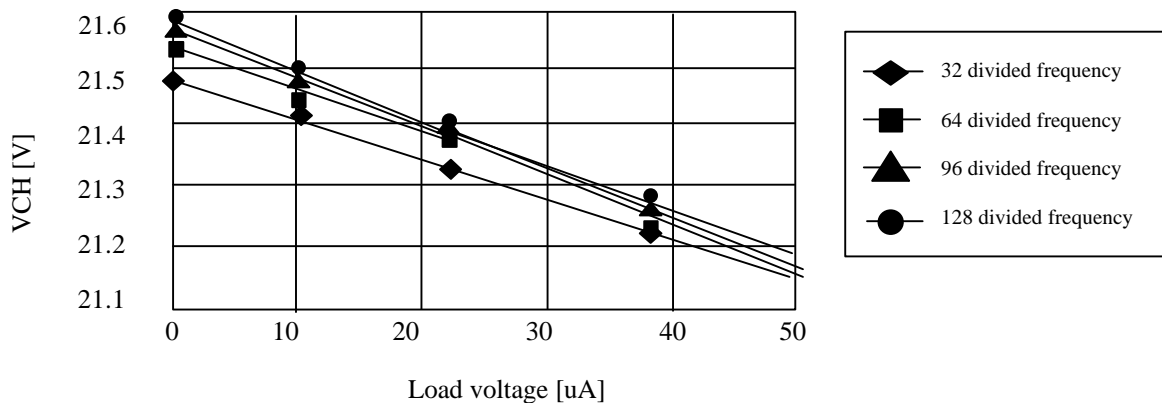


Figure 74 Step-up circuit 2- load characteristic (AP=11 amplifier constant voltage: large)

(3) Polarity inversion circuit – loading characteristic

Measuring condition

Ta = 25C, VCC = 3.0 [V], Oscillation frequency = 250 [kHz]

Vci1 step-up magnification = 0.92, Step-up circuit 1 step-up magnification two times

32 divided frequency, VREFM = 1.1 x VREFL, CT = 0.00R 1/12 Vias

Step-up circuit 2: Five times

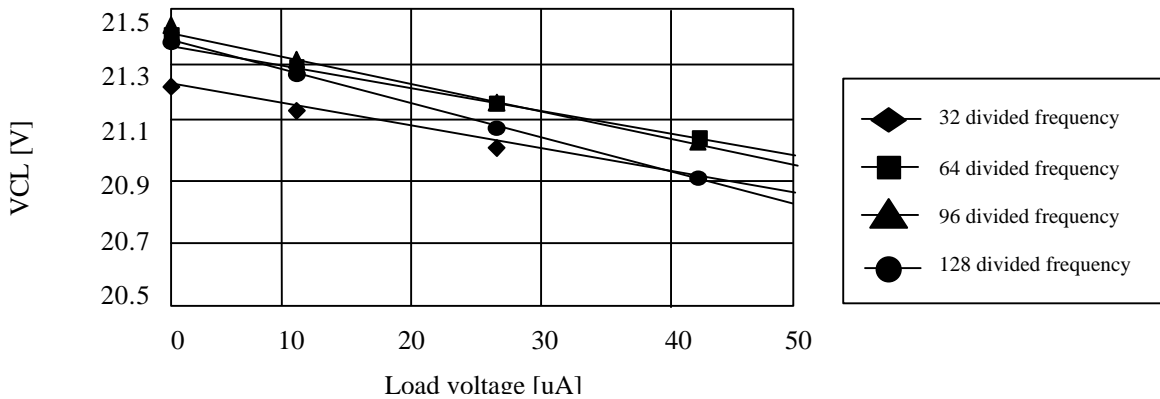


Figure 75 Polarity inversion circuit – Load characteristic (AP=01 amplifier constant current: small)

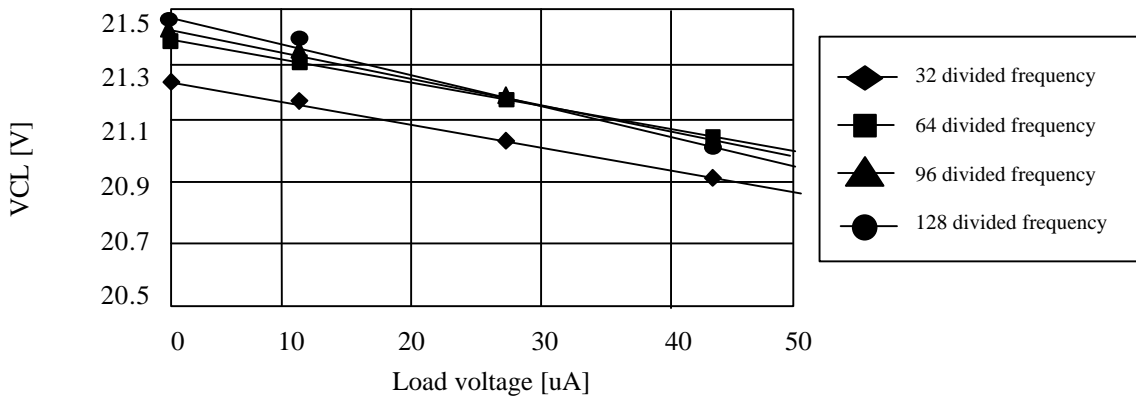


Figure 76 Polarity inversion circuit - Load characteristic (AP=10 amplifier constant current: medium)

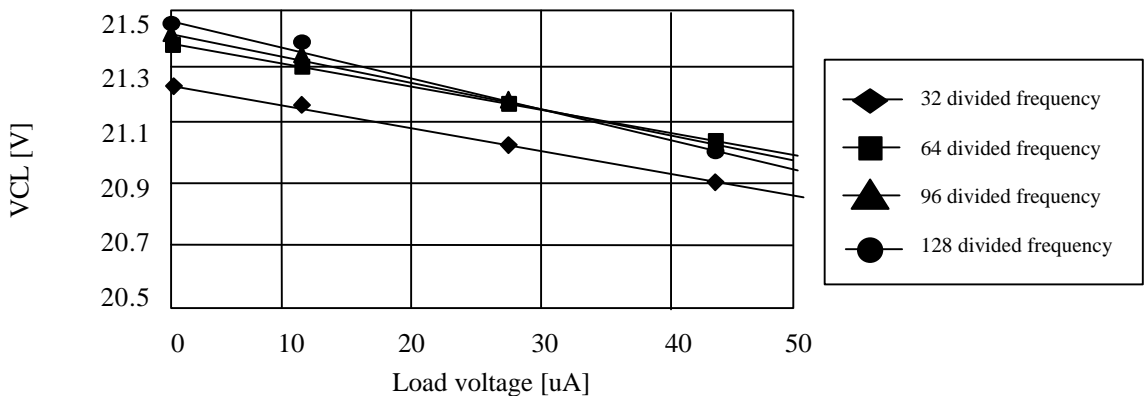


Figure 77 Polarity inversion circuit - Load characteristic (AP=11 amplifier constant current: large)

Load Circuits

AC Characteristics Test Load Circuits

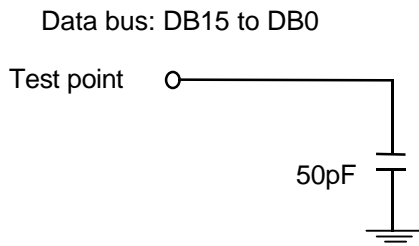


Figure 78 Load Circuit

Timing Characteristics

68-system Bus Operation

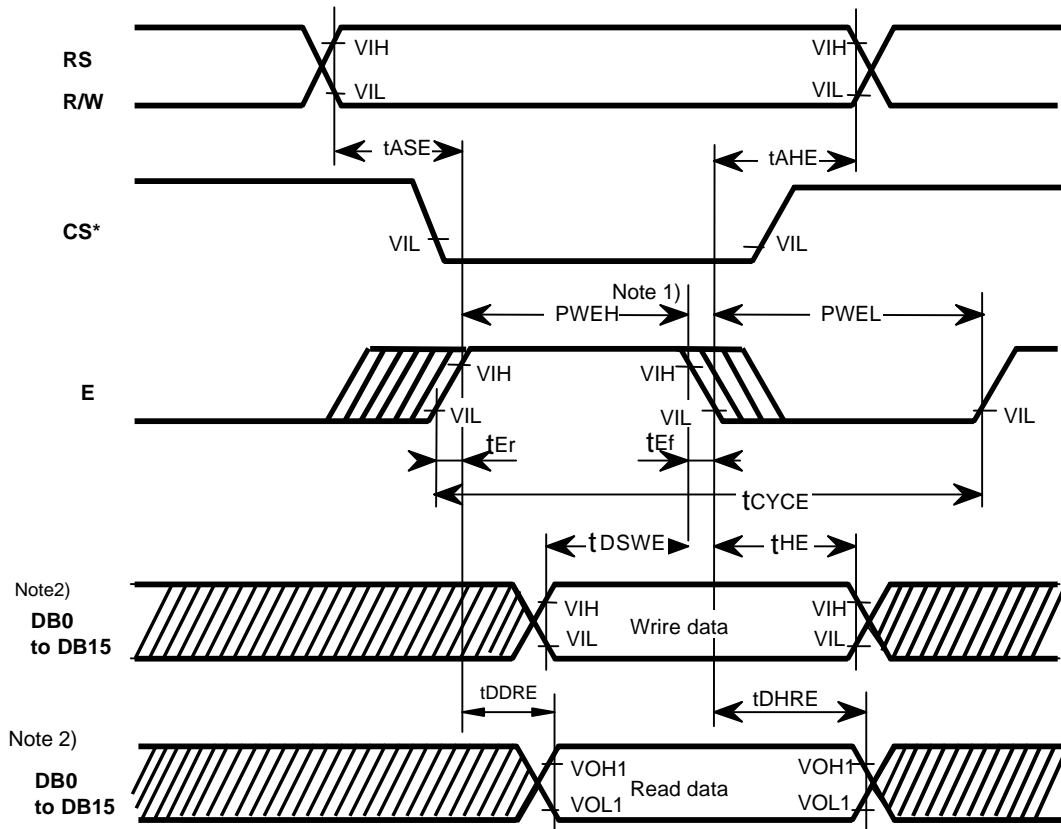


Figure79 68-system Bus Timing

- Notes: 1) PWEH is specified in the overlapped period when CS* is low and E is high.
 2) Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used.
 Fix the DB7-0 pins to Vcc or GND.

80-system Bus Operation

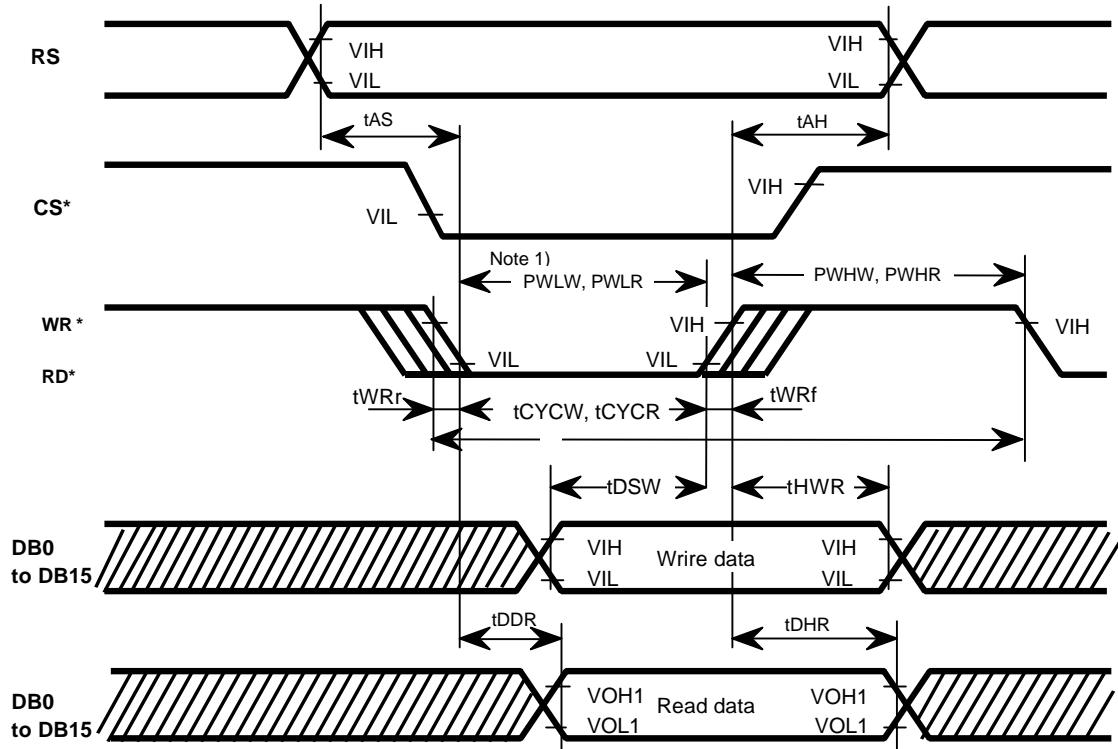


Figure 80 80-system Bus Timing

Note1) PWLW and PWLR are specified in the overlapped period when CS* is low and WR* or RD* is low.

Note2) Parallel data transfer is enabled on the DB15-0 pins when the 8-bit bus interface is used. Fix the DB7-0 pins to Vcc or GND.

Clock Synchronized Serial Interface Operation

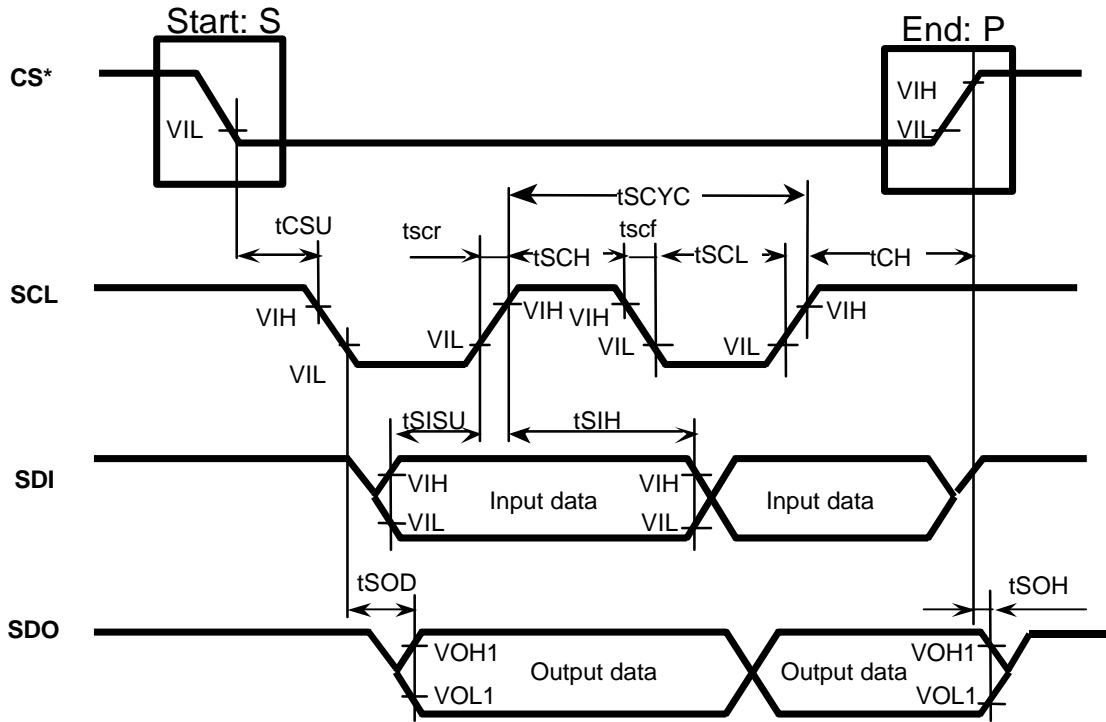


Figure 81 Clock Synchronized Serial Interface Timing

Reset Operation

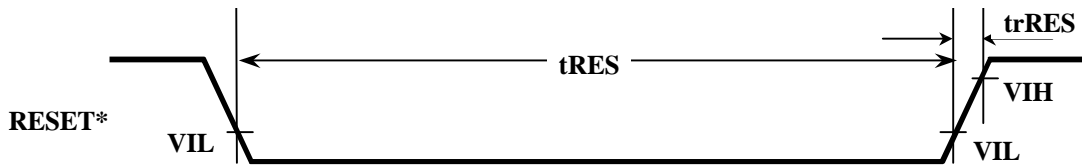


Figure 82 Reset Timin

Additional Issue

HD66766R Contrast fluctuation on RAM access

Hitachi one-chip driver; HD66766R has contrast fluctuation while accessing the internal RAM. This phenomenon occurs according to the structure of external circuit and the usage of HD66766R. Please have a clear understanding of the phenomenon and measures described below before using HD66766R.

1. Contrast fluctuation

When HD66766R is mounted on glass, the grand terminal gets contact with resistance of ITO wiring. HD66766R has 8 GNDs, 4 AGNDs for power supply circuit, and another 4 GNDs for RAM and Logic. When all the GNDs are connected on glass with ITO, transferring display data to the internal RAM at high-speed causes high current consumption. And resistance of ITO wiring connected with GND terminal raises the voltage. The raised voltage is amplified with a step-up circuit, and it results in a decrease of VCH/VCL voltage causing contrast fluctuation on display. Figure 1 shows the mechanism of the phenomenon. Figure 2 shows decrease of VCH voltage according to RAM access frequency and resistance of ITO wiring. (The value shown in Figure 2 is the actual data of a typical sample of HD66766R measured by Hitachi's jig.)

2. Measures

ITO patterns on glass must be separated as shown in Figure 3. (Even if GND bumps are separated on LSI, if ITO patterns on glass are connected, GND level rises up in RAM circuit and Logic circuit.) Also, GND resistor should be designed to be less than 10 Ω, considering the decrease of VCH voltage caused by the raise of GND voltage.

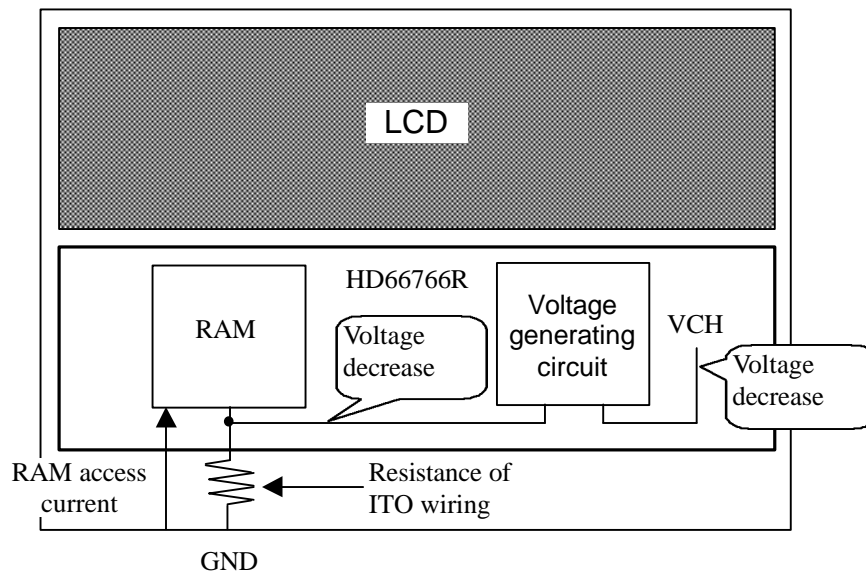


Figure 1 Influence of ITO wiring resistance

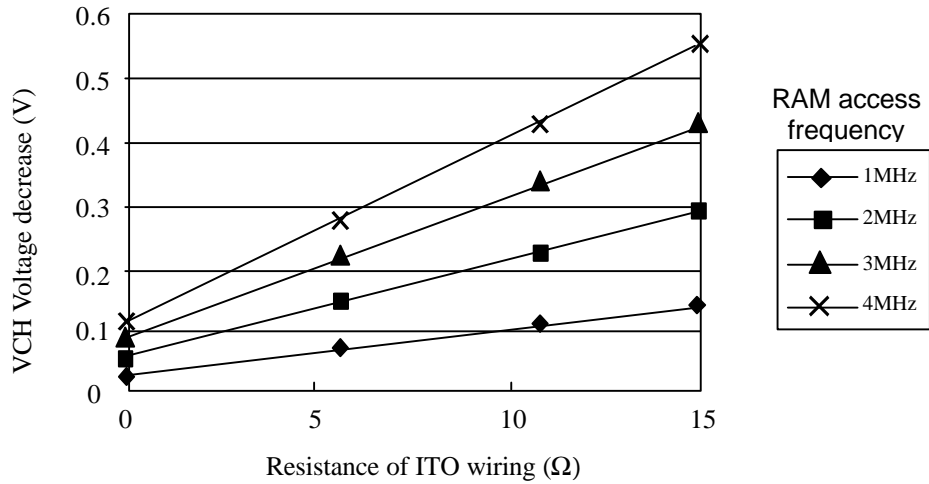


Figure 2 VCH voltage decrease depending on RAM access frequency and Resistance of ITO wiring

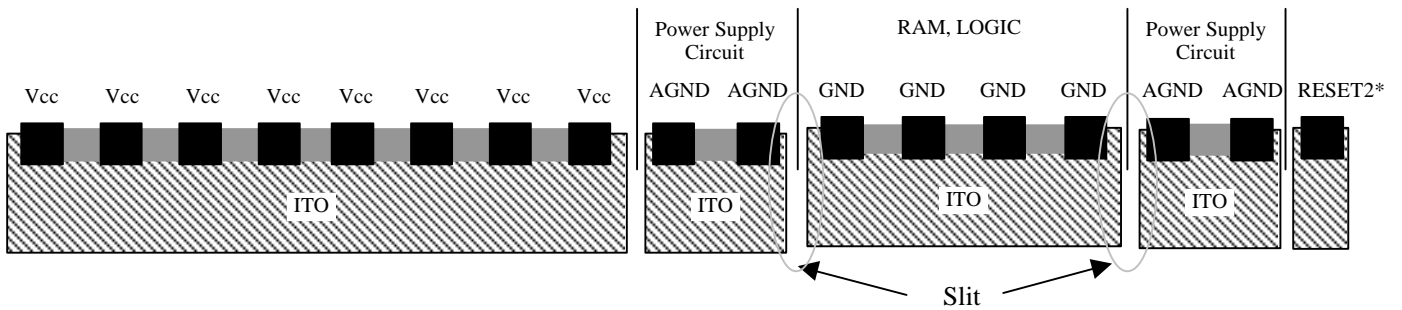


Figure 3 Recommended ITO Connection Pattern (HCD667X66)

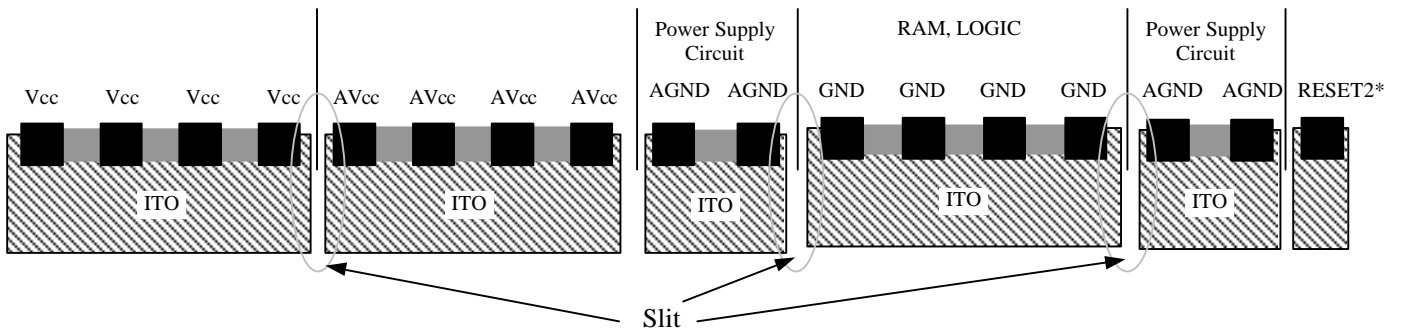


Figure 4 Recommended ITO Connection Pattern (HCD667X66R)

Maintenance history report

Rev.	Date	Contents
1.0	August 8, 2002	First release
1.1	September 17, 2002	P74 2.Determine VOUT voltage Line2 From “4.0 to 5.5V” to “4.0 to 5.75 V” P74 5.Determine input voltage of step-up circuit2 Line 3 From “4.5 to 5.75V)-0.5V” to “ (4.0 to 5.75V)-0.5V