

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER  
WITH INJECTION-CURRENT EFFECT CONTROL

SCLS554A – JANUARY 2004 – REVISED MARCH 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Injection-Current Cross Coupling  $<1\text{mV}/\text{mA}$  (see Figure 1)
- Low Crosstalk Between Switches
- Pin Compatible With CD74HC4051, SN74LV4051A, and CD4051B
- 2-V to 6-V  $V_{CC}$  Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

† Contact factory for details. Q100 qualification data available on request.

## description/ordering information

This eight-channel CMOS analog multiplexer/demultiplexer is pin compatible with the '4051 function and, additionally, features injection-current effect control, which has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

## ORDERING INFORMATION

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Tape and reel	SN74HC4851QDRQ1	HC4851Q
	TSSOP – PW	Tape and reel	SN74HC4851QPWRQ1	HC4851Q

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE

INH	INPUTS				ON CHANNEL
	C	B	A		
L	L	L	L		Y0
L	L	L	H		Y1
L	L	H	L		Y2
L	L	H	H		Y3
L	H	L	L		Y4
L	H	L	H		Y5
L	H	H	L		Y6
L	H	H	H		Y7
H	X	X	X		None

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

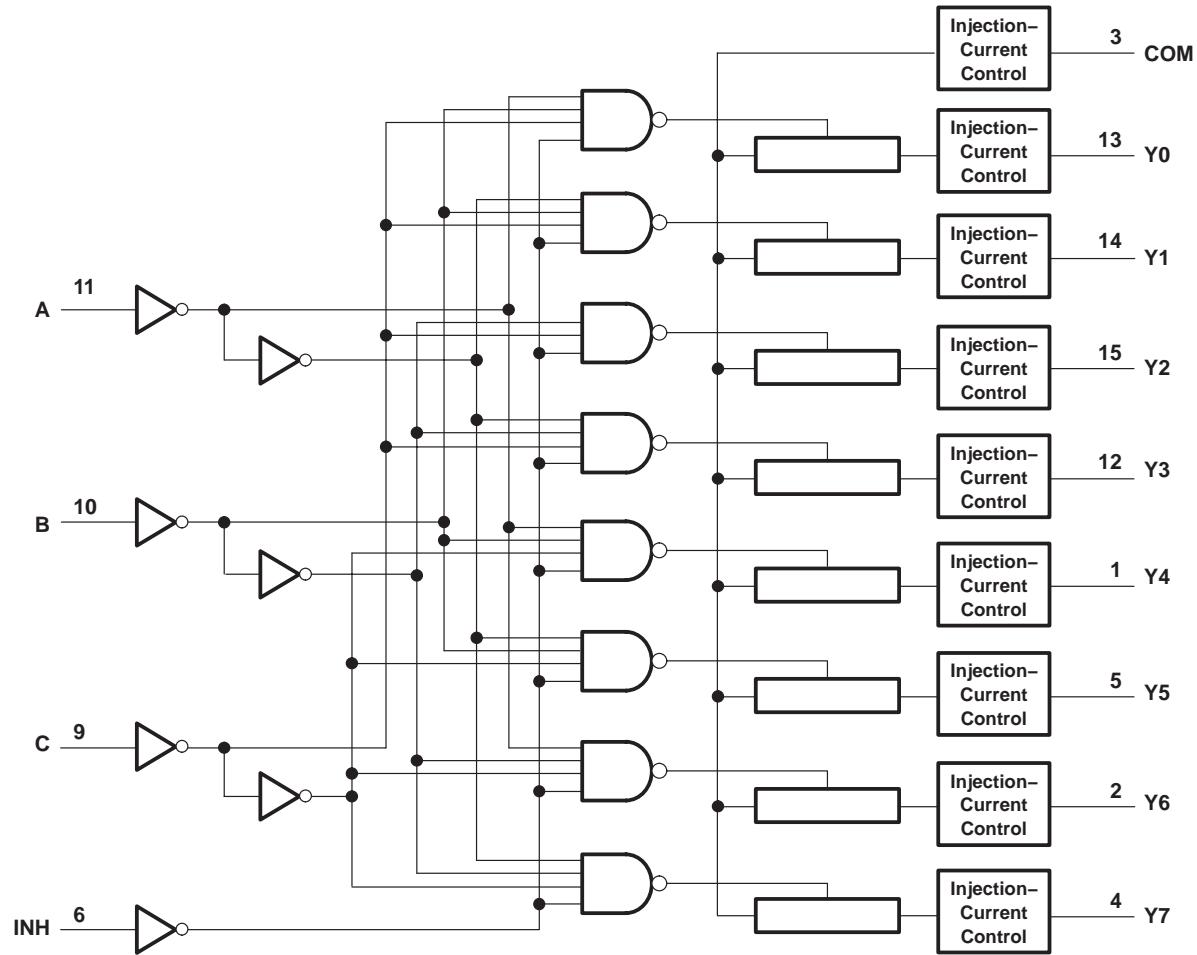


PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**logic diagram (positive logic)**



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

1. The input and output voltage ratings may be exceeded if the input and output current is increased.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	6	V
$V_{IH}$	High-level input voltage, control inputs	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 3.3\text{ V}$	2.3	
		$V_{CC} = 4.5\text{ V}$	3.15	
		$V_{CC} = 6\text{ V}$	4.2	
$V_{IL}$	Low-level input voltage, control inputs	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 3.3\text{ V}$	1	
		$V_{CC} = 4.5\text{ V}$	1.35	
		$V_{CC} = 6\text{ V}$	1.8	
$V_I$	Control input voltage	0	$V_{CC}$	V
$V_{IO}$	Input/output voltage	0	$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall time	$V_{CC} = 2\text{ V}$	1000	ns
		$V_{CC} = 3\text{ V}$	800	
		$V_{CC} = 3.3\text{ V}$	700	
		$V_{CC} = 4.5\text{ V}$	500	
		$V_{CC} = 6\text{ V}$	400	
$T_A$	Operating free-air temperature	-40	125	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r <sub>on</sub>	On-state switch resistance  I <sub>T</sub> ≤ 2 mA, V <sub>I</sub> = V <sub>CC</sub> to GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 5)	2.0	500	650		670		700		Ω
		3 V	215	280		320		360		
		3.3 V	210	270		305		345		
		4.5 V	160	210		240		270		
		6 V	150	195		220		250		
Δr <sub>on</sub>	Difference in on-state resistance between switches  I <sub>T</sub> ≤ 2 mA, V <sub>I</sub> = V <sub>CC</sub> /2, V <sub>INH</sub> = V <sub>IL</sub>	2.0	4	13		18		23		Ω
		3 V	2	10		12		16		
		3.3 V	2	9		12		16		
		4.5 V	2	9		12		16		
		6 V	3	10		14		19		
I <sub>I</sub>	Control input current  V <sub>I</sub> = V <sub>CC</sub> or GND	6 V		±0.1		±0.1		±1	μA	
I <sub>S(off)</sub>	Off-state switch leakage current (any one channel)  V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IH</sub> (see Figure 6)	6 V		±0.1		±0.5		±1	μA	
	Off-state switch leakage current (common channel)  V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IH</sub> (see Figure 7)			±0.2		±2		±4	μA	
I <sub>S(on)</sub>	On-state switch leakage current  V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> (see Figure 8)	6 V		±0.1		±0.5		±1	μA	
I <sub>CC</sub>	Supply current  V <sub>I</sub> = V <sub>CC</sub> or GND	6 V		2		20		40	μA	
C <sub>IC</sub>	Control input capacitance  A, B, C, INH			3.5	10		10	10	pF	
C <sub>IS</sub>	Common terminal capacitance  Switch off			22	40		40	40	pF	
C <sub>OS</sub>	Switch terminal capacitance  Switch off			6.7	15		15	15	pF	

injection current coupling specifications, T<sub>A</sub> = -40°C to 125°C

PARAMETER	V <sub>CC</sub>	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>Δout</sub>	3.3 V	R <sub>S</sub> ≤ 3.9 kΩ  I <sub>I</sub> ‡ ≤ 1 mA	0.05	1		mV
	5 V		0.1	1		
	3.3 V		0.345	5		
	5 V		0.067	5		
	3.3 V	R <sub>S</sub> ≤ 20 kΩ  I <sub>I</sub> ‡ ≤ 10 mA	0.05	2		
	5 V		0.11	2		
	3.3 V		0.05	20		
	5 V		0.024	20		

† Typical values are measured at T<sub>A</sub> = 25°C.

‡ I<sub>I</sub> = total current injected into all disabled channels

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2 \text{ V}$ ,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figures 9–14)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO $85^\circ\text{C}$		UP TO $125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	COM or $Y_n$	Y <sub>n</sub> or COM	19.5	30	34		37	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	A, B, C	COM or $Y_n$	23	35	40		45	ns	
$t_{PZH}$ $t_{PZL}$	Enable delay time	INH	COM or $Y_n$		95	105		115	ns	
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or $Y_n$		95	105		115	ns	

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3 \text{ V}$ ,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figures 9–14)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO $85^\circ\text{C}$		UP TO $125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	COM or $Y_n$	Y <sub>n</sub> or COM	12	17.5	19.5		21.5	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	A, B, C	COM or $Y_n$	13.5	19.5	22		25	ns	
$t_{PZH}$ $t_{PZL}$	Enable delay time	INH	COM or $Y_n$		90	100		110	ns	
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or $Y_n$		90	100		110	ns	

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V}$ ,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figures 9–14)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			UP TO $85^\circ\text{C}$		UP TO $125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	COM or $Y_n$	Y <sub>n</sub> or COM	11	16.5	18.5		20.5	ns	
$t_{PLH}$ $t_{PHL}$	Propagation delay time	A, B, C	COM or $Y_n$	12.5	18.5	21		24	ns	
$t_{PZH}$ $t_{PZL}$	Enable delay time	INH	COM or $Y_n$		85	95		105	ns	
$t_{PHZ}$ $t_{PLZ}$	Disable delay time	INH	COM or $Y_n$		85	95		105	ns	

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 4.5$  V,  $C_L = 50$  pF (unless otherwise noted) (see Figures 9–14)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	8.6	14	15		16	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	A, B, C	COM or Y <sub>n</sub>	10	16	18		20	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>		80	90		100	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>		80	90		100	ns	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 6$  V,  $C_L = 50$  pF (unless otherwise noted) (see Figures 9–14)

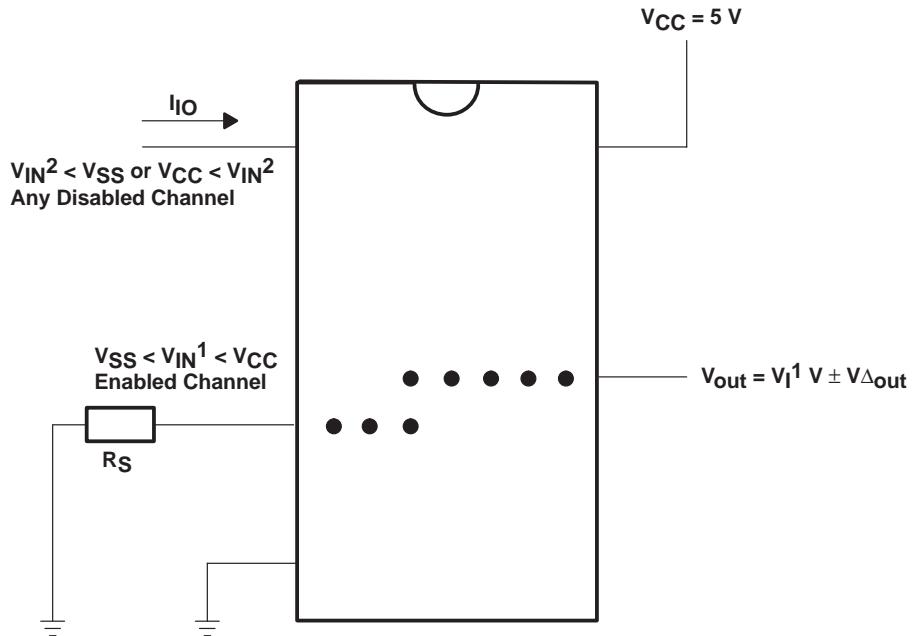
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			UP TO 85°C		UP TO 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	COM or Y <sub>n</sub>	Y <sub>n</sub> or COM	8	12.5	13.5		14.5	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time	A, B, C	COM or Y <sub>n</sub>	9.5	15	17		19	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Enable delay time	INH	COM or Y <sub>n</sub>		78	80		80	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable delay time	INH	COM or Y <sub>n</sub>		78	80		80	ns	

operating characteristics,  $T_A = 25^\circ\text{C}$  (see Figure 15)

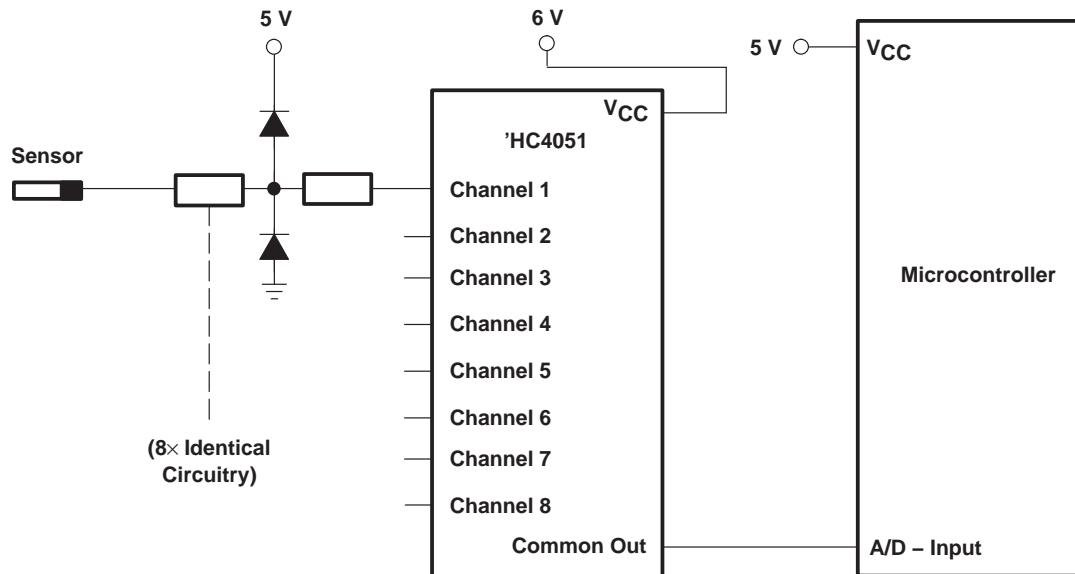
PARAMETER			V <sub>CC</sub>	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance		3.3 V	No load	32	pF
			5 V		37	

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**APPLICATION INFORMATION**



**Figure 1. Injection-Current Coupling Specification**



**Figure 2. Alternate Solution Requires 32 Passive Components and One Extra 6-V Regulator  
 to Suppress Injection Current Into a Standard 'HC4051 Multiplexer**

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**APPLICATION INFORMATION**

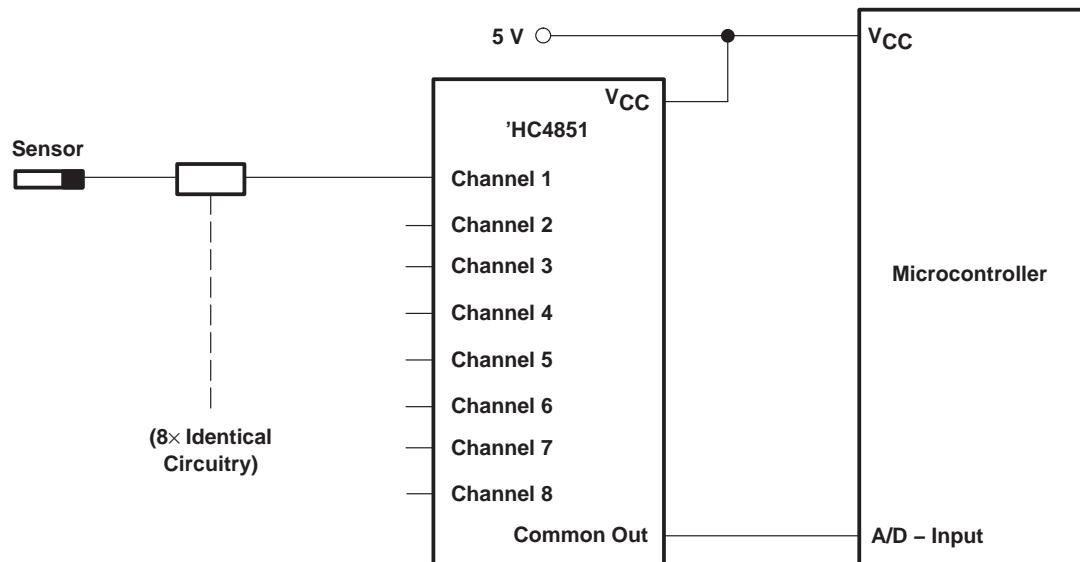


Figure 3. Solution by Applying the 'HC4851' Multiplexer

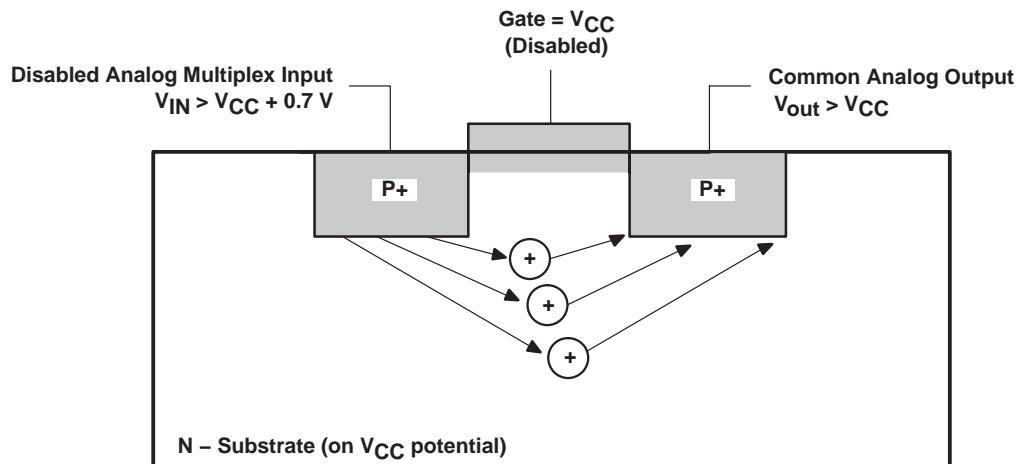


Figure 4. Diagram of Bipolar Coupling Mechanism  
(Appears if  $V_{IN}$  Exceeds  $V_{CC}$ , Driving Injection Current Into the Substrate)

PARAMETER MEASUREMENT INFORMATION

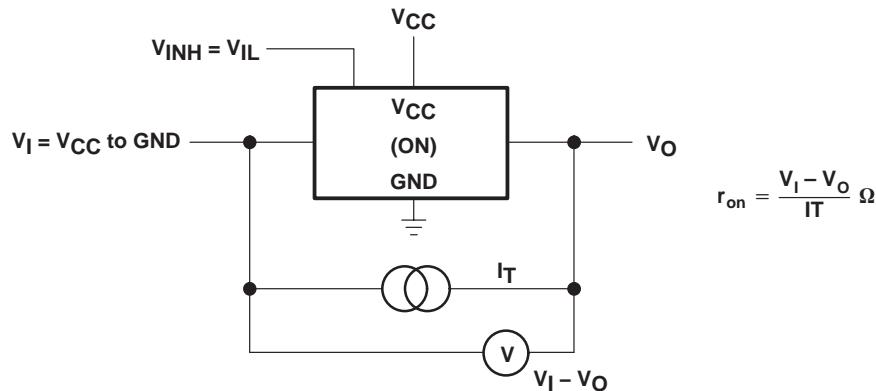


Figure 5. On-State-Resistance Test Circuit

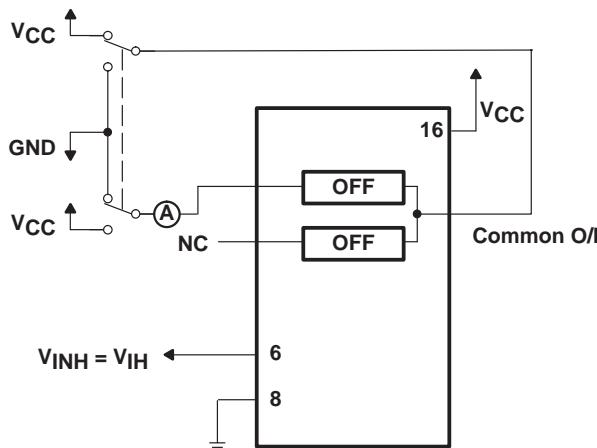


Figure 6. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

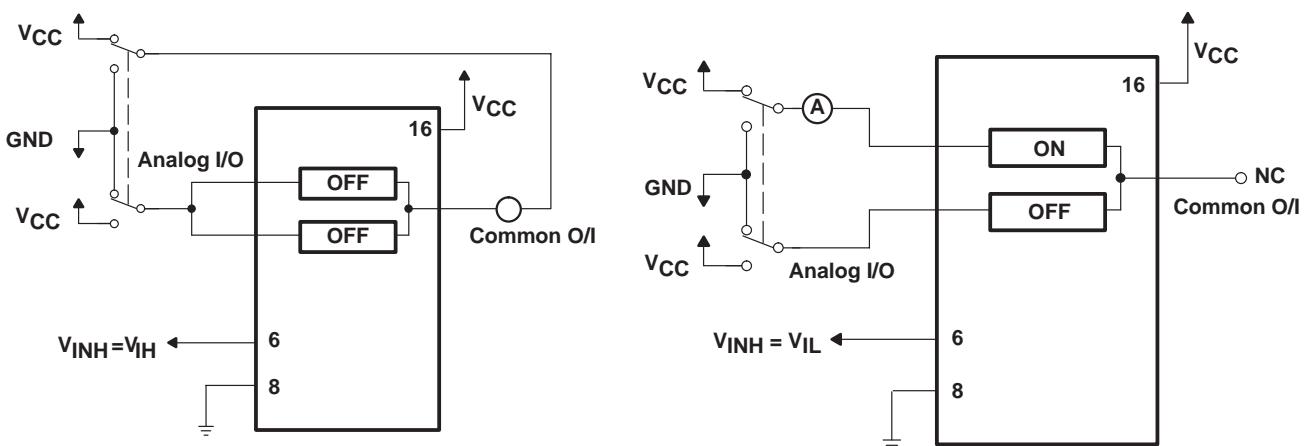


Figure 7. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

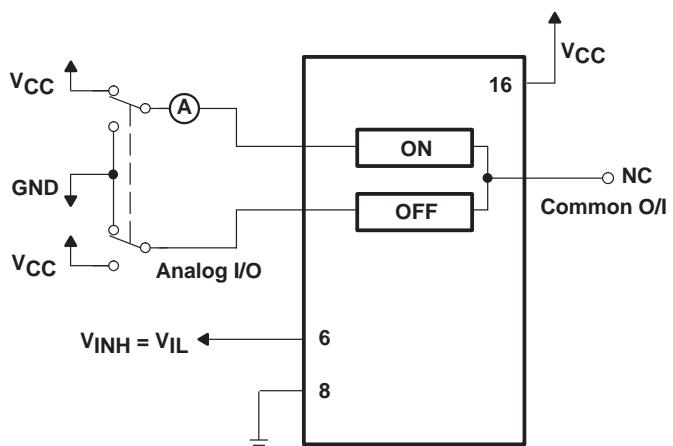
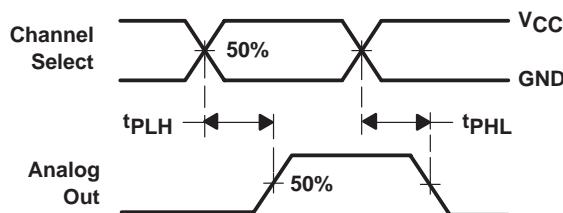


Figure 8. Maximum On-Channel Leakage Current, Channel to Channel, Test Setup

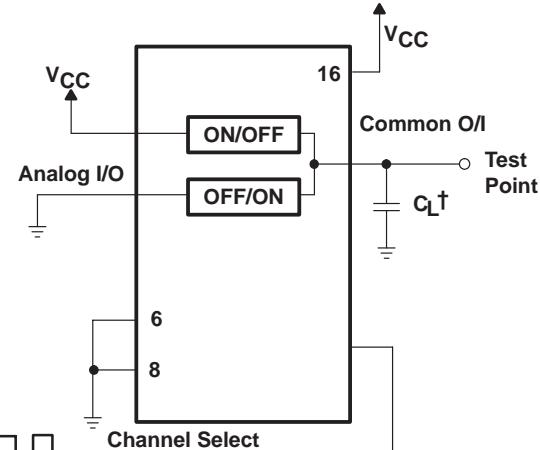
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**PARAMETER MEASUREMENT INFORMATION**

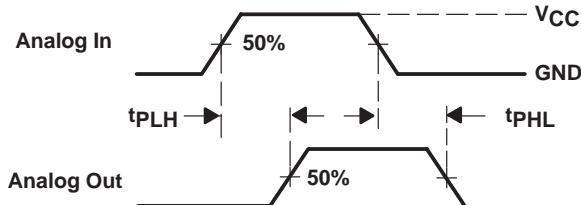


**Figure 9. Propagation Delays,  
 Channel Select to Analog Out**

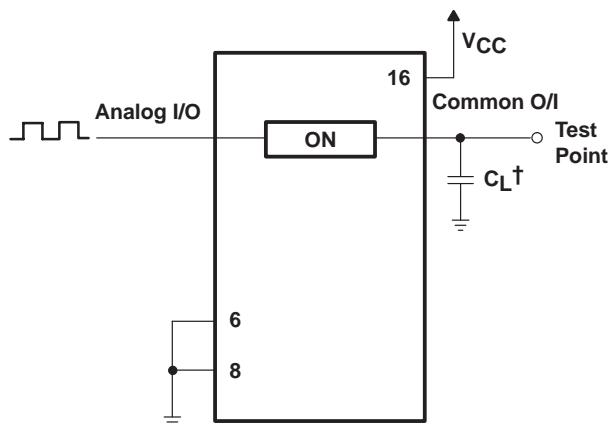


† Includes all probe and jig capacitance

**Figure 10. Propagation-Delay Test Setup,  
 Channel Select to Analog Out**



**Figure 11. Propagation Delays,  
 Analog In to Analog Out**



† Includes all probe and jig capacitance

**Figure 12. Propagation-Delay Test Setup,  
 Analog In to Analog Out**

**PARAMETER MEASUREMENT INFORMATION**

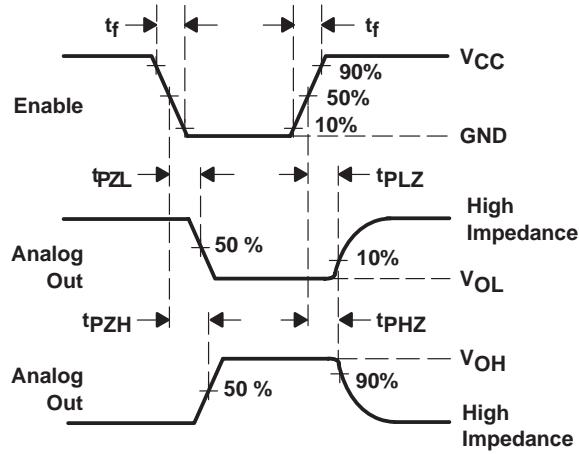


Figure 13. Propagation Delays,  
 Enable to Analog Out

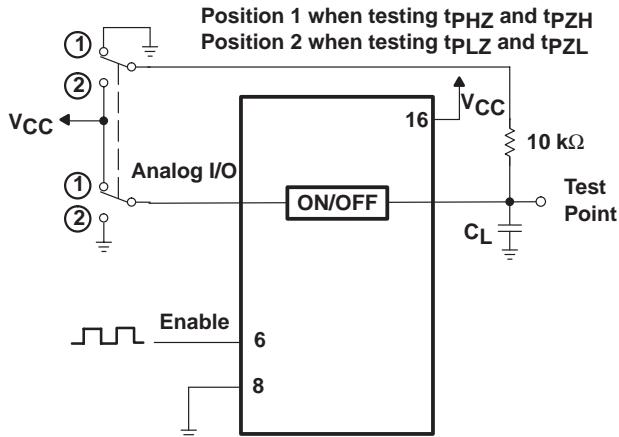


Figure 14. Propagation-Delay Test Setup,  
 Enable to Analog Out

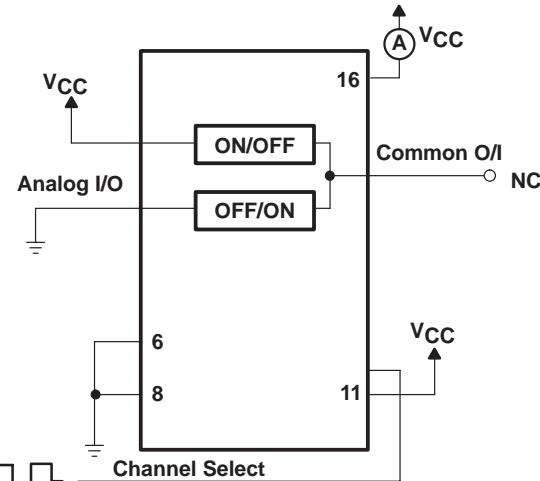


Figure 15. Power-Dissipation Capacitance Test Setup

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HC4851QDRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/Level-1-235C-UNLIM
SN74HC4851QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

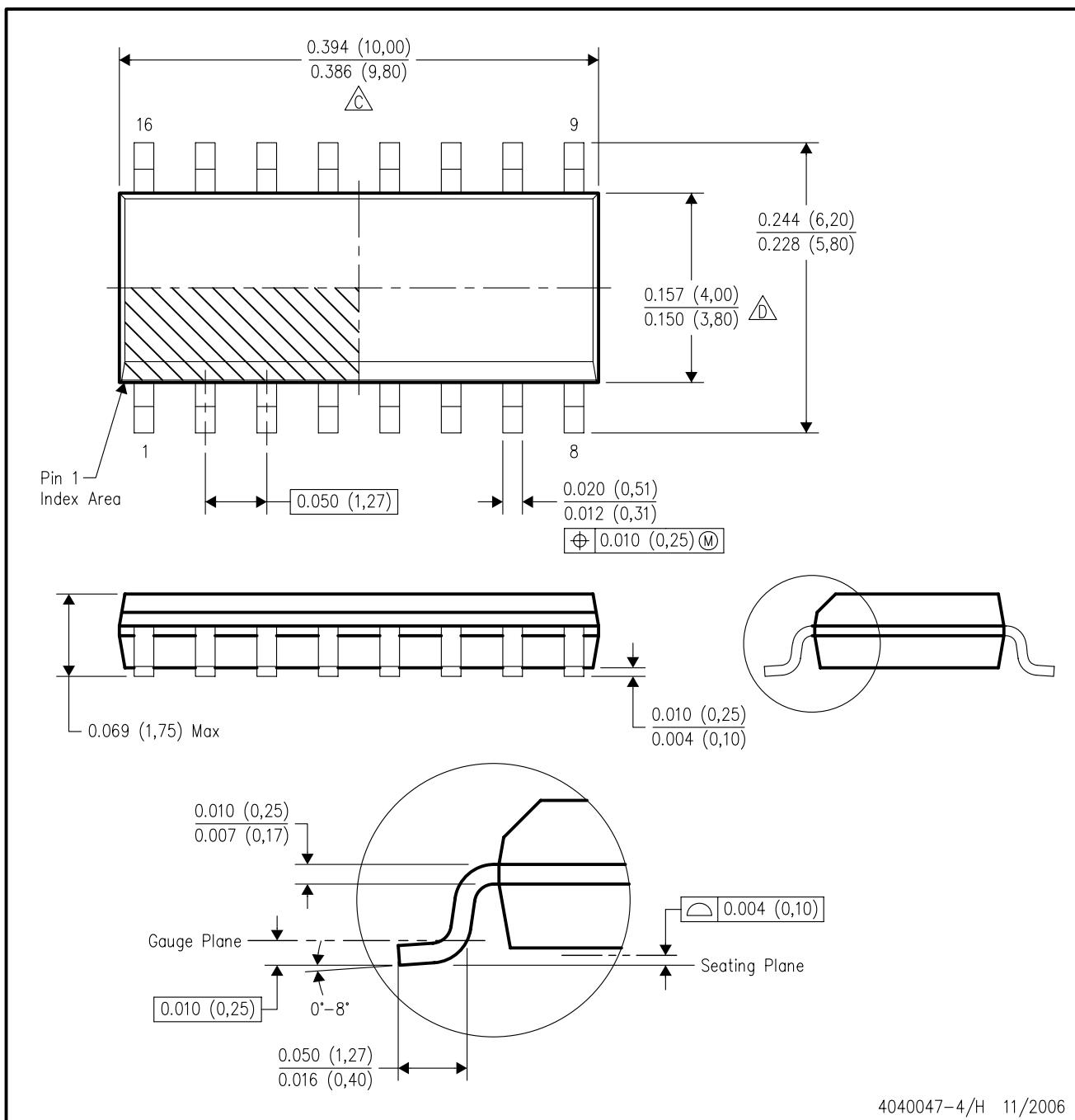
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## MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

 D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.

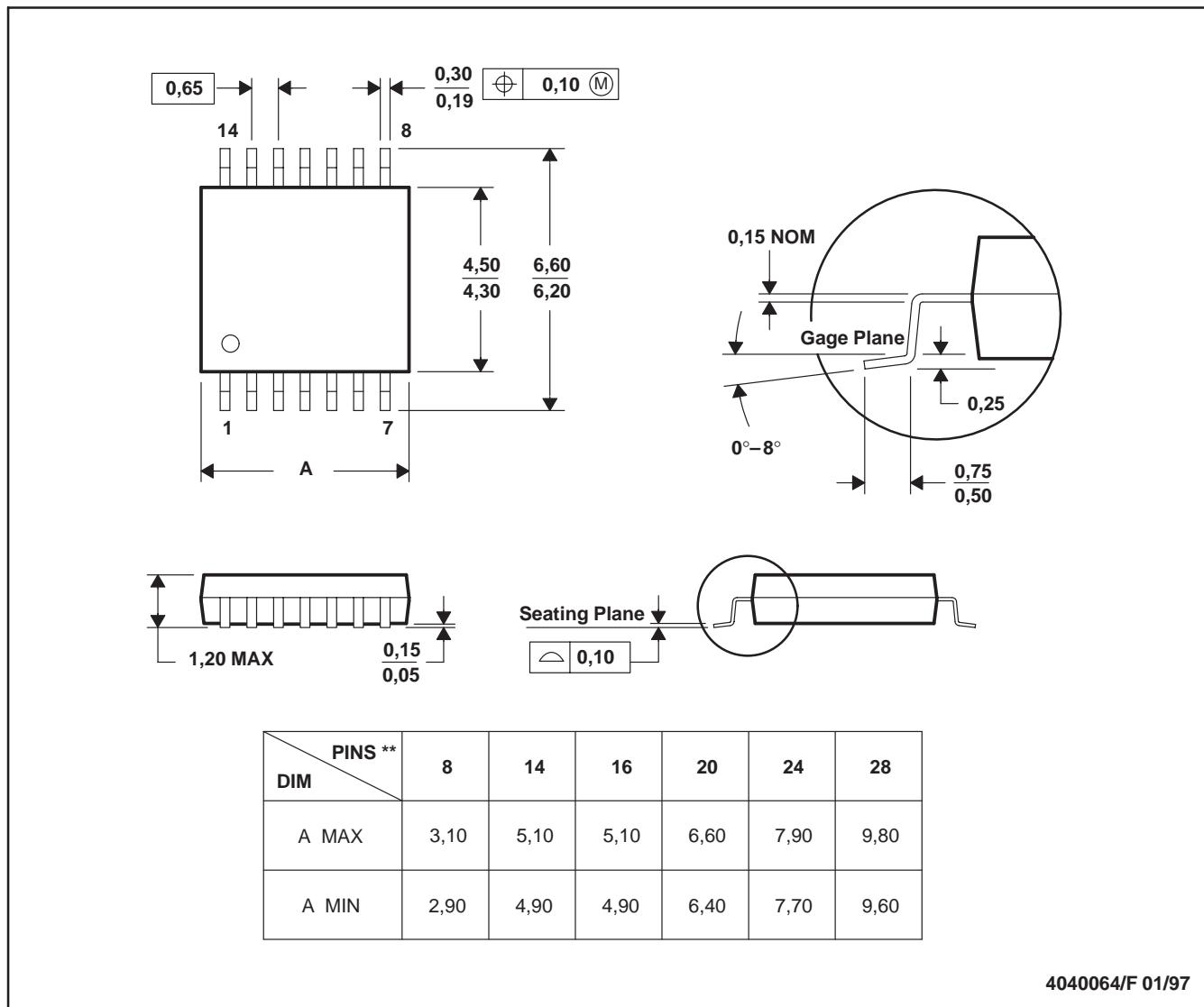
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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