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Port Bypass Circuits for Fibre Channel Arbitrated Loop Standard and its Extensions

Technical Data

HDMP-0421 Single PBC & CDR

Features

- **Supports ANSI X3T11 1.0625 Gbps FC-AL Loop Configuration**
- **Supports 802.3z 1.25 Gbps Gigabit Ethernet (GE) Rates**
- **Single PBC, CDR, Dual Signal Detect (SD) in a Single Package**
- **Bidirectional, Symmetric Bypass Capability**
- **CDR in Bypass Path and Loop Path**
- **CDR Location Determined by Wiring Configuration of Pins on PCB (Patent Pending)**
- **Envelope Detect on Cable Input (SD) for Both Directions**
- **Equalizers On All Inputs**
- **High Speed PECL I/Os Referenced to V_{CC}**
- **Buffered Line Logic (BLL) Outputs without External Bias Resistors**
- **0.4 W Typical Power at V_{CC} = 3.3 V**
- **5 V Tolerant LVTTL I/O**
- **24 Pin SSOP Package**

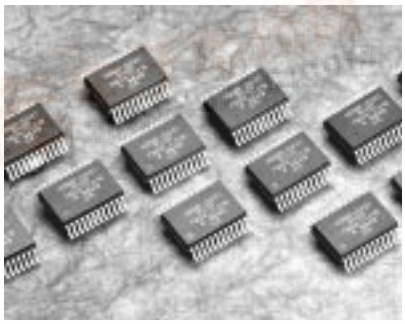
Applications

- **RAID, JBOD Cabinets**
- **1=>1 Gigabit Serial Buffer Pair (with and w/o CDR)**
- **Multi-Initiator Loops**

Description

The HDMP-0421 is a Single Port Bypass Circuit (PBC) with Clock and Data Recovery (CDR), and dual Signal Detect (SD) capability. This configuration will control jitter accumulation while repeating incoming signals. Port Bypass Circuits are used to provide loops that are continuously on in hard disk arrays constructed in Fibre Channel Arbitrated Loop (FC-AL) configurations. Hard disks may be pulled out or swapped while other disks in the array are available to the system. This device may also be used in multi-initiator loop configurations.

A Port Bypass Circuit is a 2:1 Multiplexer array with two modes of operation: DISK IN LOOP and DISK BYPASSED. In DISK IN LOOP mode, the loop goes into and out of the disk drive. Data go from the HDMP-0421's TO_NODE[n]± differential output pins to the Disk Drive Transceiver IC (for example, an HDMP-1536A) Rx± differential input pins. Data from the Disk Drive Transceiver IC Tx± differential output pins go to the HDMP-0421's FM_NODE[n]± differential input pins. Figures 4 and 5 show connection diagrams for disk drive array applications. In DISK BYPASSED mode, the disk drive is either absent or non-functional and the loop bypasses the hard disk. DISK IN LOOP mode is



enabled with a HIGH on the BYPASS[n]– pin and DISK BYPASSED mode is enabled with a LOW on the same pin.

Multiple HDMP-0421s may be cascaded or connected to other members of the HDMP-04xx family through the FM_LOOP and TO_LOOP pins to create loops for arrays of disk drives. See Table 2 to identify which of the two cells (0:1) will provide FM_LOOP, TO_LOOP pins (cell connected to cable). ALL TO_NODE outputs of the HDMP-0421 are of equal strength. Combinations of HDMP-04xx may be utilized to accommodate any number of hard disks.

The HDMP-0421 may also be used as a pair of 1=>1 buffers, one with a CDR and another without. For example, HDMP-0421 may be placed in front of a CMOS ASIC to clean the jitter of the outgoing signal (CDR path) and to better read the incoming signal (CDR-less path).

The design of the HDMP-0421 allows for placement of the CDR at one of two locations with respect to a hard disk slot. For example, if the BYPASS[0]– pin is HIGH and hard disk slot A is connected to PBC cell 1, the CDR function will be performed before entering the hard disk at slot A (Figure 4). To achieve a CDR function after slot A, the BYPASS[1]– pin must be HIGH and hard disk slot A must be connected to PBC cell 0 (Figure 5). Table 2 shows both possible connections. In both cases, a Signal Detect (SD) pin shows the status of the signal at the incoming cable. The recommended method of setting the BYPASS[i]– pins HIGH is to drive them with a high-impedence signal. Internal pull-up resistors will force the BYPASS[I]– pins to V_{CC}.

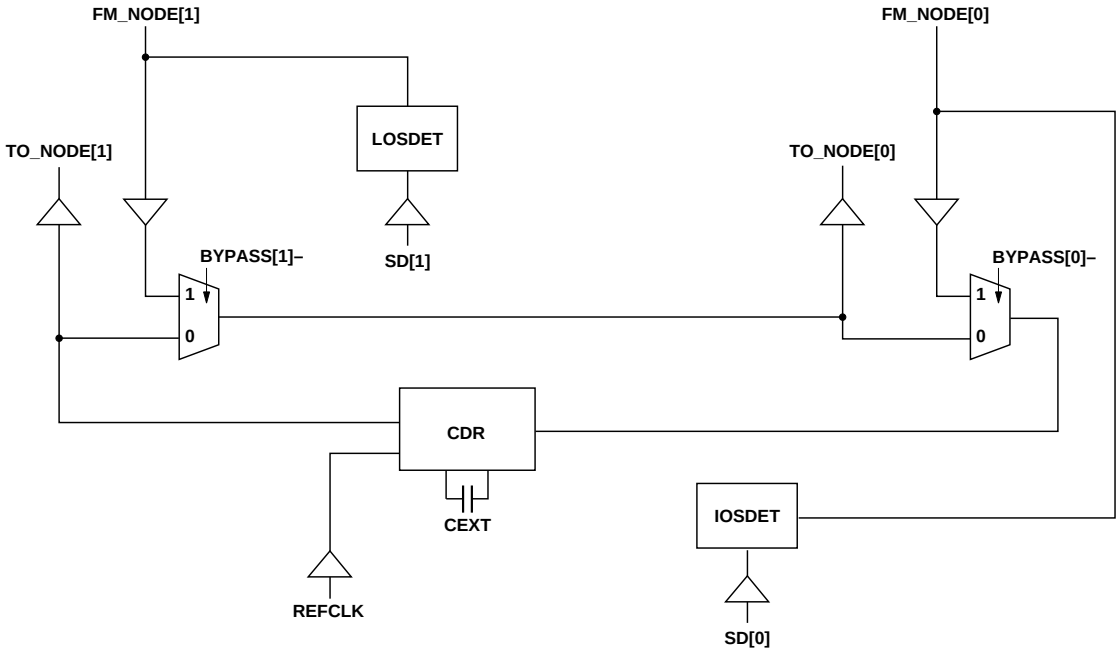


Figure 1. Block Diagram of HDMP-0421.

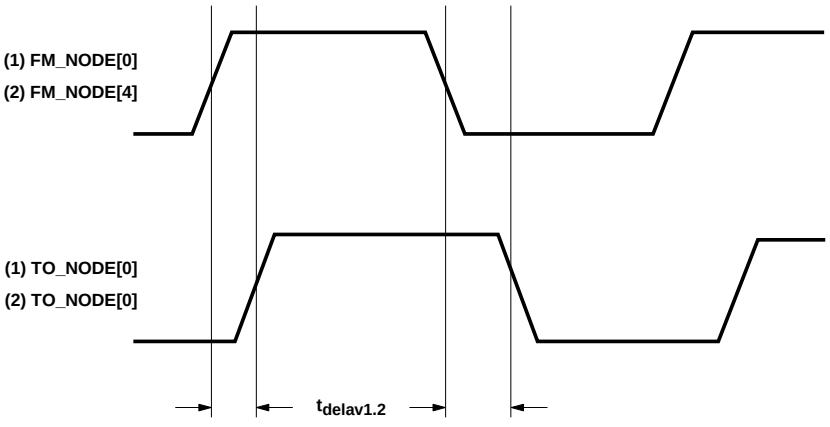


Figure 2. Timing Waveforms.

Table 1a. Truth Table for CDR at Entry Configurations

FM_LOOP = FM_NODE[0], TO_LOOP = TO_NODE[0], BYPASS[0]– = 1

TO_LOOP	TO_NODE[1]	BYPASS[1]–
FM_LOOP	FM_LOOP	0
FM_NODE[1]	FM_LOOP	1

Table 1b. Truth Table for CDR at Exit Configurations

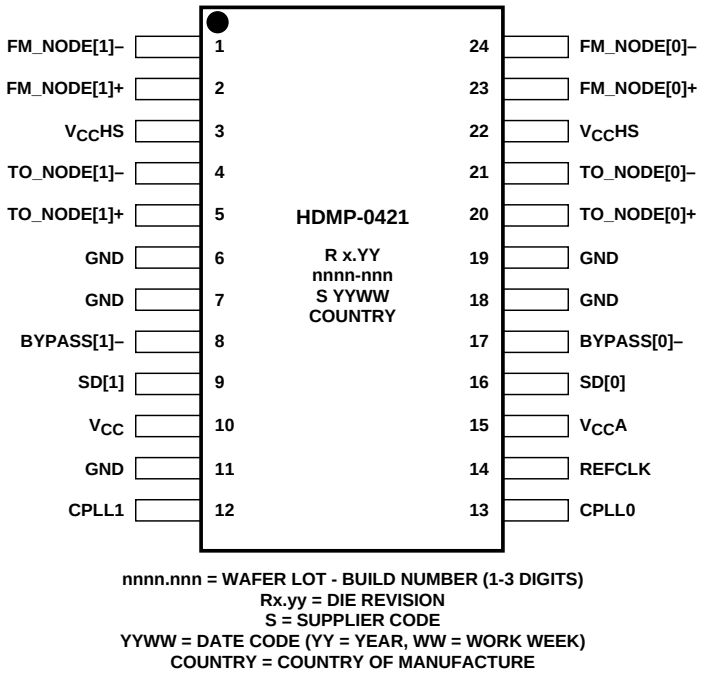
FM_LOOP = FM_NODE[1], TO_LOOP = TO_NODE[1], BYPASS[1]– = 1

TO_LOOP	TO_NODE[0]	BYPASS[0]–
FM_LOOP	FM_LOOP	0
FM_NODE[0]	FM_LOOP	1

Table 2. Pin Connection Diagram to Achieve Desired CDR Location (see Figures 4 and 5)

X Denotes CDR Position with respect to Hard Disks

Hard Disk	A	A
Connection to PBC Cells	1	0
CDR Position (x)	xA	Ax
Cell Connected to Cable	0	1



nnnn.nnn = WAFER LOT - BUILD NUMBER (1-3 DIGITS)
Rx.yy = DIE REVISION
S = SUPPLIER CODE
YYWW = DATE CODE (YY = YEAR, WW = WORK WEEK)
COUNTRY = COUNTRY OF MANUFACTURE

Figure 3: HDMP-0421 Package Layout and Marking, Top View.

Table 3. Pinout

Pin Name	Pin	Pin Type	Pin Description
TO_NODE[0]+	20	O-PECL	In CDR at entry configuration, this pin is the Serial Output (TO_LOOP+). In other configurations, this pin is wired to the hard disk.
TO_NODE[0]–	21	O-PECL	In CDR at entry configuration, this pin is the Serial Output (TO_LOOP–). In other configurations, this pin is wired to the hard disk.
FM_NODE[1]+	02	I-PECL	Input from Transceiver IC to Cell 1.
FM_NODE[1]–	01	I-PECL	Input from Transceiver IC to Cell 1.
TO_NODE[1]+	05	O-PECL	Output to Transceiver IC from Cell 1.
TO_NODE[1]–	04	O-PECL	Output to Transceiver IC from Cell 1.
FM_NODE[0]+	23	I-PECL	In CDR at entry configuration, this pin is the Serial Input (FM_LOOP+). In other configurations, this pin is wired to the hard disk.
FM_NODE[0]–	24	I-PECL	In CDR at entry configuration, this pin is the Serial Input (FM_LOOP–). In other configurations, this pin is wired to the hard disk.
BYPASS[1]–	08	I-LVTTL	Bypass pin for cell 1. In CDR at exit configuration, float to HIGH else ground connect through a 1 KΩ resistor.
BYPASS[0]–	17	I-LVTTL	Bypass pin for cell 0. In CDR at exit configuration, float to HIGH else ground connect through a 1 KΩ resistor.
REFCLK	14	I-LVTTL	Reference Clock Input for Clock and Data Recovery (CDR) circuit.
CPLL1	12	C	PLL cap pin. Connected to pin 13 with a 0.1 microFarad capacitor.
CPLL0	13	C	PLL cap pin. Connected to pin 12 with a 0.1 microFarad capacitor.
SD[1] SD[0]	09 16	O-LVTTL	Signal Detect via envelope detect method. In CDR at entry and at exit cases, detects signal on incoming cable respectively. Active High when signal is detected. If (FM_NODE[0]+ –FM_NODE[0]–) >= 400 mV peak-to-peak, SD = 1 If 400 mV >= (FM_NODE[0]+ –FM_NODE[0]–) >= 100 mV, SD = unpredictable If 100 mV >= (FM_NODE[0]+ –FM_NODE[0]–), SD = 0
GND		S	6, 7, 11, 18, 19 Ground pins.
V_{CC}A	15	S	Analog Power Supply pin.
V_{CC}HS	03 22	S S	Cell 1 High Speed Output Pins Power Supply. Cell 0 High Speed Output Pins Power Supply.
V_{CC}	10	S	Logic Power Supply pins.

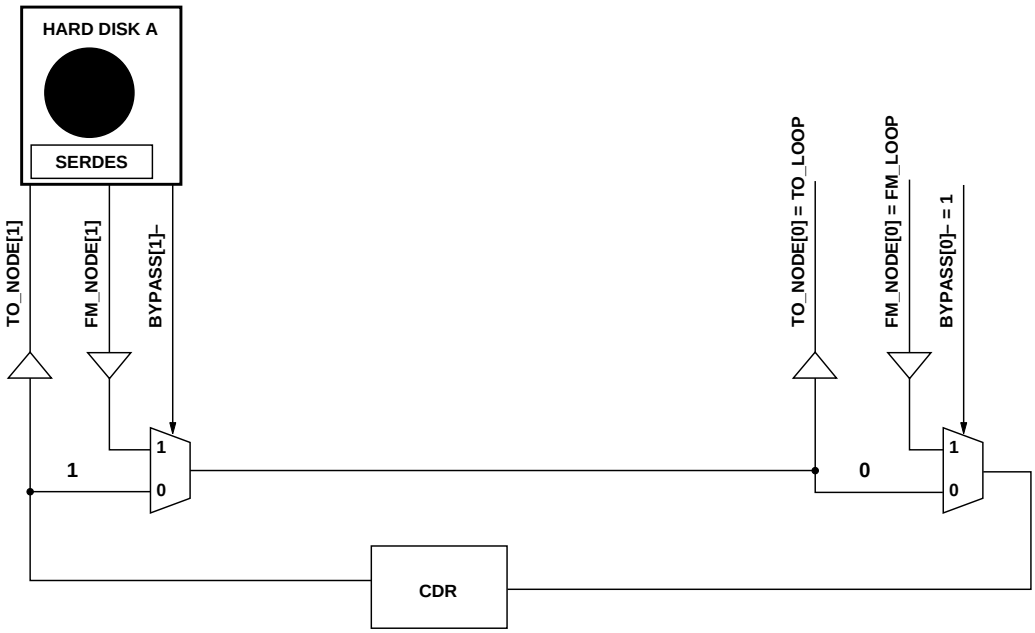


Figure 4: Connection Diagram. Case of CDR Before Entering the Hard Disk.

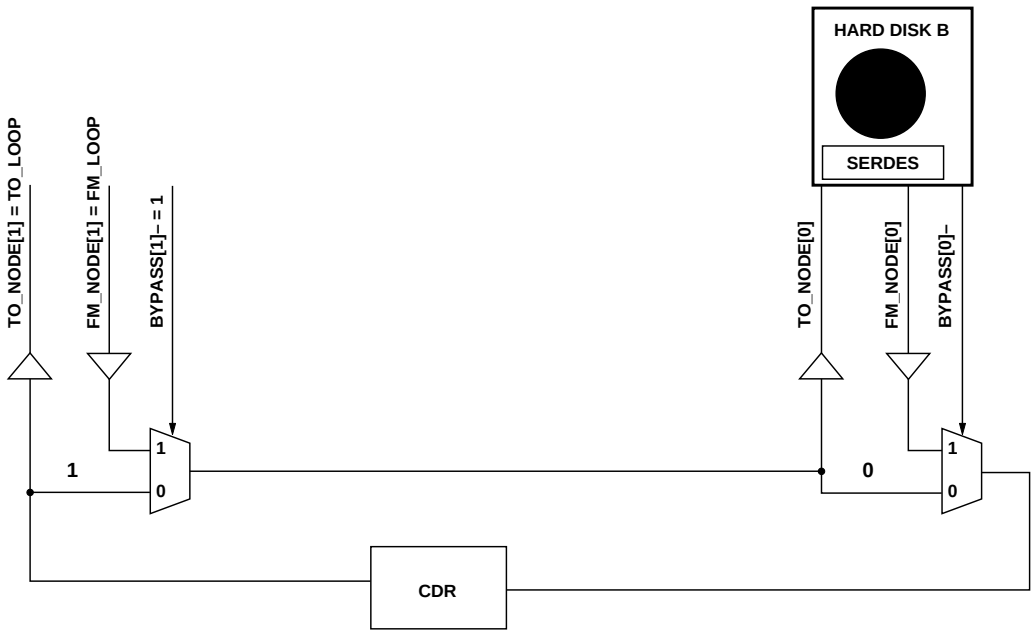


Figure 5: Connection Diagram. Case of CDR After Exiting the Hard Disk.

Absolute Maximum Ratings

T_A = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Min.	Max.
V_{CC}	Supply Voltage	V	–0.7	4.0
$V_{IN,LVTTL}$	LVTTL Input Voltage	V	–0.7	4.0
V_{IN,HS_IN}	HS_IN Input Voltage	V	2.0	V_{CC}
$I_{O,LVTTL}$	LVTTL Output Source Current	mA		± 13
T_{stg}	Storage Temperature	°C	–65	+150
T_j	Junction Temperature	°C	0	+125

Guaranteed Operating Rates

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Serial Clock Rate FC (MBd)		Serial Clock Rate GE (MBd)	
Min.	Max.	Min.	Max.
1040	1080	1240	1260

Clock and Data Recovery Circuit Reference Clock Requirements

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.	Min.	Typ.	Max.
f	Nominal Frequency	MHz		106.25			125.00	
F_{tol}	Frequency Tolerance	ppm	–100		+100	–100		+100
Symm	Symmetry (Duty Cycle)	%	40		60	40		60

DC Electrical Specifications

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
$V_{IH,LVTTL}$	LVTTL Input High Voltage Range	V	2		4.0
$V_{IL,LVTTL}$	LVTTL Input Low Voltage Range	V	0		0.8
$V_{OH,LVTTL}$	LVTTL Output High Voltage Level, I_{OH} = –400 µA	V	2.2		3.45
$V_{OL,LVTTL}$	LVTTL Output Low Voltage Level, I_{OL} = 1 mA	V	0		0.6
$I_{IH,LVTTL}$	Input High Current (Magnitude), V_{IN} = 2.4 V, V_{CC} = 3.45 V	µA		0.003	40
$I_{IL,LVTTL}$	Input Low Current (Magnitude), V_{IN} = 0.4 V, V_{CC} = 3.45 V	µA		300	600
I_{CC}	Total Supply Current, T_A = 25°C	mA		110	

AC Electrical Specifications

T_A= 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Units	Min.	Typ.	Max.
t_{delay1}	Total Loop Latency from FM_NODE[0] to TO_NODE[0]	ns		4.0	
t_{delay2}	Per Cell Latency from FM_NODE[4] to TO_NODE[0]	ns		2.0	
$t_{r,LVTTLin}$	Input LVTTL Rise Time Requirement, 0.8 V to 2.0 V	ns		2.0	
$t_{f,LVTTLin}$	Input LVTTL Fall Time Requirement, 2.0 V to 0.8 V	ns		2.0	
$t_{r,LVTTLout}$	Output LVTTL Rise Time Range, 0.8 V to 2.0 V, 10 pF Load	ns		1.5	2.4
$t_{f,LVTTLout}$	Output LVTTL Fall Time Range, 2.0 V to 0.8 V, 10 pF Load	ns		2.0	3.5
$t_{rs,\ HS\_OUT}$	HS_OUT Single-Ended Rise Time	ps		200	350
t_{fs,HS_OUT}	HS_OUT Single-Ended Fall Time	ps		200	350
$t_{rd,\ HS\_OUT}$	HS_OUT Differential Rise Time	ps		200	350
t_{fd,HS_OUT}	HS_OUT Differential Fall Time	ps		200	350
V_{IP,HS_IN}	HS_IN Input Peak-To-Peak Required Differential Voltage Range	mV	200	1200	2000
V_{OP,HS_OUT}	HS_OUT Output Peak-To-Peak Differential Voltage (Z0=750 Ω, Figure 10)	mV	1100	1400	2000

Power Dissipation and Thermal Resistance

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Typ.	Max.
P_D	Power Dissipation	mW	360	
Θ_{jc}	Thermal Resistance, Junction to Case	°C/W	14	

Output Jitter Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Unit	Typ.	Max.
RJ	Random Jitter at TO_NODE pins (1 sigma rms)	ps	6	
DJ	Deterministic Jitter at TO_NODE pins (pk-pk)	ps	16	

Note:
Please refer to Figures 7 and 8 for jitter measurement setup information.

Locking Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Parameter	Unit	Max.
Bit Sync Time (phase lock)	bits	2500
Frequency Lock at Powerup	μs	500

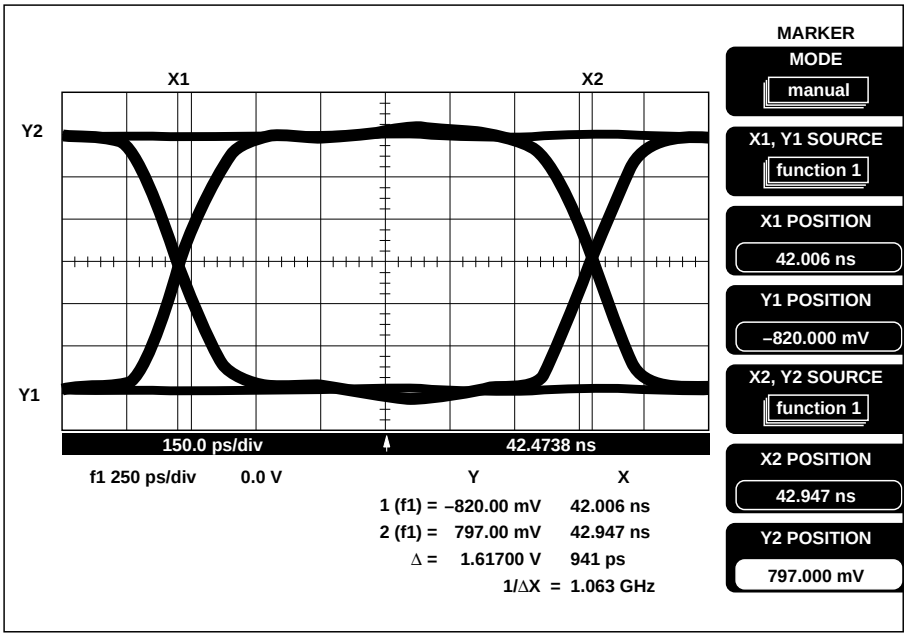


Figure 6. Eye Diagram of a High Speed Differential Output.

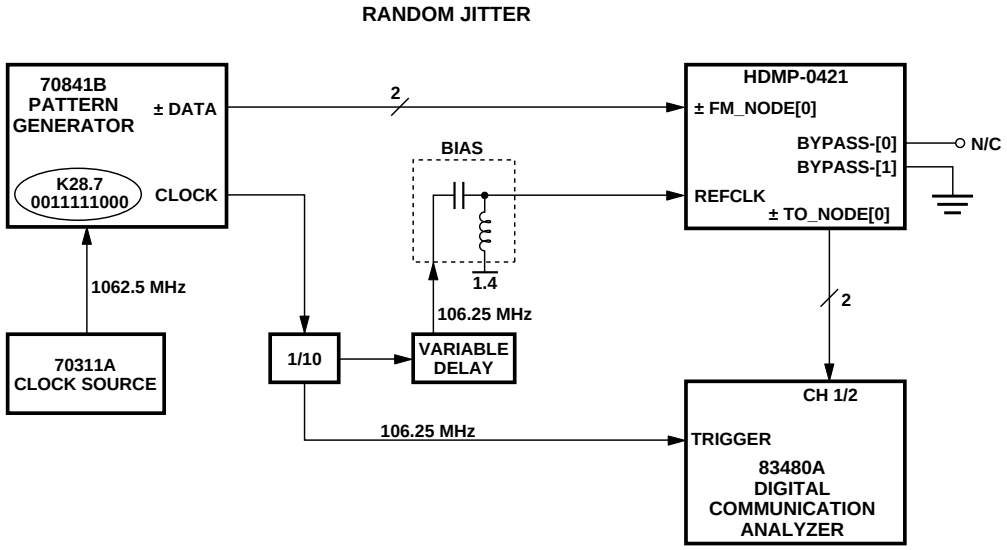


Figure 7. Setup for Measurement of Random Jitter.

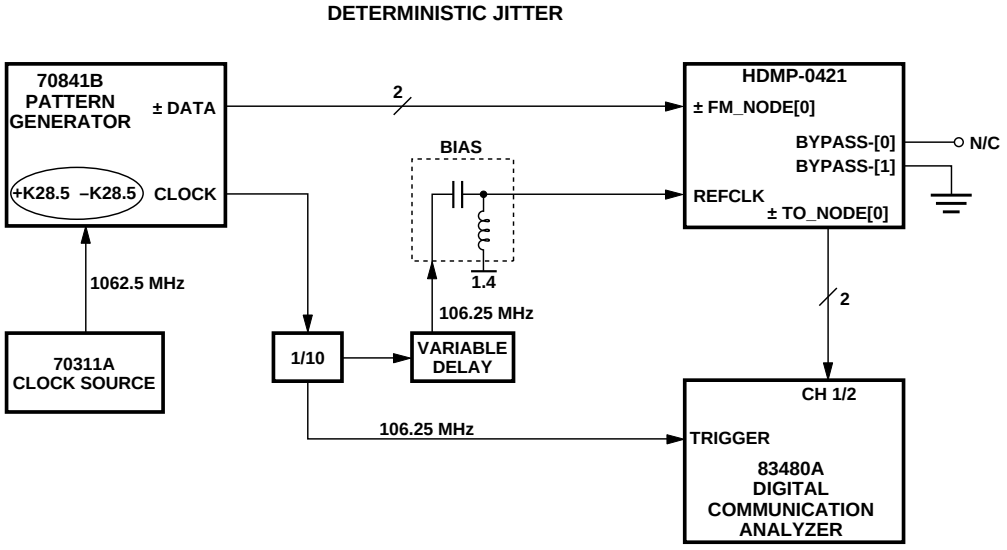


Figure 8. Setup for Measurement of Deterministic Jitter.

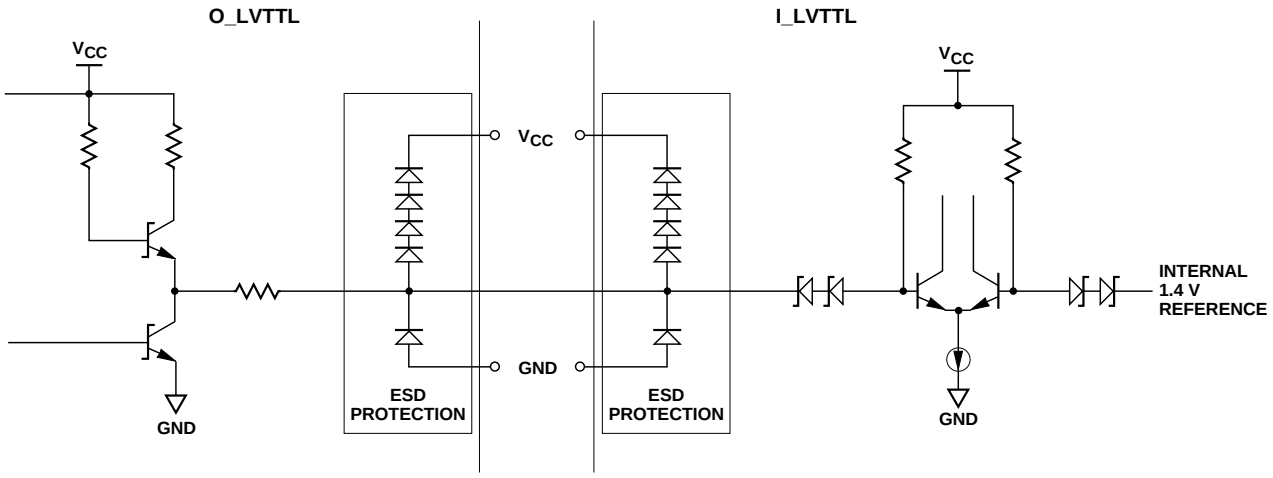


Figure 9. O-LVTTL and I-LVTTL Simplified Circuit Schematic.

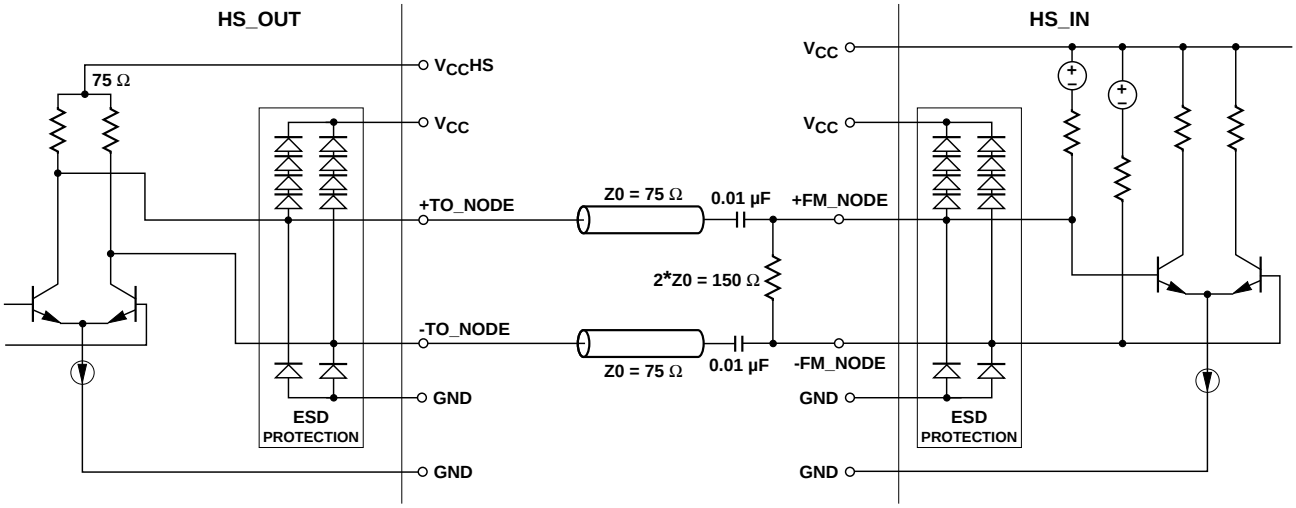
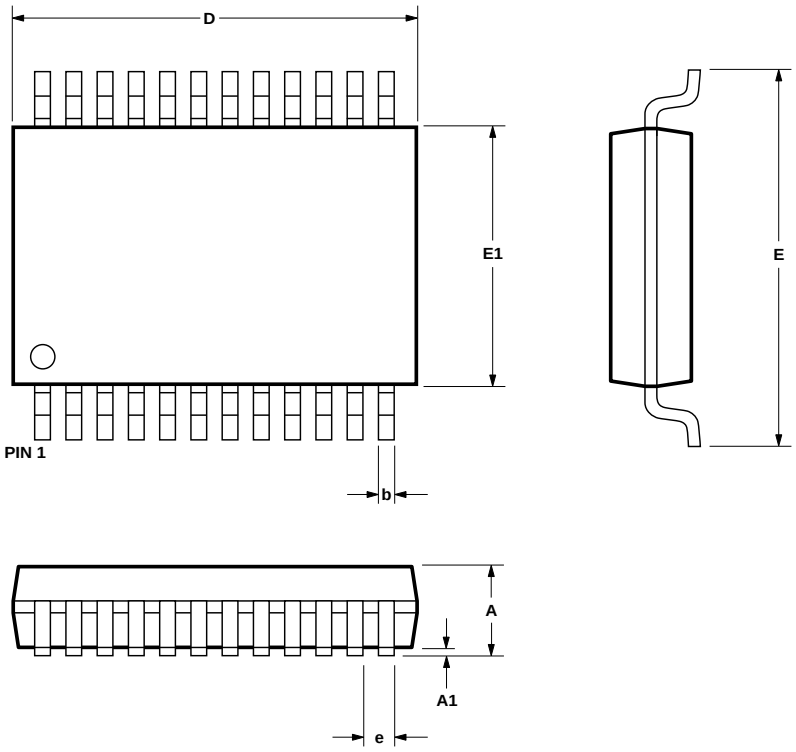


Figure 10. O-PECL and I-PECL Simplified Circuit Schematic.



DIMENSION	A	A1	D	E	E1	e	b	LEAD COPLANARITY
VALUE	2.00	0.05/0.21	8.20	7.80	5.30	0.65	0.30	0.10
TOLERANCE	MAX.	MIN./MAX.	±0.05	±0.10	±0.10	BASIC	±0.05	MAX.

ALL DIMENSIONS ARE IN MILLIMETERS

Figure 11. HDMP-04221 Package Drawings.

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