HD66113T

(120-Channel Common Driver Packaged
in a Slim Tape Carrier Package)

HITACHI

Description

The HD66113T is a common driver for large dot matrix liquid crystal graphics displays. It features 120 channels which can be divided into two groups of 60 channels by selecting data input/output pins. The driver is powered by about 3V, making it suitable for the design of portable equipment which fully utilizes the low power dissipation of liquid crystal elements. The HD66113T, packaged in a slim tape carrier package (slim-TCP), makes it possible to reduce the size of the user area (wiring area).

Features

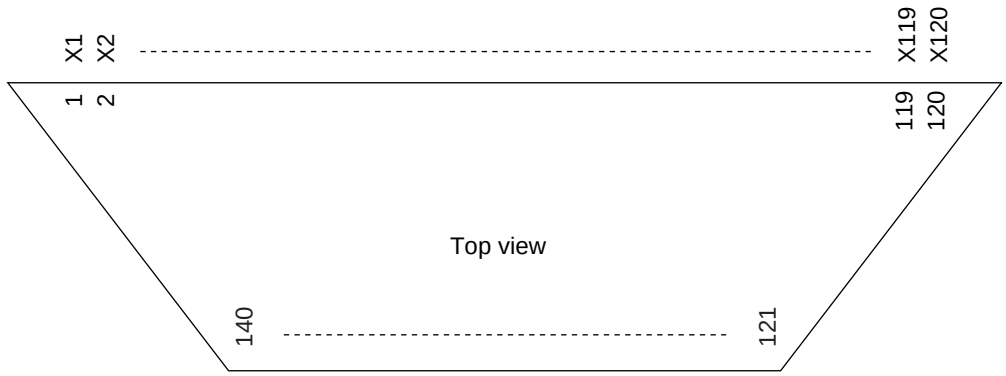
- Duty cycle: About 1/100 to 1/480
- 120 LCD drive circuits
- High LCD driving voltage: 14V to 40V
- Output division function (2 × 60-channel outputs)
- Display off function
- Operating voltage: 2.5V to 5.5V
- Slim-TCP
- Low output impedance: 0.7 kΩ (typ)

Ordering Information

Type No.	Outer Lead Pitch (μm)
HD66113TA0	190
HD66113TA1	240

Note: The details of TCP pattern are shown in „The Information of TCP.“

Pin Arrangement



Note: This figure does not specify the tape carrier package dimensions.

Pin Assignments

VLCD1	V1L	V6L	V5L	V2L	GND	DIO1	M	$\overline{\text{DISPOFF}}$	SHL	CH	DI	CL	DIO2	V_{CC}	V2R	V5R	V6R	V1R	VLCD2
140	139	138	137	136	135	134	133	132	131	130	129	128	127	126	125	124	123	122	121

Pin Descriptions

Symbol	Pin No.	Pin Name	Input/Output	Classification
VLCD1, 2	140, 121	VLCD	—	Power supply
V_{CC}	126	V_{CC}	—	Power supply
GND	135	GND	—	Power supply
V1L, V1R	139, 122	V1	Input	Power supply
V2L, V2R	136, 125	V2	Input	Power supply
V5L, V5R	137, 124	V5	Input	Power supply
V6L, V6R	138, 123	V6	Input	Power supply
CL	128	Clock	Input	Control signal
M	133	M	Input	Control signal
CH	130	CH	Input	Control signal
SHL	131	Shift left	Input	Control signal
DIO1	134	Data	Input/output	Control signal
DIO2	127	Data	Input/output	Control signal
DI	129	Data	Input	Control signal
$\overline{\text{DISPOFF}}$	132	Display off	Input	Control signal
X1–X120	1–120	X1–X120	Output	LCD drive output

Pin Functions

Power Supply

V_{CC}, GND: Supply power to the internal logic circuits.

VLCD, GND: Supply power to the LCD drive circuits (Figure 1).

V1L, V1R, V2L, V2R, V5L, V5R, V6L, V6R: Supply different power levels to drive the LCD. V1 and V2 are selected levels, and V5 and V6 are non-selected levels.

Control Signals

CL: Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts data input via the DIO pins.

M: Changes the LCD drive outputs to AC.

CH: Selects the data shift mode. (CH = high: 2 × 60-output mode, CH = low: 120-output mode)

SHL: Selects the data shift direction for the shift register and the common signal scan direction (Figure 2).

DIO1, DIO2: Input or output data. DIO1 is input and DIO2 is output when SHL is high. DIO1 is output and DIO2 is input when SHL is low.

DI: Input data. DI is input to X61–X120 when CH and SHL are high, and to X60–X1 when SHL is low.

$\overline{\text{DISPOFF}}$: Controls LCD output level. A low $\overline{\text{DISPOFF}}$ sets the LCD drive outputs X1–X120 to the V2 level. A high $\overline{\text{DISPOFF}}$ is normally used.

LCD Drive Outputs

X1–X120: Each X outputs one of four voltage levels V1, V2, V5, or V6, depending on the combination of the M signal and the data level (Figure 3).

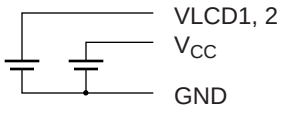


Figure 1 Power Supply for LCD Driver

SHL	Data shift direction
High	Shift to right DIO1 → SR1 → SR2 → SR3 • • • → SR120 → DIO2
Low	Shift to left DIO2 → SR120 → SR119 • • • → SR1 → DIO1

Note: SR1 to SR120 correspond to the outputs of X1 to X120, respectively.

Figure 2 Selection of Data Shift Direction and Common Signal Scan Direction by SHL

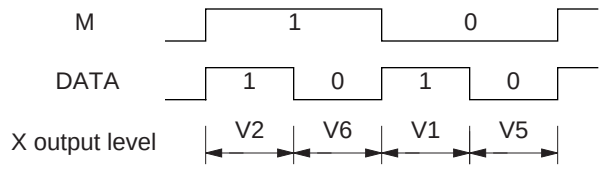
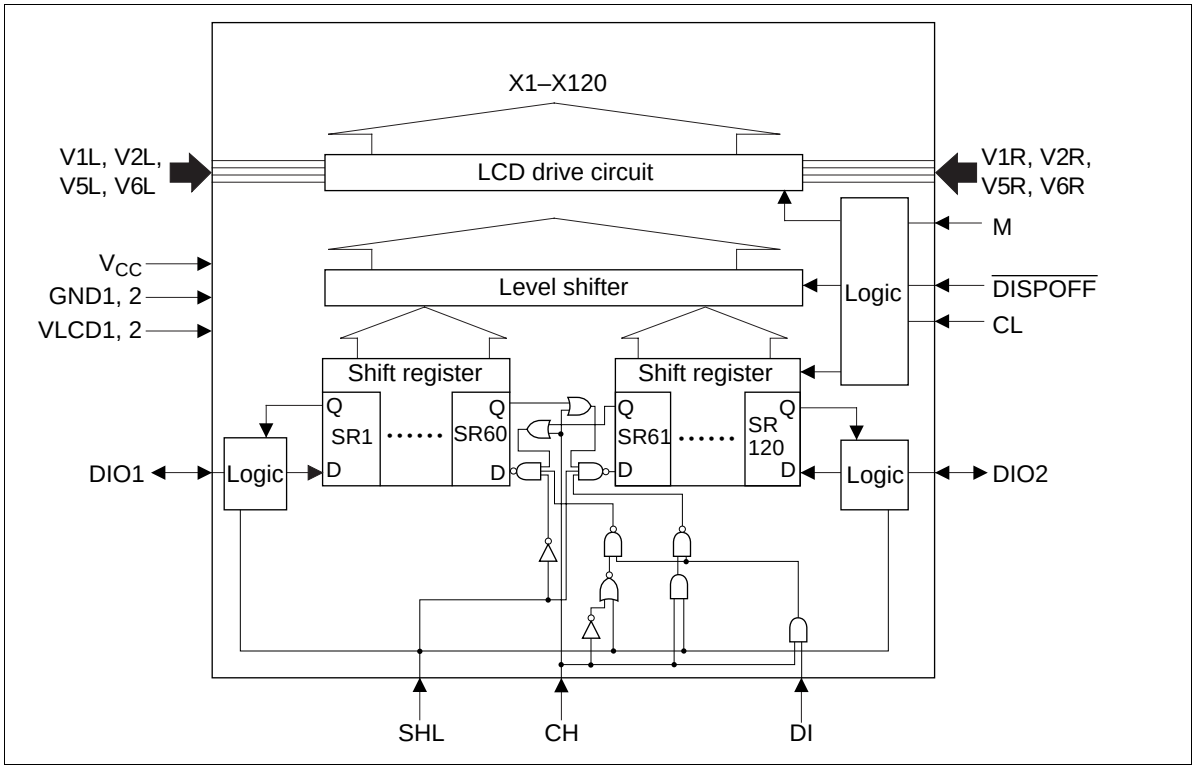


Figure 3 Selection of LCD Drive Output Level

Block Diagram



Block Functions

LCD Drive Circuit

The 120-bit LCD drive circuit generates four voltage levels V1, V2, V5, and V6, which drive the LCD panel. One of these four levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes logic control signals (2.5 V–5.5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 120-bit shift register shifts the data input via the DIO pin by one bit at a time. The one bit of shifted-out data is output from the DIO pin to the next driver IC. Both actions occur simultaneously at the falling edge of each shift clock (CL) pulse. The SHL pin selects the data shift direction.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	–0.3 to +7.0	V	1, 5
Power supply voltage for LCD drive circuits	VLCD	–0.3 to +42	V	1, 5
Input voltage 1	VT1	–0.3 to V_{CC} + 0.3	V	1, 2
Input voltage 2	VT2	–0.3 to VLCD + 0.3	V	1, 3
Input voltage 3	VT3	–0.3 to +7.0	V	1, 4
Operating temperature	T_{opr}	–30 to +75	°C	
Storage temperature	T_{stg}	–55 to +110	°C	

Notes: 1. The reference point is GND (0V).
2. Applies to pins CL, M, SHL, DI, $\overline{\text{DISPOFF}}$, and CH.
3. Applies to pins V1 and V6.
4. Applies to pins V2 and V5.
5. Power should be applied to V_{CC}–GND first, and then VLCD–GND. It should be disconnected in the reverse order.
6. If the LSI is used beyond its absolute maximum ratings, it may be permanently damaged.
   It should always be used within its specified operating range in order to prevent malfunctions or loss of reliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.5V to 5.5V, GND = 0V, and T_a = –30°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	VIH	1	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low voltage	VIL	1	0	—	$0.2 \times V_{CC}$	V		
Output high voltage	VOH	2	V_{CC} – 0.4	—	—	V	I_{OH} = –0.4 mA	
Output low voltage	VOL	2	—	—	0.4	V	I_{OL} = 0.4 mA	
Vi–Xj on resistance	R_{ON}	3	—	0.7	1.0	kΩ	I_{ON} = 150 mA	1
Input leakage current 1	I_{IL1}	1	–5	—	5	µA	VIN = V_{CC} to GND	
Input leakage current 2	I_{IL2}	4	–25	—	25	µA	VIN = VLCD to GND	
Current consumption 1	I_{GND}	—	—	—	0.5	mA	f_{CL} = 36 kHz f_M = 75 kHz	2
Current consumption 2	I_{LCD}	—	—	—	1.0	mA		

Note: Pins: 1. CL, M, SHL, CH, DI, DIO1, DIO2, $\overline{\text{DISPOFF}}$
2. DIO1, DIO2
3. X1–X120, V
4. V1, V2, V5, V6

Notes: 1. Indicates the resistance between one of the pins X1–X120 and one of the voltage supply pins V1, V2, V5, or V6, when load current is applied to the X pin; defined under the following conditions:

VLCD–GND = 40V

V1, V6 = V_{CC} – {1/20 (VLCD–GND)}

V5, V2 = GND + {1/20 (VLCD–GND)}

All voltages must be within ΔV, VLCD ≥ V1 ≥ V6 ≥ VLCD – 7.0V, and 7.0V ≥ V5 ≥ V2 ≥ GND.

Note that ΔV depends on the power supply voltage VLCD–GND (Figure 5).

2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, VIH and VIL must be held at V_{CC} and GND, respectively.

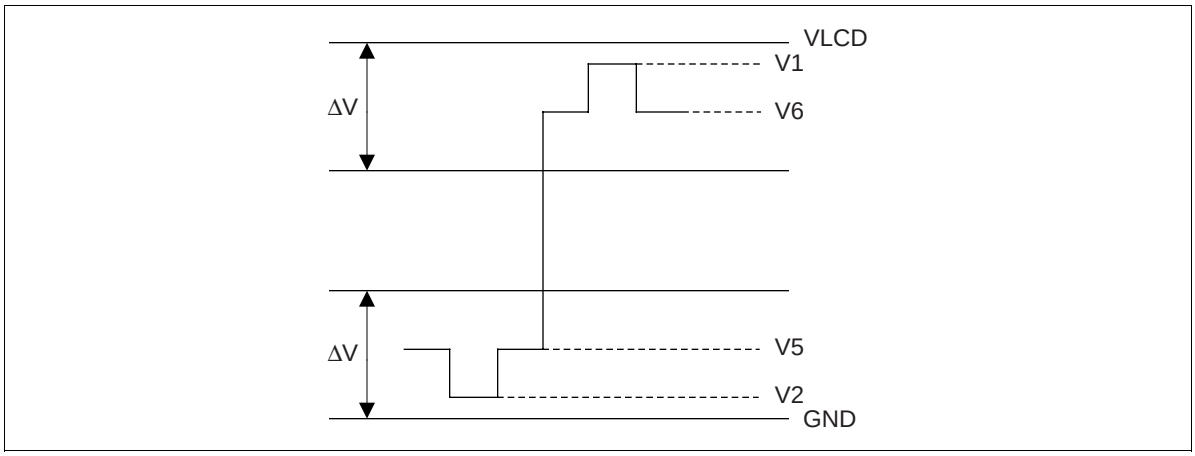


Figure 4 Relation between Driver Output Waveform and Voltage Levels

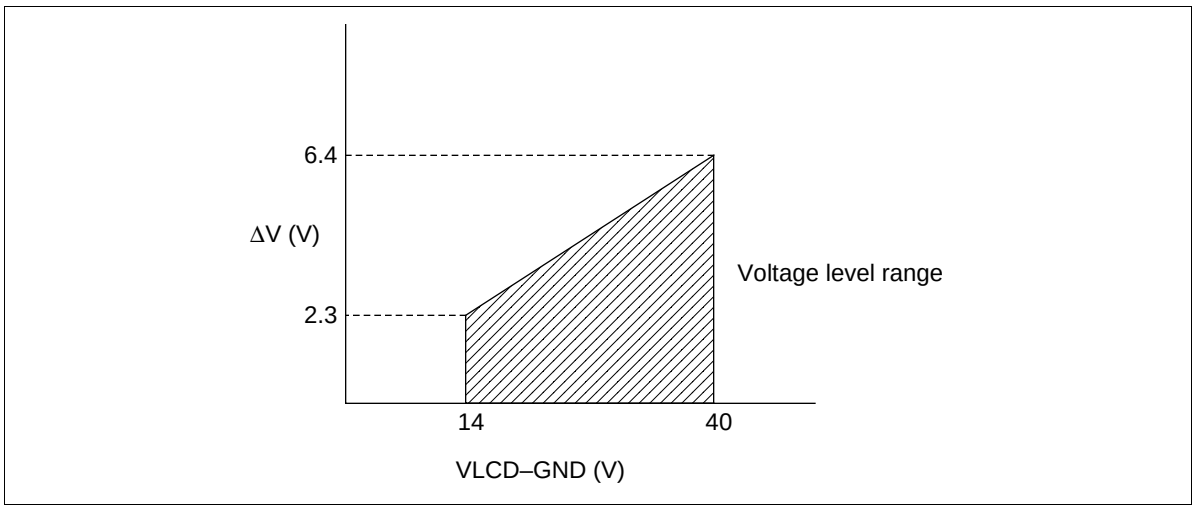


Figure 5 Relation between VLCD–GND and ΔV

AC Characteristics (V_{CC} = 2.5V to 5.5V, GND = 0V, and T_a = –30°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	1
Clock fall time	t_f	CL	—	30	ns	1
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	350	ns	2
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	1.2	µs	3
Output delay time 2	t_{pd2}	X (n), M	—	1.2	µs	3

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, and T_a = –30°C to +75°C, unless otherwise stated)

Item	Symbol	Pins	Min	Max	Unit	Notes
Clock cycle time	t_{CYC}	CL	400	—	ns	
Clock high-level width	t_{CWH}	CL	30	—	ns	
Clock low-level width	t_{CWL}	CL	370	—	ns	
Clock rise time	t_r	CL	—	30	ns	1
Clock fall time	t_f	CL	—	30	ns	1
Data setup time	t_{DS}	DI, DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DI, DIO1, DIO2, CL	30	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	150	ns	2
M phase difference	t_M	M, CL	–300	300	ns	
Output delay time 1	t_{pd1}	X (n), CL	—	0.7	µs	3
Output delay time 2	t_{pd2}	X (n), M	—	0.7	µs	3

Notes: 1. t_r, $t_f < (t_{cyc} - t_{CWH} - t_{CWL})/2$ and t_r, $t_f \leq 30$ ns

2, 3 The load circuit shown in Figure 6 is connected.

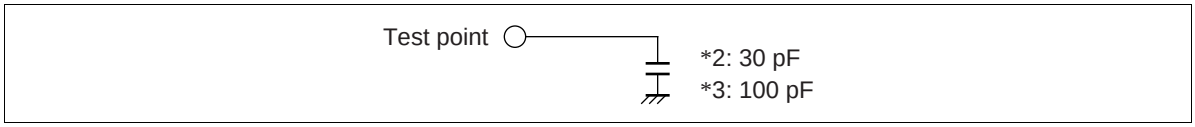


Figure 6 Load Circuit

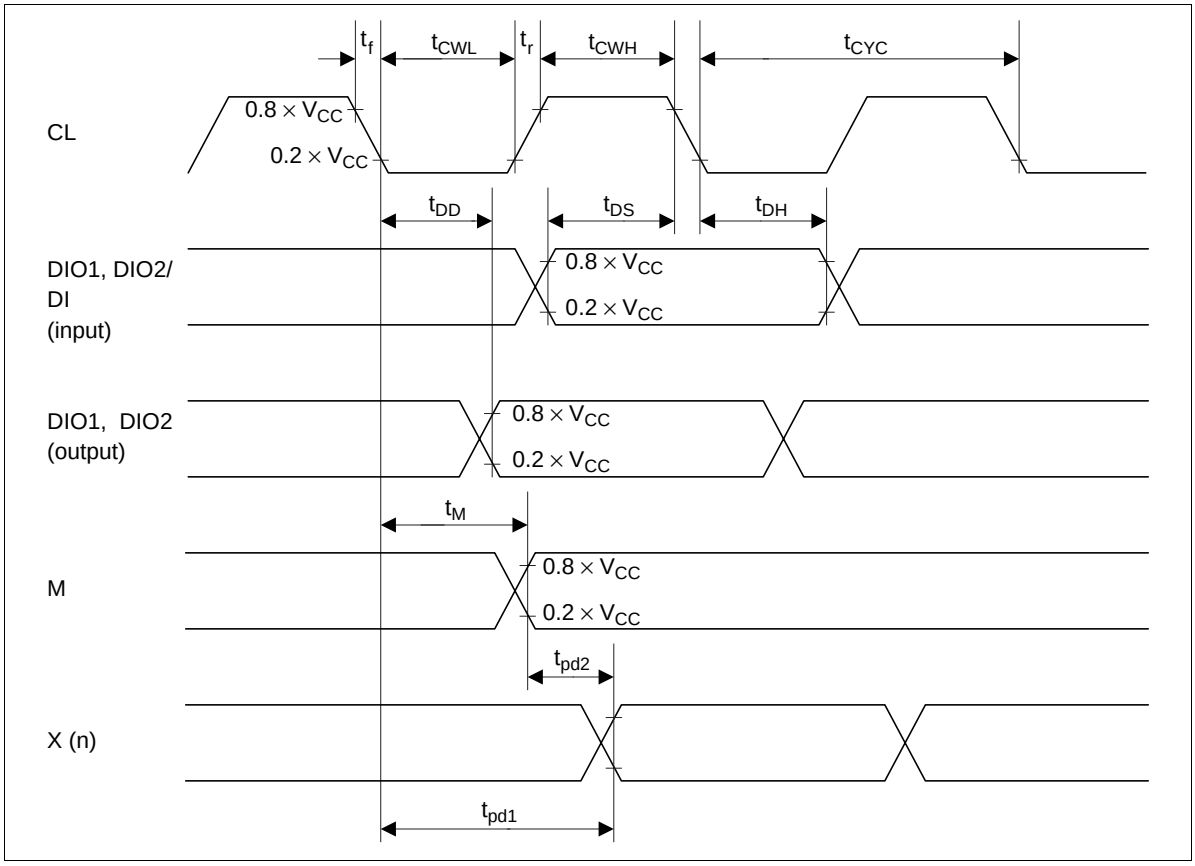
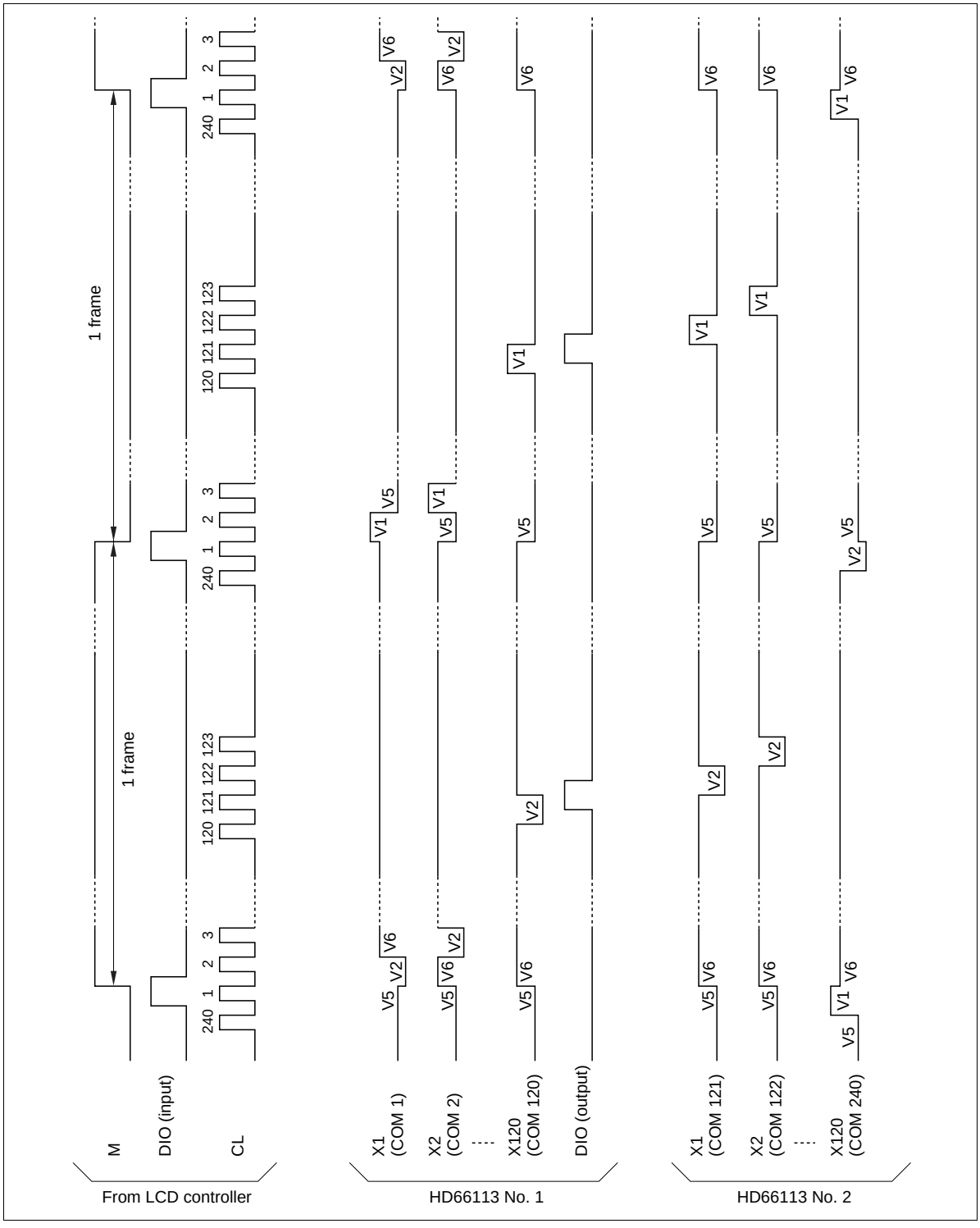


Figure 7 LCD Controller Interface Timing

Operation Timing (1/240 Duty Cycle)



Connection Examples

Figures 8 and 9 show examples of how HD66113Ts can be configured to drive a 600-line LCD panel with a 1/300 duty cycle. Figures 10 and 11 show examples of how HD66113Ts can be configured to drive a 240-line LCD panel with a 1/240 duty cycle. The HD66113T's 120 channels can be divided into two groups of 60 channels, and its data shift direction can be changed by selecting the data output mode pin (CH) and data shift pin (SHL), respectively.

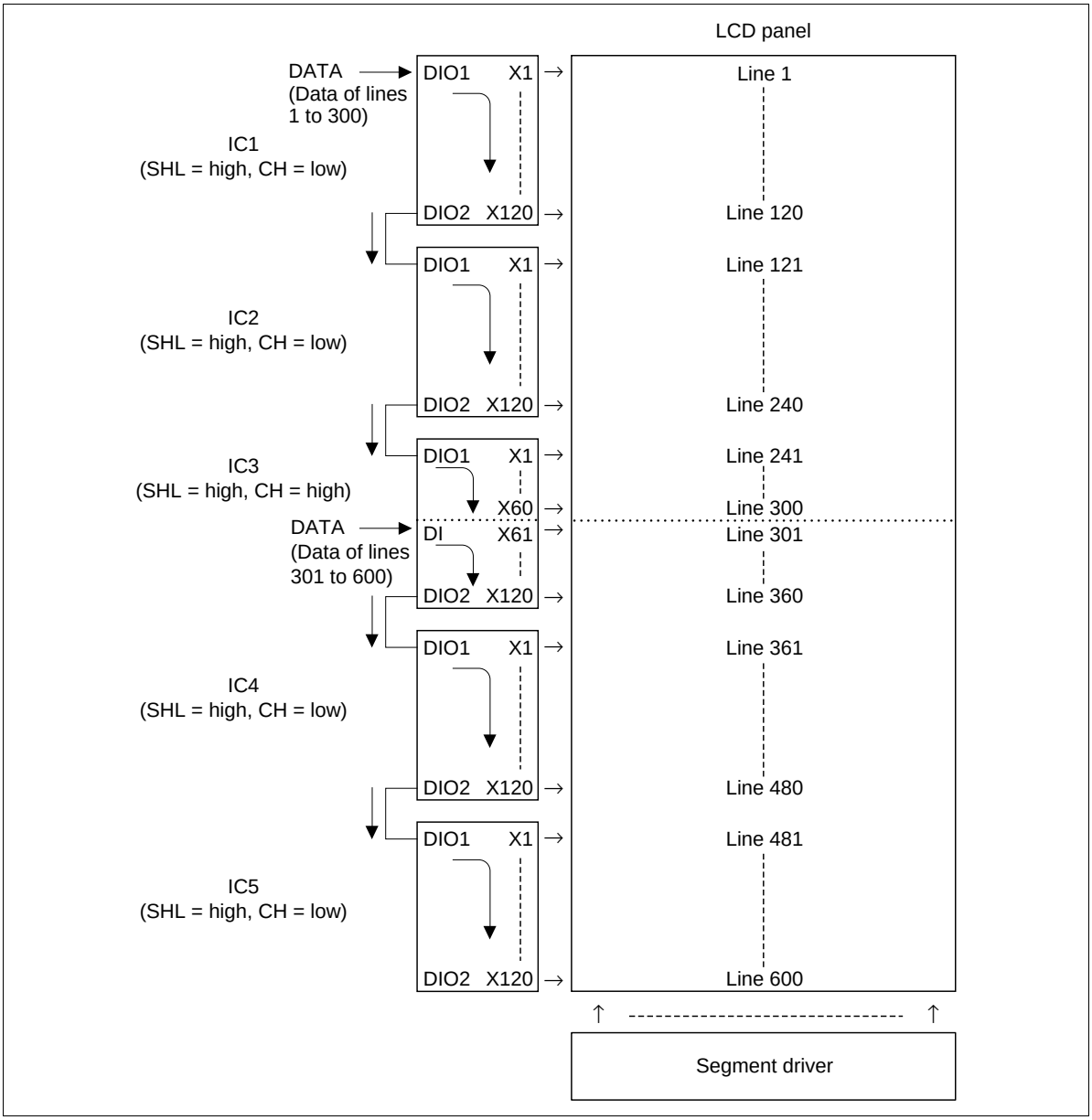


Figure 8 Dual-Screen Configuration of a 600-Line LCD Panel with a 1/300 Duty Cycle (1)

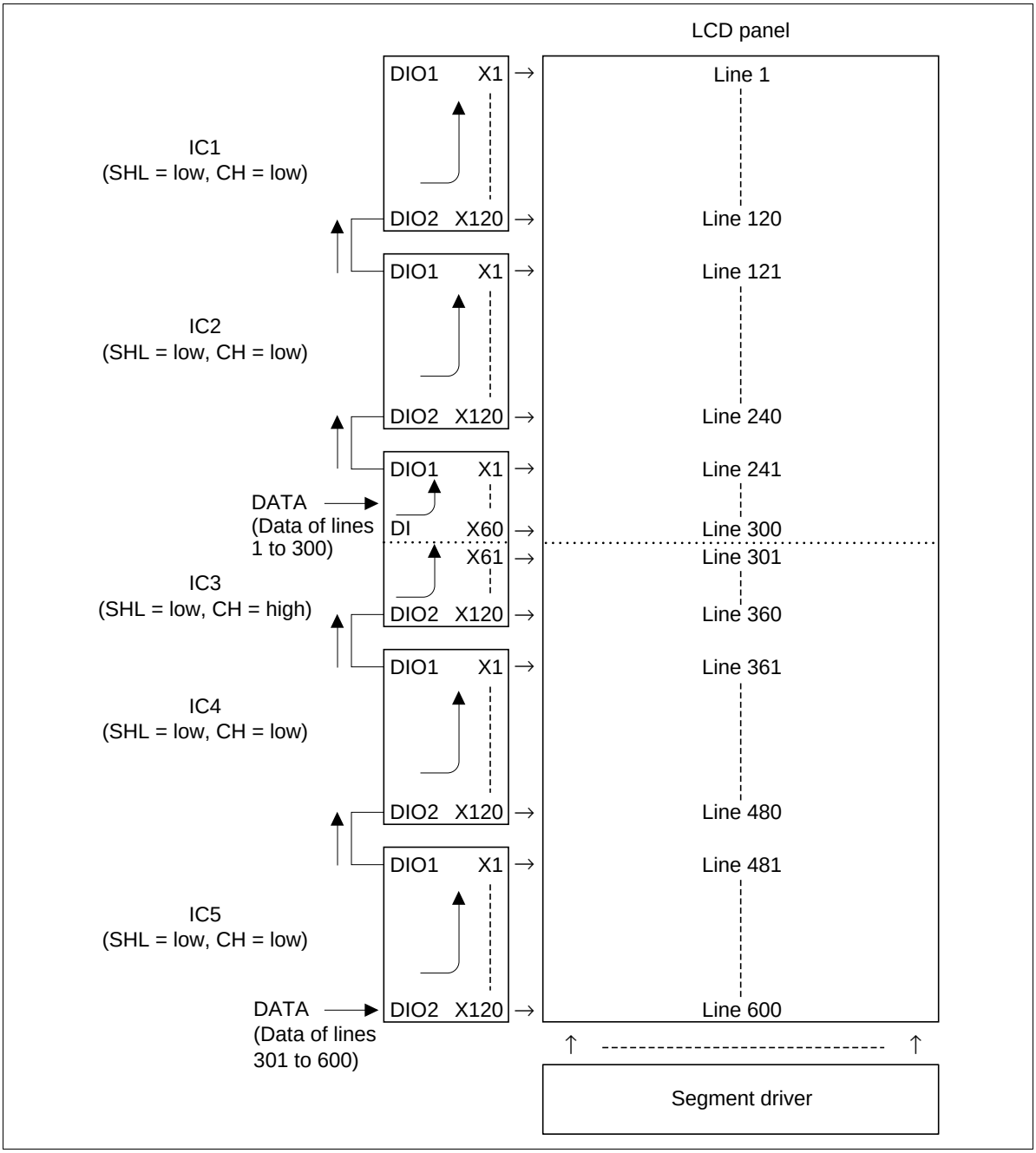


Figure 9 Dual-Screen Configuration of a 600-Line LCD Panel with a 1/300 Duty Cycle (2)

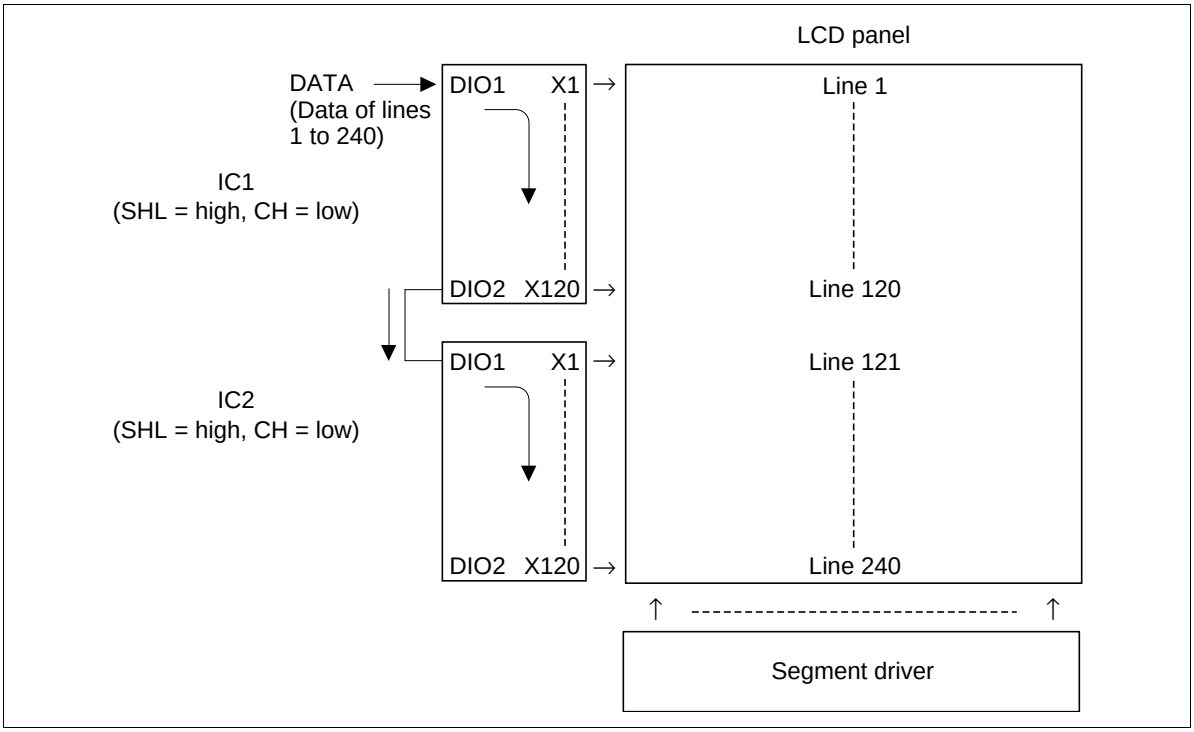


Figure 10 Single-Screen Configuration of a 240-Line LCD Panel with a 1/240 Duty Cycle (1)

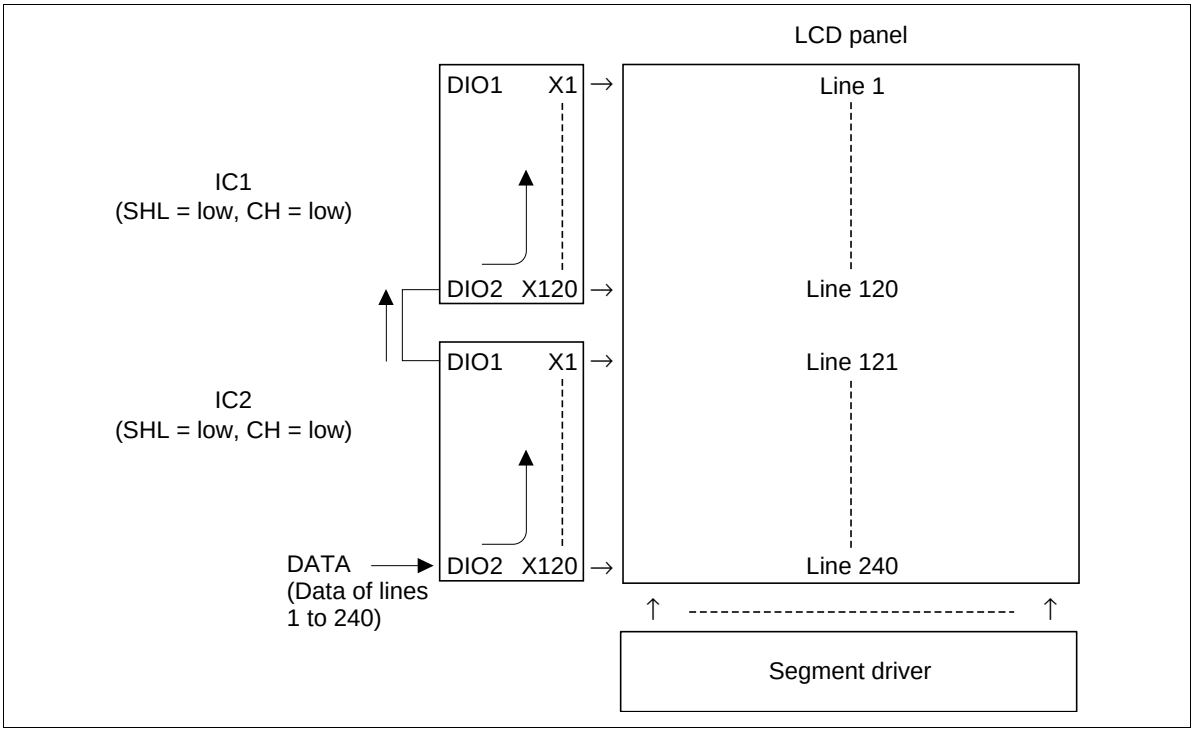


Figure 11 Single-Screen Configuration of a 240-Line LCD Panel with a 1/240 Duty Cycle (2)

Notes on Power-On/Off of the LCD Driver

To prevent an LCD driver display error at power on/off, the sequence for power-on signal activation must be as follows (see Figure 12):

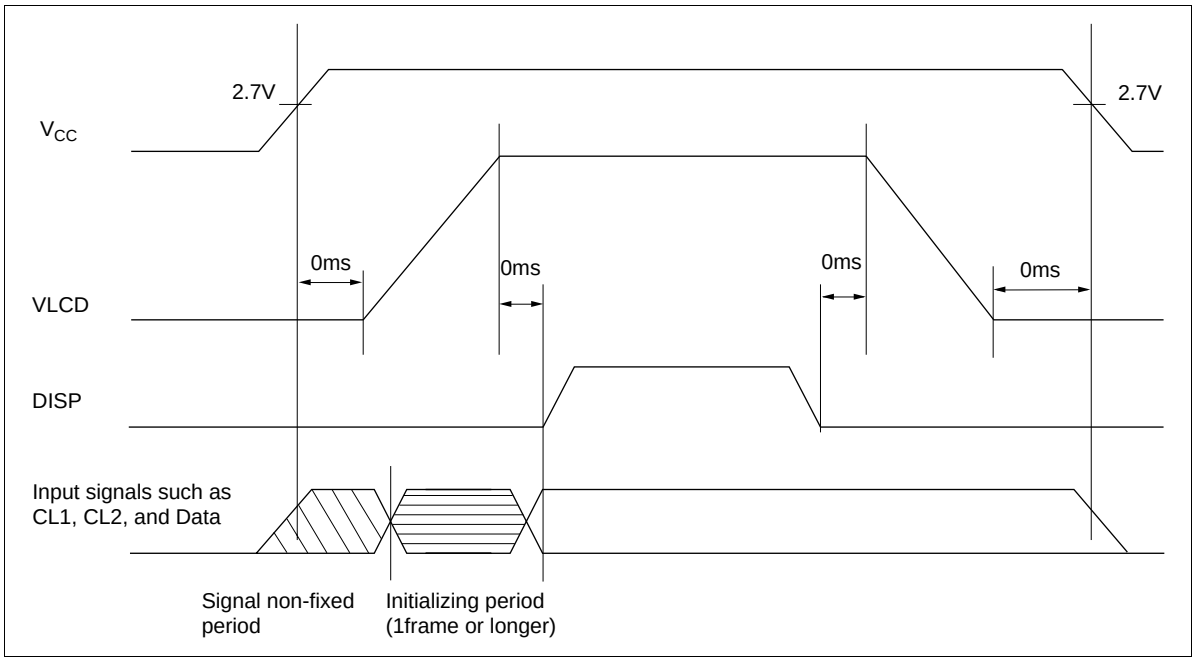


Figure 12 Sequence of Power-On/Off

At Power On

(1) Power on V_{CC}. At this time, input 0 to the $\overline{DISP}$ pin.
(2) Display-off function forces the LCD driver to output a V2 level (lowest level).
(3) Display-off function takes priority even if the input signal status becomes irregular immediately after V_{CC} power-on.
(4) Input the specified signals to initialize registers of the LCD driver. Its period must be 1 frame or longer.
(5) Set the $\overline{DISP}$ level to 1 to cancel display-off function after steps (1) to (4). At this time, VLCD and each V pin input must be at the specified levels.

At Power Off

Basically, the power-off procedure is the reverse of the power-on procedure.

(1) Set the $\overline{DISP}$ level to 0.
(2) Lower LCD driver power supply to 0V
(3) Lower V_{CC} and each input signals to 0V

At this time, each V pin input must be at 0V. Display-off function stops when V_{CC} falls to 0V, and therefore, the LCD driver may output a level other than V2 (lowest level). As a result, a display error may be caused at power-off or power-on.

LCD Driver LSI Power Supply Pin Connection

A feature of the LCD driver is the LCD drive power supply. As the number of pixel drives per LSI increases, so does the voltage and number of outputs.

Consequently, if multi-output CMOS circuits are switched simultaneously, a wiring voltage drop may occurs due to transient currents, and the potential between the LCD drive circuit power supply (V_{LCD}) and LCD drive level power supplies (V1, V6, and V3) or GND and the LCD level power supplies (V2, $\overline{V5}$, and V4) may be inverted, resulting in latchup breakdown. To prevent this, it is recommended that, when designing the LCD drive power supply and board power supply wiring, the power supply wiring be designed as low-impedance and capacitors be inserted in the wiring between V_{LCD} and V1, V3, V6, and between V2, V4, V5 and GND. In set evaluation, it is recommended that a check be carried out to confirm that there is no inversion of the LCD drive power supply and level power supplies in the period between when the LCD drive power supply is turned on and turned off.

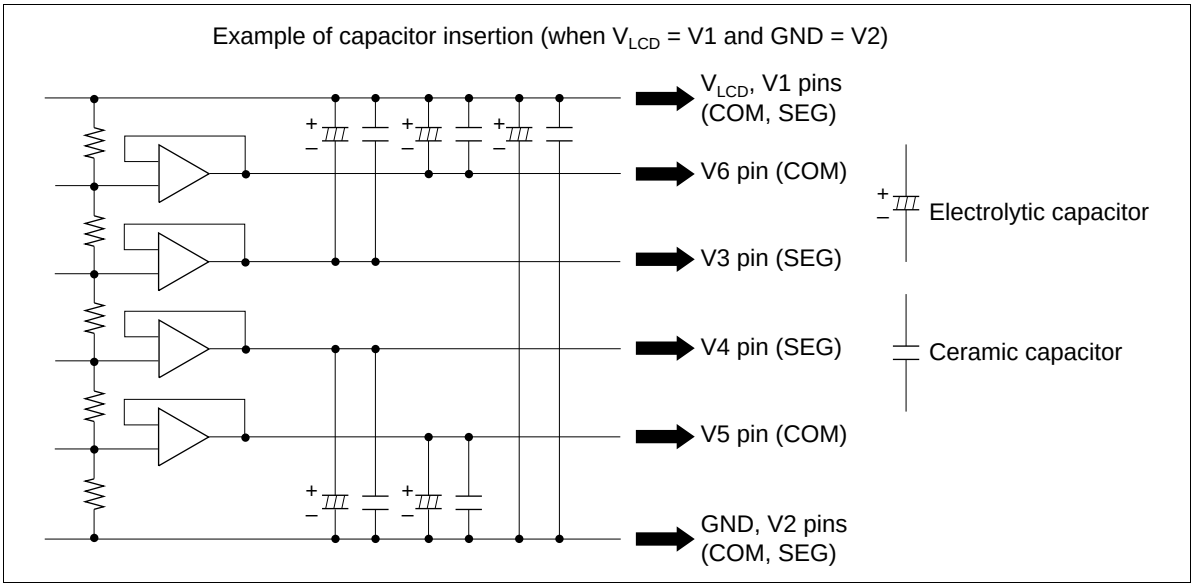


Figure 13 Example of Capacitor Insertion